User's Guide
SLLU295–February 2018

UCC5390ECDWV Isolated Gate Driver Evaluation Module User's Guide

This manual describes the UCC5390ECDWV evaluation module (EVM). The UCC5390ECDWVEVM allows designers to evaluate AC and DC performance of the UCC53x0 family of devices (split output, Miller clamp, and UVLO) in a DWV package with user-installed IGBT in the standard TO-247 package.

WARNING

Although these devices provide galvanic isolation of up to 5000 V, the EVM cannot be used for isolation voltage testing. Voltage exceeding the EVM ratings (V_{CC1} > 15 V, V_{CC2} – V_{EE2} > 33 V, or IGBT collector-emitter voltage V_{CE} > 50 V) can damage the EVM resulting in personal injury.

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1 Overview

The UCC53x0xDWV devices are 5-kV_{RMS}, IGBT and MOSFET gate drivers with split outputs (UCC53x0S), Miller clamp (UCC53x0M), and UVLO (UCC53x0E) features. These gate drivers are capable of sourcing and sinking 1.1 A to 10 A of peak current, depending on the device. The input side operates from a single 3-V to 15-V supply. The output side allows for a supply range from a minimum of 13.2 V to a maximum of 33 V. Two complementary CMOS inputs control the output state of the gate driver. The short propagation time ensures accurate control of the output stage.

When the IGBT is turned off during normal operation with bipolar output supply, the output is hard clamped to V_{EE2} in a UVLO (UCC53x0E) device. The UCC53x0M devices, with a unipolar output supply, have an active Miller clamp, allowing Miller current to sink across a low-impedance path, which prevents the IGBT from being dynamically turned on during high-voltage transient conditions. The UCC53x0S device, which has a split output, provides better control over the rise and fall time of the driver output.

2 Pin Configuration of the UCC53x0 Isolated IGBT Gate Drivers

Figure 1 shows the UCC53x0 pin configurations.

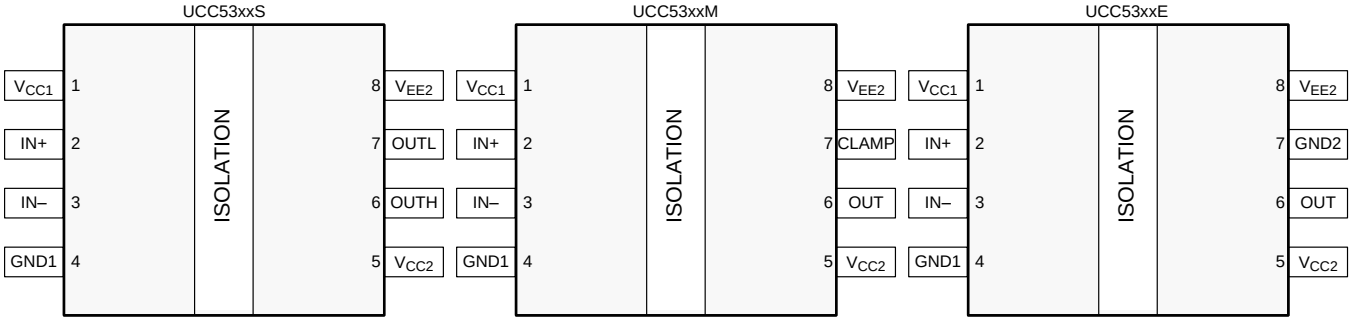

Figure 1. UCC53x0 Pin Configurations

3 EVM Setup and Precautions

3.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the UCC5390ECDWVEVM. Observe all safety precautions.

Warning Warning hot surface. Contact may cause burns. Do not touch.

Danger High Voltage The UCC5390ECDWVEVM does not have an isolation boundary. If you apply high voltage to this board, all terminals should be considered high voltage.

Electric shock is possible when connecting the board to live wire. The board should be handled with care by a professional.

For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

CAUTION

Do not leave the EVM powered while unattended.

The IGBT device can be populated onboard only for low current functionality testing. If the IGBT device requires a heat sink (high load current), it must be externally connected and is not recommended to be populated on EVM.

3.2 Power Supply Connections

Figure 2 shows the UCC5390ECDWVEVM power supply schematic.

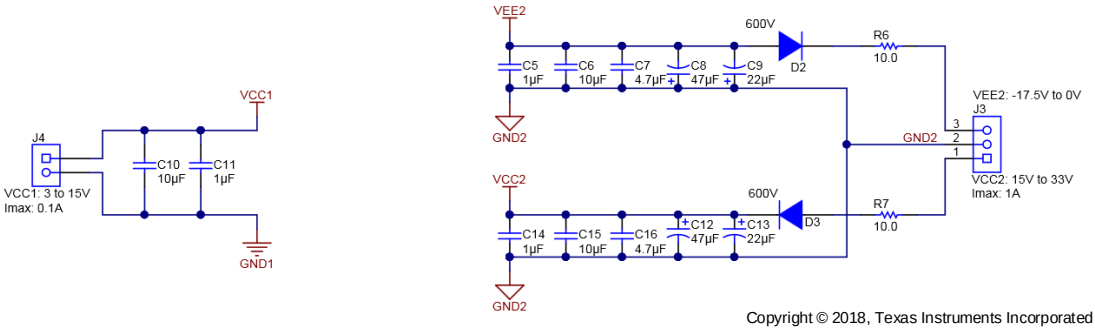

Figure 2. UCC5390ECDWVEVM Power Supply Schematic

The input side of the UCC53x0x EVM (V_{CC1}) operates from a single 3-V to 15-V power supply and is connected by J4. A test point (TP1) is available for monitoring the input power supply.

The UCC5390ECDWVEVM provides connections for evaluating the output side (V_{CC2}, V_{EE2}) with either a bipolar or unipolar power supply, from a minimum 13.2 V to maximum 33 V. V_{CC2} and V_{EE2} can be supplied at J3. The D2 and D3 diodes and R6 and R7 resistors are provided for supply reverse polarity protection and to limit the supply current.

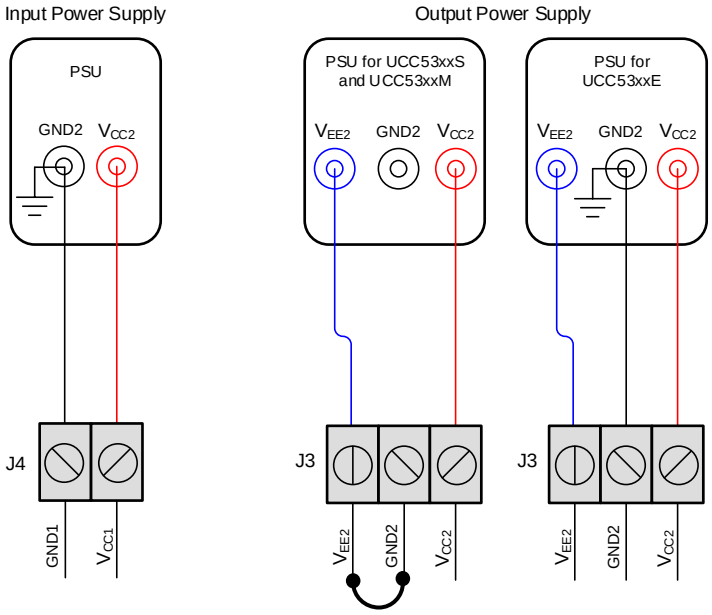

Figure 3. Input Power Supply (J4) and Output Power Supply (J3)

3.3 Signal Connections

The UCC5390ECDWVEVM is a universal EVM designed to support the UCC53x0xDWV family of devices. The same EVM can be used for a split output, Miller clamp, and UVLO device by configuring it according to Table 1, while referencing Figure 4.

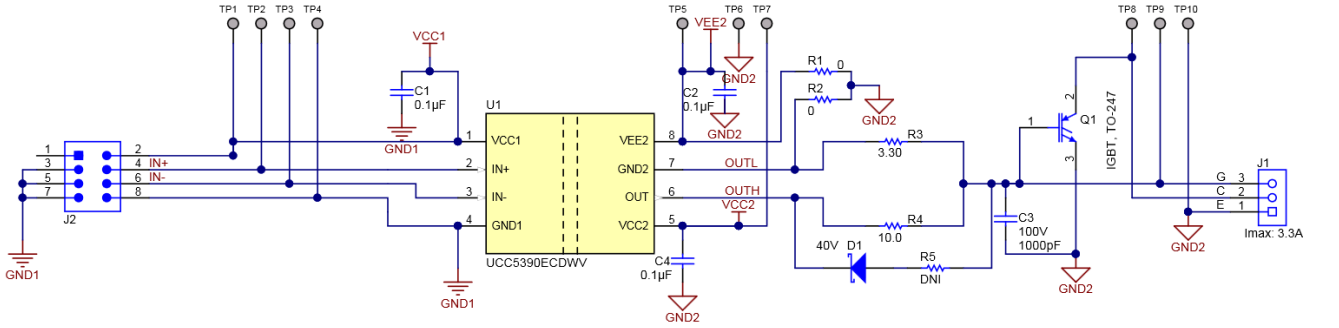

Figure 4. UCC5390ECDWVEVM Signal Path Schematic

Table 1 lists the UCC53x0 configurations.

Table 1. UCC5390ECDWVEVM Configurations

UCC53x0 Configurations	Pin 7	R3	R5	R2	R1
UCC53x0S: Split	OUTL	3.3 Ω	DNI	DNI	0 Ω
UCC53x0M: Miller	CLAMP	0 Ω	10 Ω	DNI	0 Ω
UCC53x0E: UVLO-GND2	GND2	DNI	10 Ω	0 Ω	DNI

3.3.1 I/O Connections

Figure 4 shows the signal path schematic of the EVM. The J2 jumper allows for stimulus or monitoring of the device input pins IN+ and IN–. The test points TP2 and TP3 provide additional access to the I/O pins.

3.3.2 Output and Loading

The EVM provides the option of driving a capacitive load (not provided) or a user provided FET/IGBT. The output can be monitored directly with TP9. The gate resistors, R3 and R4, control the rise and fall times of the output (OUTH and OUTL). These resistors can be modified by the user to alter the turnon and turnoff characteristics of the output.

The EVM also allows for functional evaluation of the device with an IGBT at light loads (low current and voltage < 50 V). If the IGBT device requires a heat sink (higher load current), it should be externally connected, and is not recommended to be populated on the EVM. During evaluation with an IGBT load, the capacitive load must be removed.

The EVM provides an additional connection (J1) for applying an external power supply to the IGBT collector. The EVM is not intended for high-voltage testing and the voltage applied to J1 should be limited to 50-V DC.

3.3.3 EVM Configurations

3.3.3.1 Split (UCC53x0S)

The OUTL pin (pin 7) is connected to the gate by a 3.3-Ω resistor (R3), while the OUTH pin is connected to the gate using a 10-Ω resistor (R4). This configuration enables separate control over rise and fall times. The R2 and R5 resistors must be removed, and the R1 resistor must be connected by a 0-Ω resistor to ensure proper connection to the GND2 node.

3.3.3.2 Miller-Clamp (UCC53x0M)

The CLAMP pin (pin 7) is connected to the gate by a 0-Ω resistor (R3). The gate must also be connected to the OUT pin with a diode and series 10-Ω resistance (R5). The R2 resistor must be removed, and the R1 resistor must be connected by a 0-Ω resistor to ensure proper connection to the GND2 node.

3.3.3.3 UVLO-GND2 (UCC53x0E)

In this configuration, pin 7 becomes the GND2 pin, while pin 8 becomes V_{EE2}, where negative voltage with respect to GND2 can be applied. The R1 and R3 resistors must both be removed, and the R2 resistor must be connected by a 0-Ω resistor to ensure proper connection to the GND2 pin (pin 7). The gate must also be connected to the OUT pin with a diode and series 10-Ω resistance (R5).

4 Example Measurements

Figure 4 shows measurements performed under the default EVM configuration (with R3 = DNI, R2 = 0 Ω, and R4 and R5 not populated). For these measurements, V_{IN-} is connected to GND1.

Figure 5 shows output of the UCC5390ECDWVEVM for a 10-kHz input signal with R2 = 0 Ω, R1 and R3 not populated, and a unipolar output supply (V_{CC2} = 18 V, V_{EE2} = GND2).

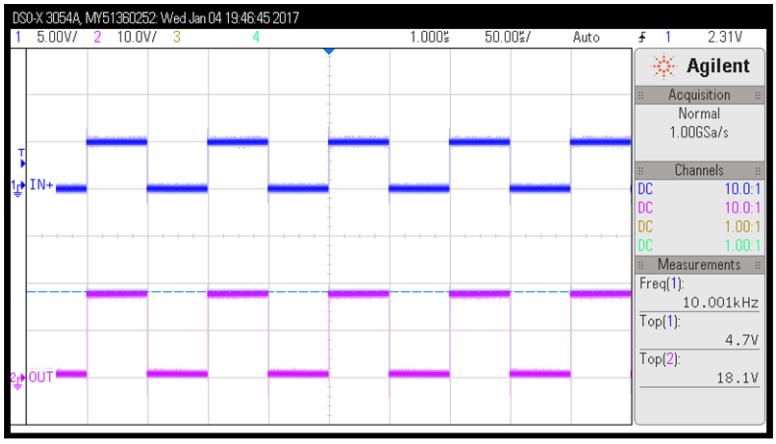

Figure 5. Input and Output With Unipolar Output Supply

Figure 6 shows output of the UCC5390ECDWVEVM for a 10-kHz input signal with R5 = 10 Ω, R2 = 0 Ω, R1 and R4 not populated, and a bipolar output supply (V_{CC2} = 15 V, V_{EE2} = –15 V).

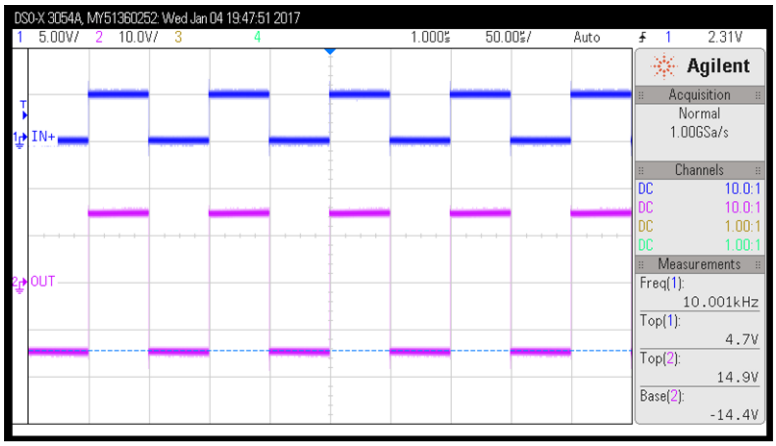

Figure 6. Input and Output With Bipolar Output Supply

5 Printed-Circuit Board and Layout

The UCC53x0 device is an isolated gate driver with several important features. The printed-circuit board (PCB) and EVM, as shown in (wide-body SOIC (8) DWV package), have been designed to support the UCC53x0S, UCC53x0M, UCC53x0E family of devices and to allow the user to evaluate basic operation and features. The left side of the PCB contains the interface to the input and control functions of the integrated circuit (IC). The right side of the PCB has been designed to interface to an IGBT. No electrical connections exist between the right and left sides of the PCB.

Figure 7 and Figure 8 show the PCB layout for the UCC5390ECDWVEVM.

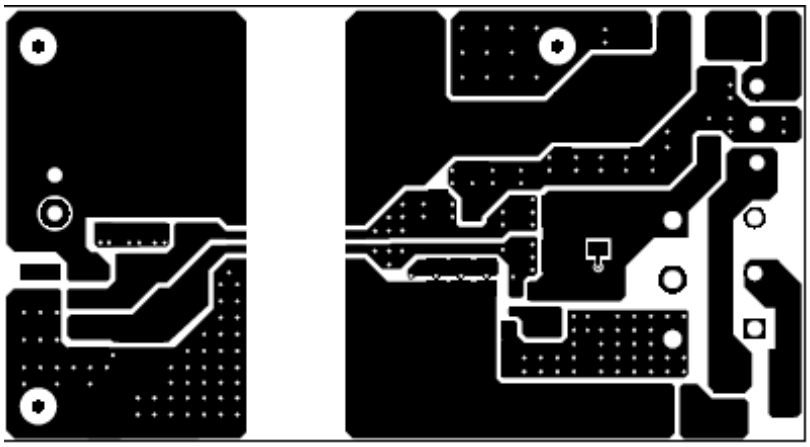

Figure 7. UCC5390ECDWVEVM Top Layer

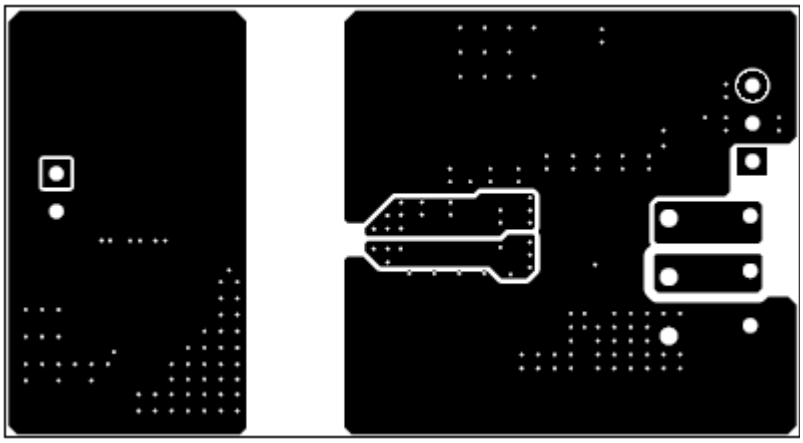

Figure 8. UCC5390ECDWVEVM Bottom Layer

5.1 UCC5390ECDWVEVM Operation

5.1.1 Input-Side Operation: DC Power and Control

5.1.1.1 DC Input Power

The left side of the UCC5390ECDWVEVM (and therefore the PCB) can be operated using either a 3-V (±10%) to 15-V (±10%) DC power supply. Or, the user can choose to operate the UCC5390ECDWVEVM by battery. The DC power supply must be connected to the J4 terminal.

5.1.1.2 Control

The interface to the device is through the J2 header. It contains the IN+ and IN– inputs. The J1 header allows easy connections to test equipment using standard clip leads. The IN+ and IN– control signals have test points for additional connections. These are test points TP2 and TP3.

5.1.2 Output-Side Operation

5.1.2.1 DC Output Power

Power is provided to V_{CC2} on the right side of the device at the J3 terminal, as shown in Figure 3. The DC supply must be able to provide a bias voltage over the range of 13.2-V DC to 33-V DC. The user can choose to operate the UCC5390ECDWV by battery. If a negative gate drive is required, a DC supply (or battery) must be connected across V_{EE2} (–17.5 V to 0 V) at the J3 terminal, as shown in Figure 3. The voltage across V_{CC2} and V_{EE2} must not exceed 33 V for operation. Take note of the supply voltage range and UVLO of the gate driver under evaluation.

5.1.2.2 Load

As shipped, the UCC5390ECDWVEVM does not have an IGBT or load capacitor installed. The user can populate IGBT for low-current functionality testing at the pads provided. The IGBT device that requires a heat sink (higher load current) should be externally connected and is not recommended to be populated on the EVM. Most IGBTs are available in the standard TO-247 package.

5.1.3 Test Points

Test points have been provided for ready access to signal monitoring and are listed in Table 2.

Table 2. Test Points

Test Point	Type	Function
TP1	Supply	V_{CC1} (side1)
TP2	Input	IN+ (side1)
TP3	Input	IN– (side1)
TP4	Ground	GND1 (Side1)
TP8	Input	Collector voltage (side2)
TP9	Output	Gate voltage (side2)
TP10	Input	Emitter voltage (side2)
TP5	GND and negative supply voltage	UCC53x0E: V_{EE2} (side2)
		UCC53x0S: GND2 (side2)
		UCC53x0M: GND2 (side2)
TP6	GND	GND2 (side2)
TP7	Supply	V_{CC2} (side 2)

5.2 UCC53x0D EVM Bill of Materials

Table 3 lists the UCC53x0D EVM bill of materials.

Table 3. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1, C2, C4	3	0.1 µF	Capacitor, ceramic, 0.1 µF, 50 V, ± 10%, X7R, 0805	0805	C0805C104K5RACTU	Kemet
C5, C11, C14	3	1 µF	Capacitor, ceramic, 1 µF, 50 V, ± 10%, X7R, 0805	0805	C0805C105K5RACTU	Kemet
C6, C10, C15	3	10 µF	Capacitor, ceramic, 10 µF, 50 V, ± 10%, X5R, 1206_190	1206_190	CL31A106KBHNNNE	Samsung Electro-Mechanics
C7, C16	2	4.7 µF	Capacitor, ceramic, 4.7 µF, 50 V, ± 10%, X5R, 0805	0805	C2012X5R1H475K125AB	TDK
C8, C12	2	47 µF	Capacitor, AL, 47 µF, 50 V, ± 20%, 0.68 Ω, AEC-Q200 Grade 2, SMD	SMT Radial D8	EEE-FK1H470XP	Panasonic
D1	1	40 V	Diode, Schottky, 40 V, 0.75 A, AEC-Q101, SOD-323	SOD-323	BAT165E6327HTSA1	Infineon Technologies
D2, D3	2	600 V	Diode, Ultrafast, 600 V, 2 A, SMB	SMB	MURS160T3G	ON Semiconductor
J1	1		Terminal Block, 3 × 1, 5.08 mm, TH	3x1 Terminal Block	OSTTA034163	On-Shore Technology
J2	1		Header, 100 mil, 4x2, Gold, SMT	Header, 100mil, 4x2, SMT	0015910080	Molex
J3	1		Terminal Block, 3.5 mm Pitch, 3 × 1, TH	10.5x8.2x6.5mm	ED555/3DS	On-Shore Technology
J4	1		Terminal Block, 3.5 mm Pitch, 2 × 1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
R1, R2	2	0	RES, 0, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	1210	CRCW12100000Z0EAHP	Vishay-Dale
R4, R6, R7	3	10.0	RES, 10.0, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	1210	CRCW121010R0FKEAHP	Vishay-Dale
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	10		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		5-kVRMS Single-Channel Isolated Gate Drivers, DWV0008A (SOIC-8)	DWV0008A	UCC5390ECDWV	Texas Instruments
C3	0	1000 pF	Capacitor, ceramic, 1000 pF, 100 V, ± 5%, C0G/NP0, 0805	0805	C0805C102J1GACTU	Kemet
C9, C13	0	22 µF	Capacitor, AL, 22 µF, 50 V, ± 20%, 0.88 Ω, AEC-Q200 Grade 2, SMD	SMT Radial D	EEE-FK1H220P	Panasonic
Q1	0	650 V	IGBT, TO-247	TO-247	IKW50N65F5FKSA1	Infineon Technologies
R3	0	3.30	RES, 3.30, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	1210	CRCW12103R30FKEAHP	Vishay-Dale
R5	0	10.0	RES, 10.0, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	1210	CRCW121010R0FKEAHP	Vishay-Dale

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