

50 MHz to 750 MHz CASCADEABLE AMPLIFIER

Check for Samples: [THS9001](#)

FEATURES

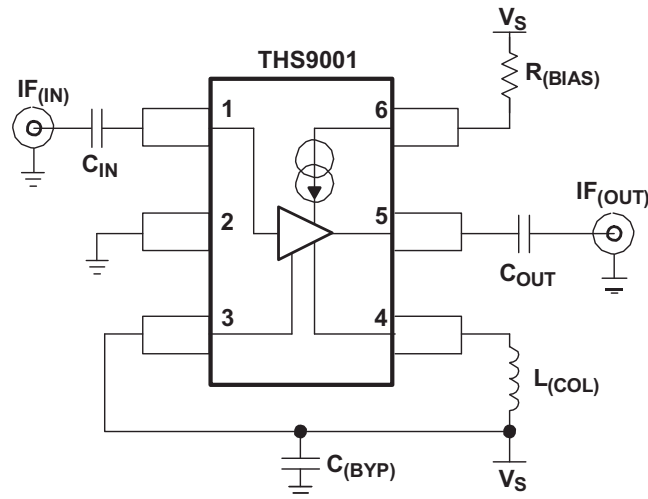
- **High Dynamic Range**
 - $OIP_3 = 36 \text{ dBm}$
 - $NF < 4.5 \text{ dB}$
- **Single-Supply Voltage**
- **High Speed**
 - $V_S = 3 \text{ V to } 5 \text{ V}$
 - $I_S = \text{Adjustable}$
- **Input/Output Impedance**
 - 50Ω

APPLICATIONS

- **IF Amplifiers**
 - TDMA: GSM, IS-136, EDGE/UWE-136
 - CDMA: IS-95, UMTS, CDMA2000
 - **Wireless Local Loops**
 - **Wireless LAN: IEEE802.11**

DESCRIPTION

The THS9001 is a medium power, cascadeable, gain block optimized for high IF frequencies. The amplifier incorporates internal impedance matching to 50Ω , and achieves greater than 15-dB input, and output return loss from 50 MHz to 350 MHz with $V_S = 5 \text{ V}$, $R_{(\text{BIAS})} = 237 \Omega$, $L_{(\text{COL})} = 470 \text{ nH}$. Design requires only 2 dc-blocking capacitors, 1 power-supply bypass capacitor, 1 RF choke, and 1 bias resistor.

Function Block Diagram


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

PACKAGED DEVICE ⁽¹⁾	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
THS9001DBVT	SOT-23-6	Tape and Reel, 250
THS9001DBVR		Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature (unless otherwise noted)⁽¹⁾

		UNIT	
V _{SS}	Supply voltage, GND to V _S	5.5	
V _I	Input voltage	GND to V _S	
	Continuous power dissipation	See Dissipation Rating table	
T _J	Maximum junction temperature	150°C	
T _J	Maximum junction temperature, continuous operation, long term reliability ⁽²⁾	125°C	
T _{stg}	Storage temperature	–65 to 150°C	
:	ESD Ratings	HBM	2000
		CDM	1500
		MM	100

- (1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING ⁽¹⁾	
			T _A ≤ 25°C	T _A = 85°C
DBV ⁽²⁾	70.1	215	463 W	185 mW

- (1) Power rating is determined with a junction temperature of 125°C. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance.
- (2) This data was taken using the JEDEC standard High-K test PCB.

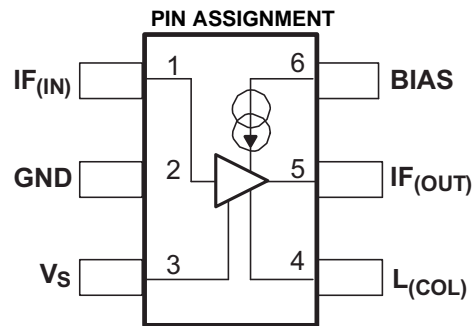
RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{SS}	Supply voltage	2.7		5	V
T _A	Operating free-air temperature,	–40		85	°C
I _S	Supply current		100		mA

ELECTRICAL CHARACTERISTICS

 Typical Performance ($V_S = 5\text{ V}$, $R_{(\text{BIAS})} = 237\ \Omega$, $L_{(\text{COL})} = 470\text{ nH}$) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain	$f = 50\text{ MHz}$		15.8		dB
	$f = 350\text{ MHz}$		15		
OIP ₃	$f = 50\text{ MHz}$		35		dBm
	$f = 350\text{ MHz}$		37		
1-dB compression	$f = 50\text{ MHz}$		20.6		dBm
	$f = 350\text{ MHz}$		20.6		
Input return loss	$f = 50\text{ MHz}$		15.4		dB
	$f = 350\text{ MHz}$		16.6		
Output return loss	$f = 50\text{ MHz}$		17		dB
	$f = 350\text{ MHz}$		15		
Reverse isolation	$f = 50\text{ MHz}$		20.7		dB
	$f = 350\text{ MHz}$		20.7		
Noise figure	$f = 50\text{ MHz}$		3.7		dB
	$f = 350\text{ MHz}$		4		



Terminal Functions

PIN NUMBERS	NAME	DESCRIPTION
1	IF _(IN)	Signal input
2	GND	Negative power-supply input
3	V _S	Positive power-supply input
4	L _(COL)	Output transistor load inductor
5	IF _(OUT)	Signal output
6	BIAS	Bias current input

SIMPLIFIED SCHEMATIC

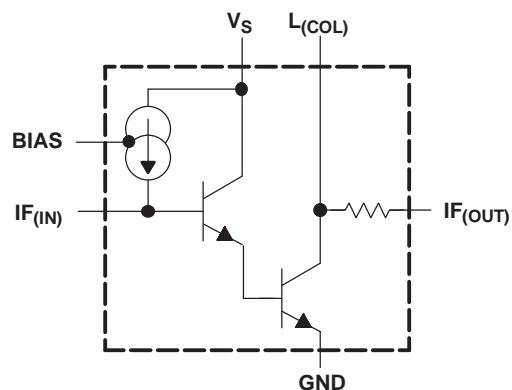


TABLE OF GRAPHS

		FIGURE
	S21 Frequency response	1
	S22 Frequency response	2
	S11 Frequency response	3
	S12 Frequency response	4
	S21 vs $R_{(Bias)}$	5
	Noise figure vs Frequency	6
I_S	Supply current vs $R_{(Bias)}$	7
	Output power vs Input power	8
	Adjacent channel (ACPR) and Alternate channel (AltCPR) protection ratios vs Input power	9
	OIP ₂ vs Frequency	10
	OIP ₃ vs Frequency	11
	S21 Frequency response	12
	S22 Frequency response	13
	S11 Frequency response	14
	S12 Frequency response vs Frequency	15
	Noise figure	16
	OIP ₂ vs Frequency	17
	Output power vs Input power	18
	OIP ₃ vs Frequency	19

TYPICAL CHARACTERISTICS

S-Parameters of THS9000 as mounted on the EVM with $V_S = 5\text{ V}$, $R_{(BIAS)} = 237\ \Omega$, and $L_{(COL)} = 68\text{ nH}$ to 470 nH at room temperature.

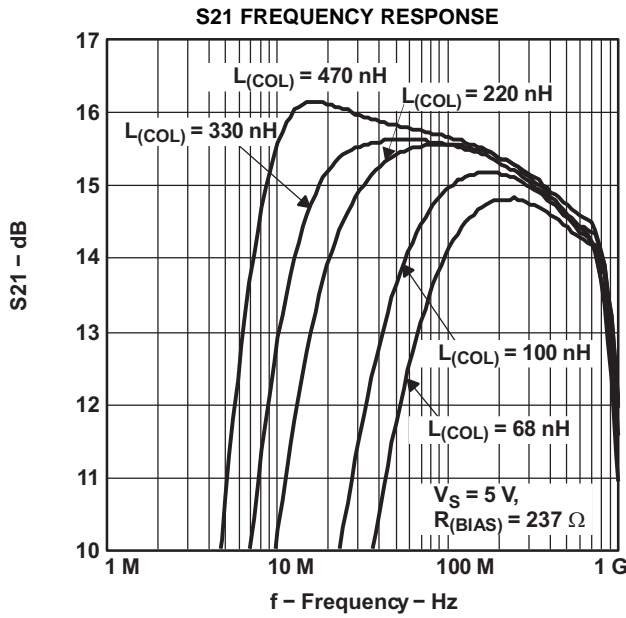


Figure 1.

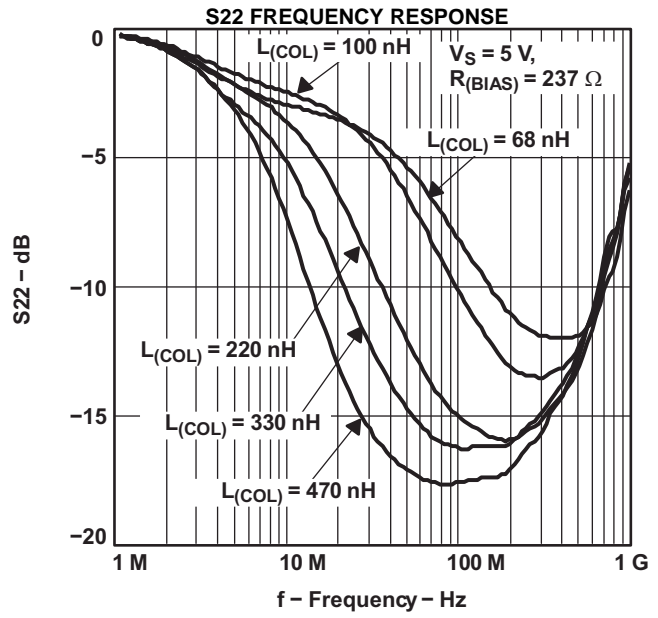


Figure 2.

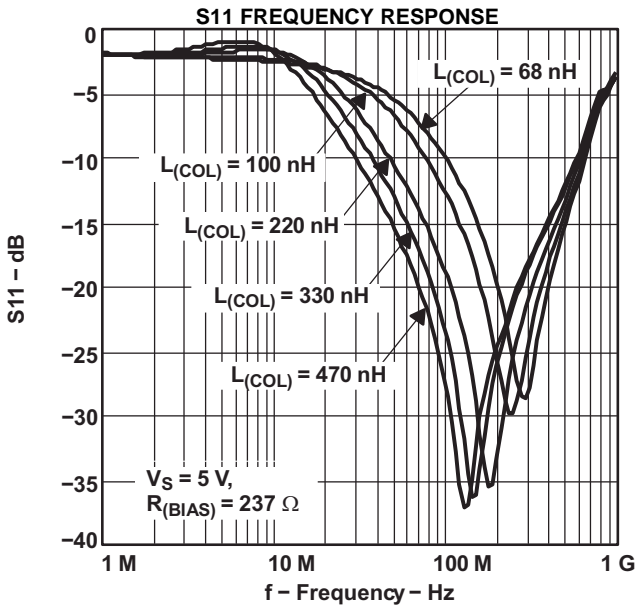


Figure 3.

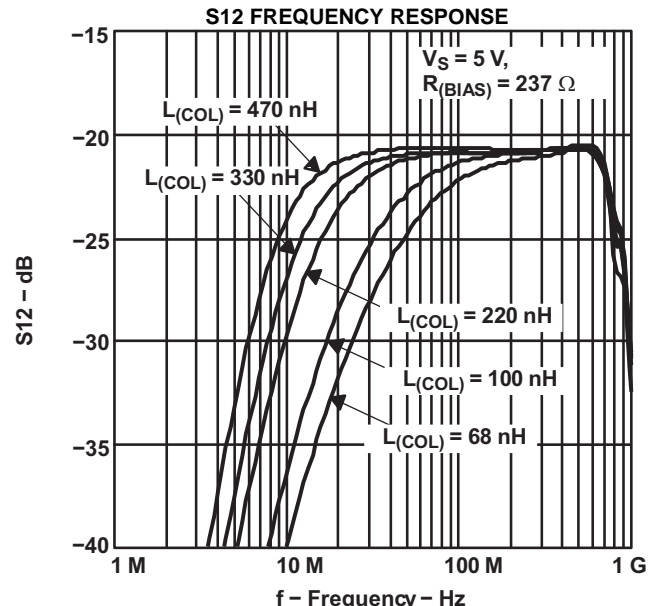


Figure 4.

TYPICAL CHARACTERISTICS

S-Parameters of THS9000 as mounted on the EVM with $V_S = 3\text{ V}$ and 5 V , $R_{(BIAS)}$ = various, and $L_{(COL)} = 470\text{ nH}$ at room temp.

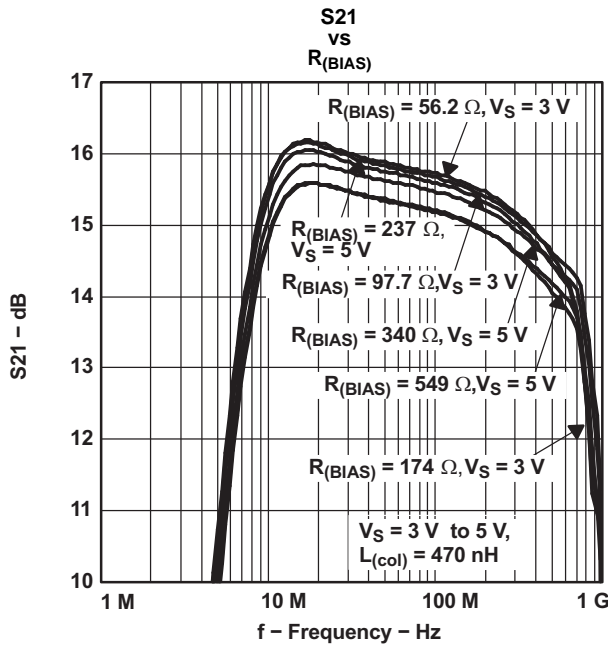


Figure 5.

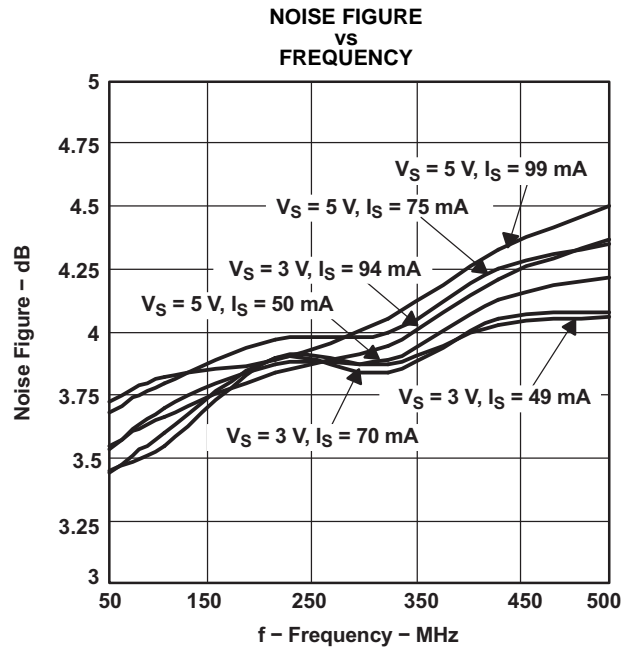


Figure 6.

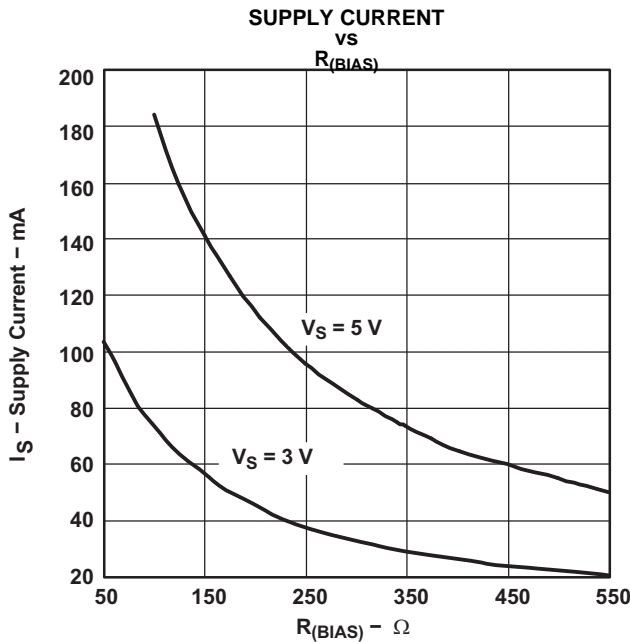


Figure 7.

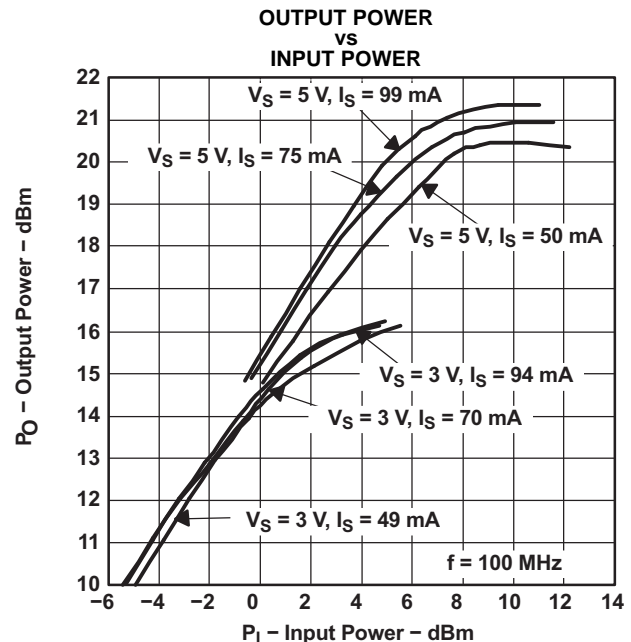
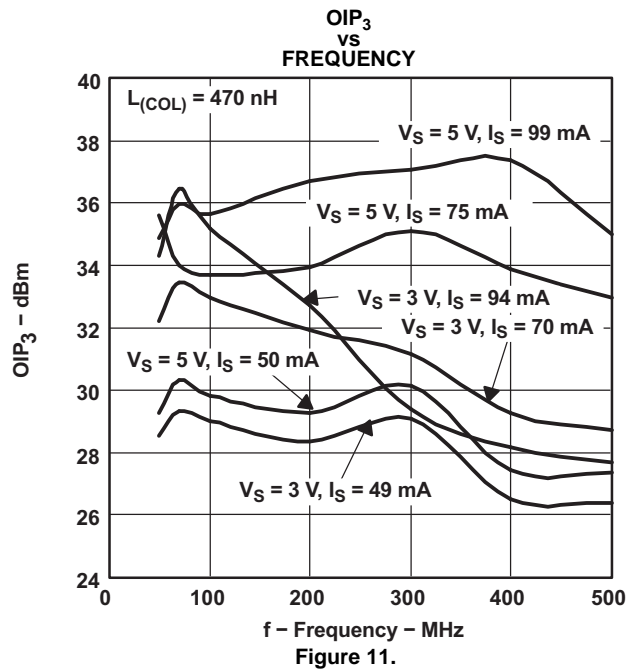
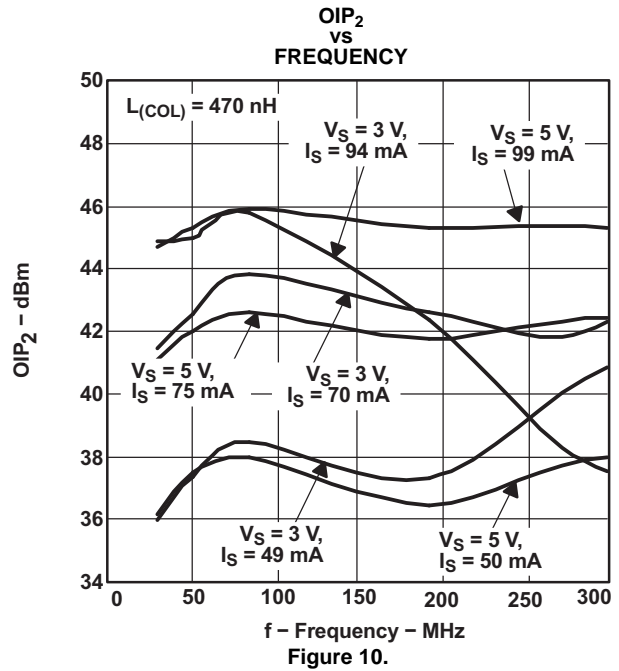
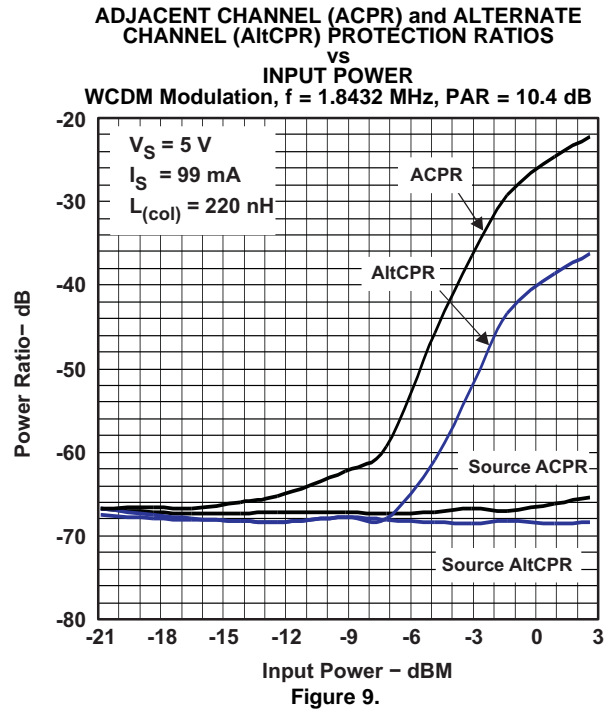


Figure 8.

TYPICAL CHARACTERISTICS (continued)

S-Parameters of THS9000 as mounted on the EVM with $V_S = 3\text{ V}$ and 5 V , $R_{(BIAS)}$ = various, and $L_{(COL)} = 470\text{ nH}$ at room temp.



TYPICAL CHARACTERISTICS

THS9000 as mounted on the EVM with $V_S = 3\text{ V}$ and 5 V , $R_{(BIAS)} = 237\ \Omega$, and $L_{(COL)} = 470\text{ nH}$ at -40°C , 25°C , and 85°C .

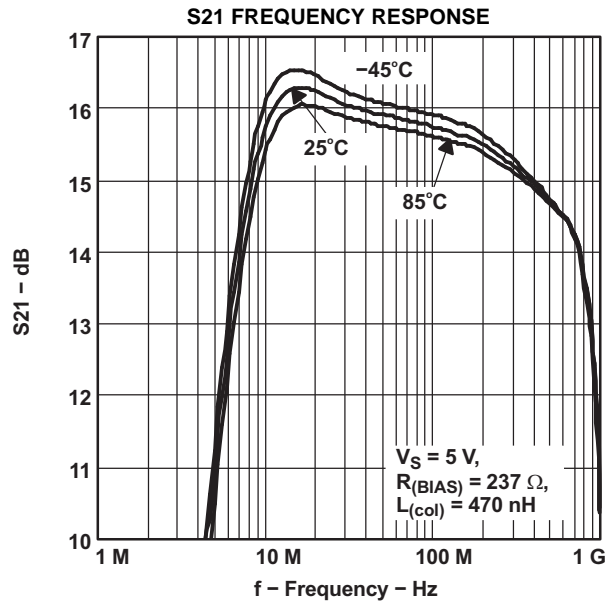


Figure 12.

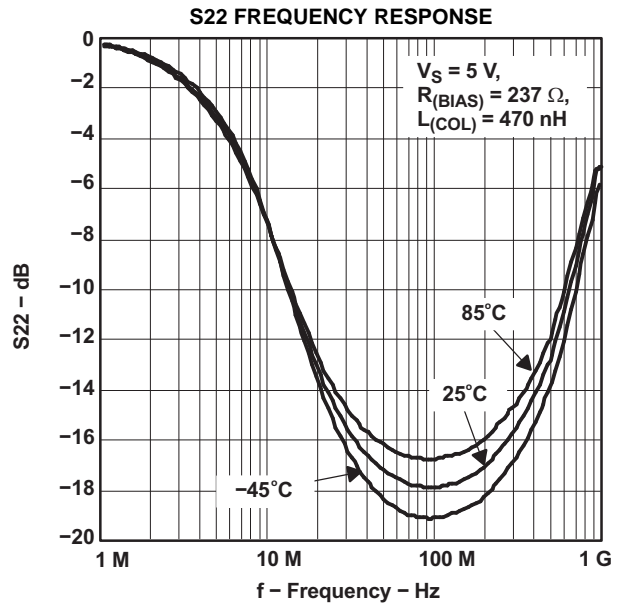


Figure 13.

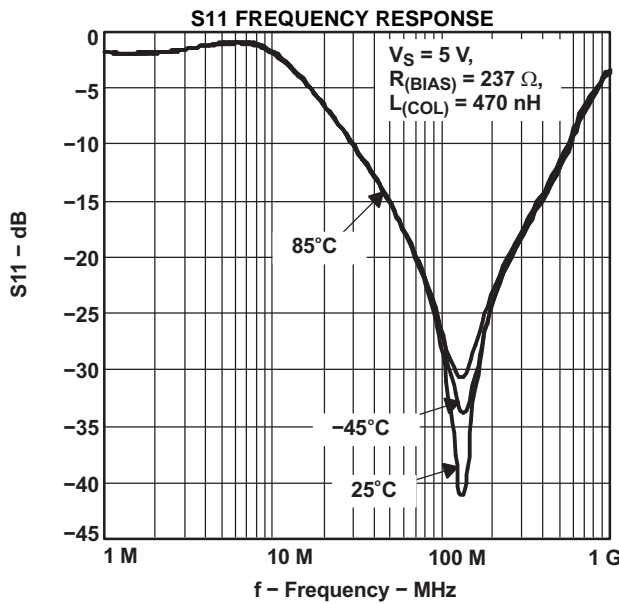


Figure 14.

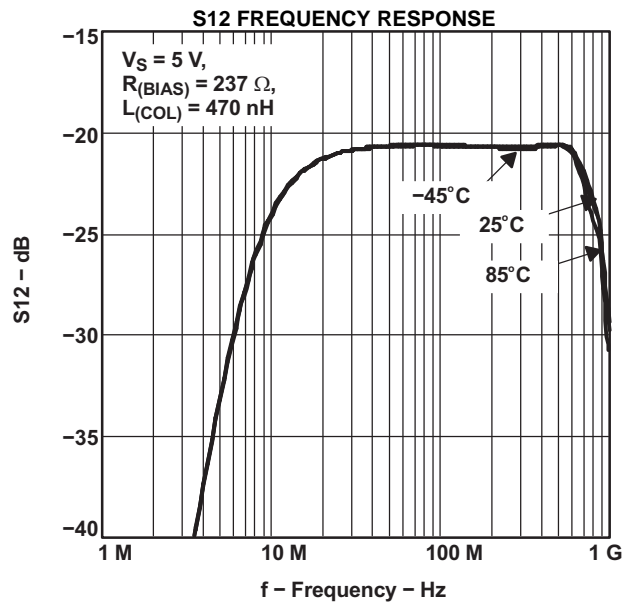
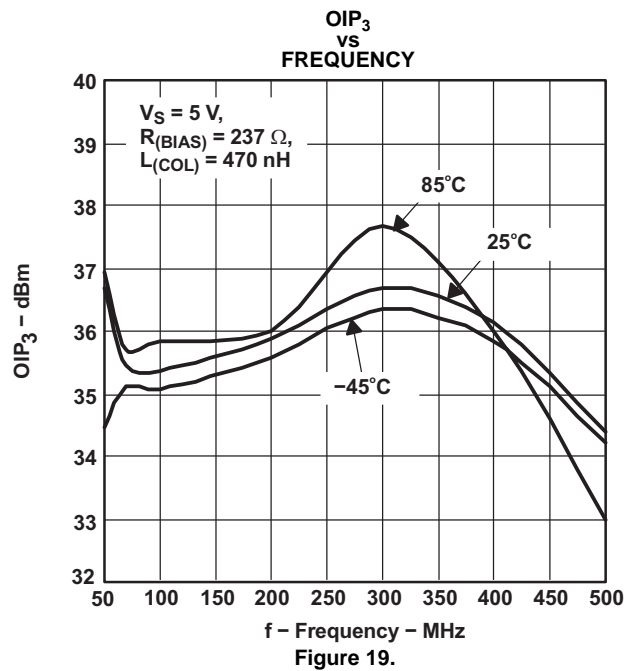
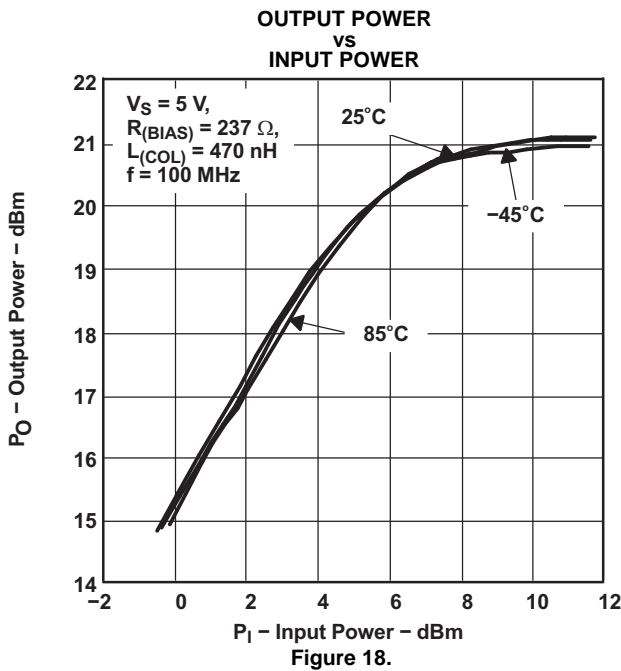
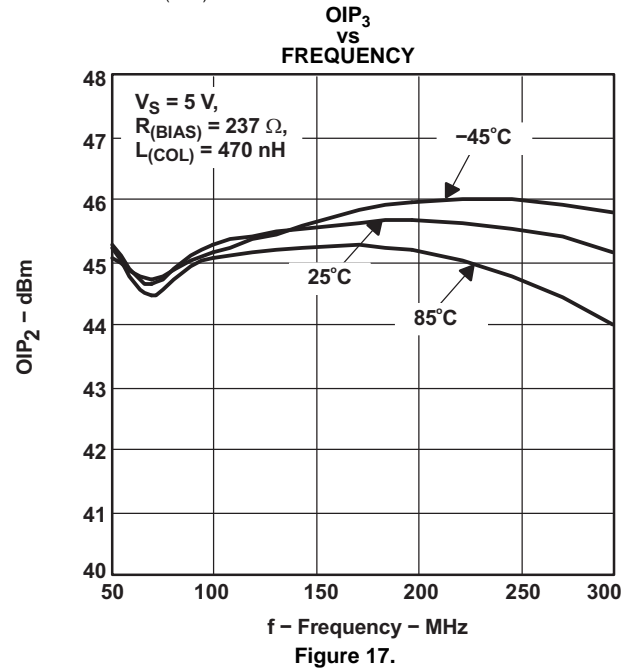
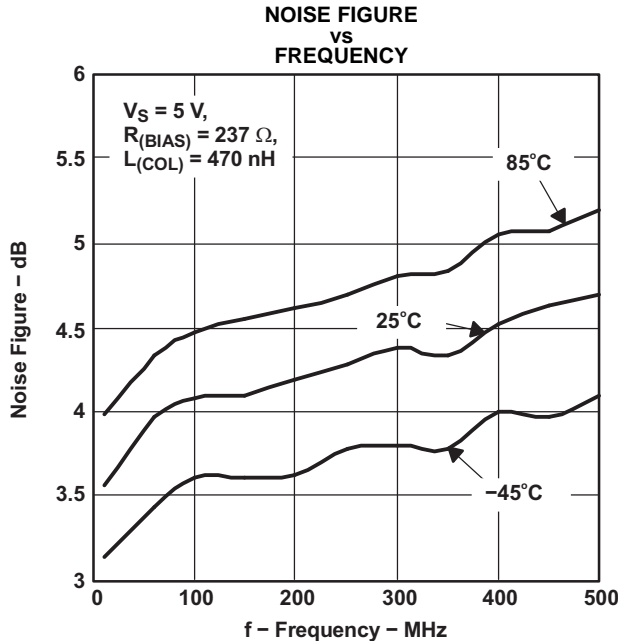


Figure 15.

TYPICAL CHARACTERISTICS (continued)

THS9000 as mounted on the EVM with $V_S = 3\text{ V}$ and 5 V , $R_{(\text{BIAS})} = 237\ \Omega$, and $L_{(\text{COL})} = 470\text{ nH}$ at -40°C , 25°C , and 85°C .



TYPICAL CHARACTERISTICS

Table 1. S-Parameters Tables of THS9001 with EVM De-Embedded

$V_S = 5\text{ V}$, $R_{(\text{BIAS})} = 237$, $L_{(\text{COL})} = 470\text{ nH}$								
Frequency (MHz)	S21		S11		S22		S12	
	Gain (dB)	Phase (deg)	Gain (dB)	Phase (deg)	Gain (dB)	Phase (deg)	Gain (dB)	Phase (deg)
1.0	-3.5	-165.0	-2.3	-1.1	-2.6	174.8	-64.4	-121.7
5.0	11.7	-127.1	-1.5	-14.9	-2.8	140.4	-32.4	123.0
10.2	15.8	-150.1	-2.2	-42.3	-5.3	99.8	-23.6	79.5
19.7	16.3	-170.8	-6.6	-69.3	-10.7	64.5	-21.1	40.7
50.1	15.9	175.7	-16.2	-90.3	-16.2	33.9	-20.6	14.5
69.7	15.8	171.5	-21.1	-95.4	-16.9	26.4	-20.6	9.4
102.4	15.7	165.7	-32.3	-86.5	-17.1	19.9	-20.6	5.3
150.5	15.6	158.2	-28.0	45.9	-16.8	14.7	-20.7	2.1
198.1	15.5	151.1	-21.9	46.8	-16.2	10.8	-20.7	0.1
246.9	15.3	144.1	-18.9	37.2	-15.3	6.0	-20.7	-1.4
307.6	15.2	135.3	-16.0	27.8	-14.2	-1.8	-20.6	-3.9
362.8	15.0	127.8	-14.2	17.4	-13.3	-9.2	-20.6	-5.9
405.0	14.9	121.9	-12.8	10.9	-12.6	-16.0	-20.6	-8.2
452.2	14.7	115.4	-11.6	3.0	-11.8	-23.9	-20.6	-10.8
504.7	14.5	108.4	-10.3	-6.0	-10.9	-33.0	-20.7	-14.2
563.4	14.4	100.3	-8.9	-17.4	-9.8	-45.2	-20.9	-19.3
595.3	14.2	96.0	-8.2	-23.3	-9.2	-52.2	-21.0	-22.6
664.5	14.1	87.0	-6.7	-36.9	-8.0	-68.3	-21.7	-30.5
702.1	14.0	80.9	-5.9	-44.6	-7.3	-79.1	-22.5	-38.6
741.8	13.9	76.5	-5.1	-54.0	-6.8	-91.4	-24.0	-44.9
828.1	13.5	62.2	-4.3	-76.1	-6.3	-113.2	-26.5	-35.0
874.9	13.0	54.0	-4.1	-84.6	-5.9	-126.0	-27.0	-49.0
924.4	12.8	44.9	-3.6	-93.1	-5.1	-136.8	-28.0	-62.9
976.7	11.6	35.9	-3.5	-104.4	-5.3	-157.8	-34.0	-104.4
1031.9	11.1	33.0	-3.4	-115.7	-5.8	-172.3	-37.1	107.9
1090.3	10.4	29.2	-3.3	-122.0	-5.7	-173.4	-37.8	162.5
1151.9	10.3	22.2	-3.0	-131.3	-4.8	179.4	-31.1	169.5
1217.1	9.7	4.7	-2.9	-142.3	-3.9	161.9	-26.3	137.1
1285.9	8.6	0.7	-2.9	-151.7	-3.6	147.6	-22.7	121.9
1358.6	7.3	-8.3	-2.9	-161.2	-3.4	134.6	-20.6	116.5
1435.5	5.8	-14.5	-3.0	-170.1	-3.2	122.6	-18.8	105.2
1516.6	4.6	-22.7	-3.1	-178.6	-3.2	112.1	-17.2	96.0
1602.4	3.2	-28.4	-3.1	173.2	-3.1	101.7	-15.7	87.0
1693.0	1.5	-38.0	-3.1	165.1	-3.0	92.4	-14.3	79.2
1788.8	-0.5	-47.9	-3.1	157.6	-2.9	83.6	-13.1	68.8
1889.9	-2.5	-51.0	-3.2	148.8	-2.7	74.4	-12.4	56.9
1996.8	-4.1	-49.0	-3.4	139.5	-2.3	65.0	-12.2	48.2

APPLICATION INFORMATION

The THS9001 is a medium power, cascadeable, amplifier optimized for high intermediate frequencies in radios. The amplifier is unconditionally stable and the design requires only 2 dc-blocking capacitors, 1 power-supply bypass capacitor, 1 RF choke, and 1 bias resistor. Refer to [Figure 25](#) for the circuit diagram.

The THS901 operates with a power-supply voltage ranging from 2.5 V to 5.5 V.

The value of $R_{(BIAS)}$ sets the bias current to the amplifier. Refer to [Figure 14](#). This allows the designer to trade-off linearity versus power consumption. $R_{(BIAS)}$ can be removed without damage to the device.

Component selection of $C_{(BYP)}$, C_{IN} , and C_{OUT} is not critical. The values shown in [Figure 25](#) were used for all the data shown in this data sheet.

The amplifier incorporates internal impedance matching to 50 Ω that can be adjusted for various frequencies of operation by proper selection of $L_{(COL)}$.

[Figure 20](#) shows the s-parameters of the part mounted on the standard EVM with $V_S = 5$ V, $R_{(BIAS)} = 237$ Ω , and $L_{(COL)} = 470$ nH. With this configuration, the part is very broadband, and achieves greater than 15-dB input and output return loss from 50 MHz to 325 MHz.

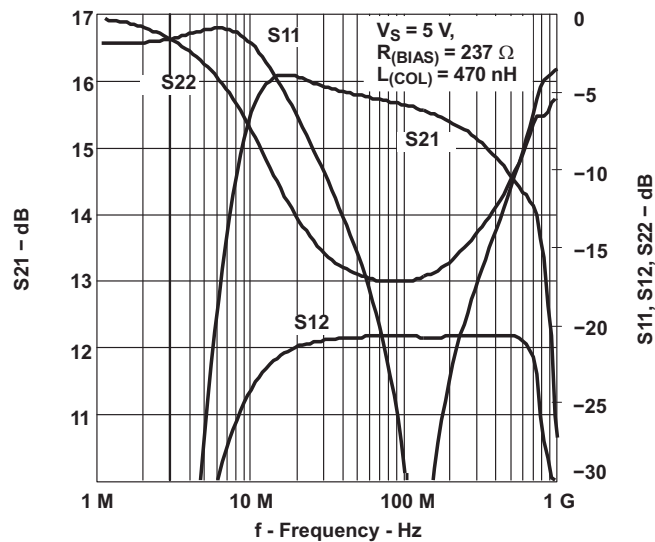


Figure 20. S-Parameters of THS9001 Mounted on the Standard EVM with $V_S = 5$ V, $R_{(BIAS)} = 237$ Ω , and $L_{(COL)} = 470$ nH

Figure 21 shows an example of a single conversion receiver architecture and where the THS9001 would typically be used.

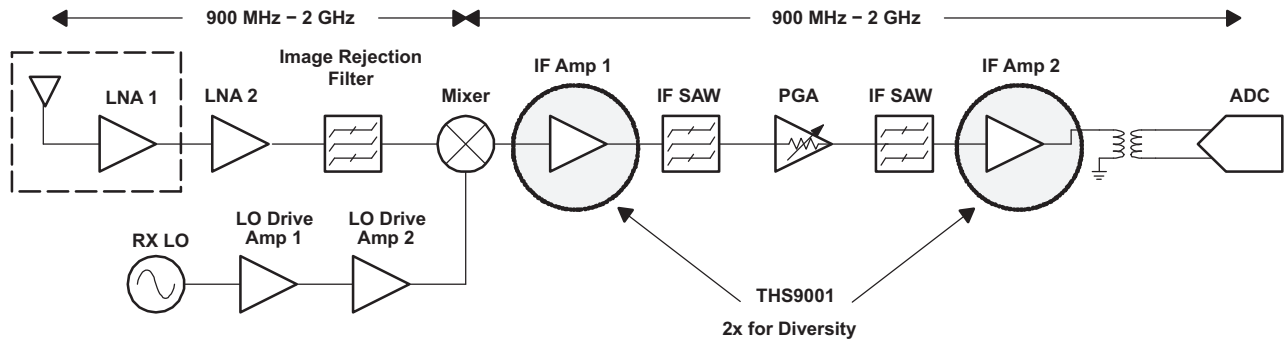


Figure 21. Example Single Conversion Receiver Architecture

Figure 22 shows an example of a dual conversion receiver architecture and where the THS9001 would typically be used.

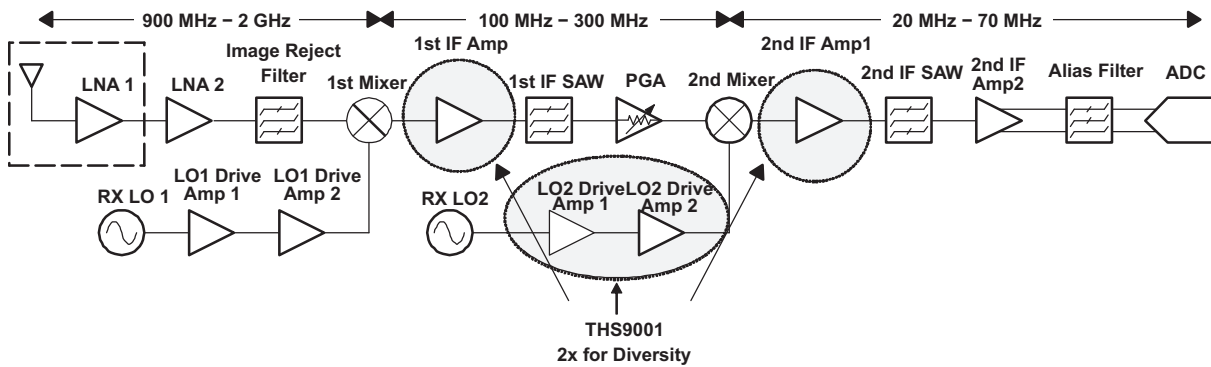


Figure 22. Example Dual Conversion Receiver Architecture

Figure 23 shows an example of a dual conversion transmitter architecture and where the THS9001 would typically be used.

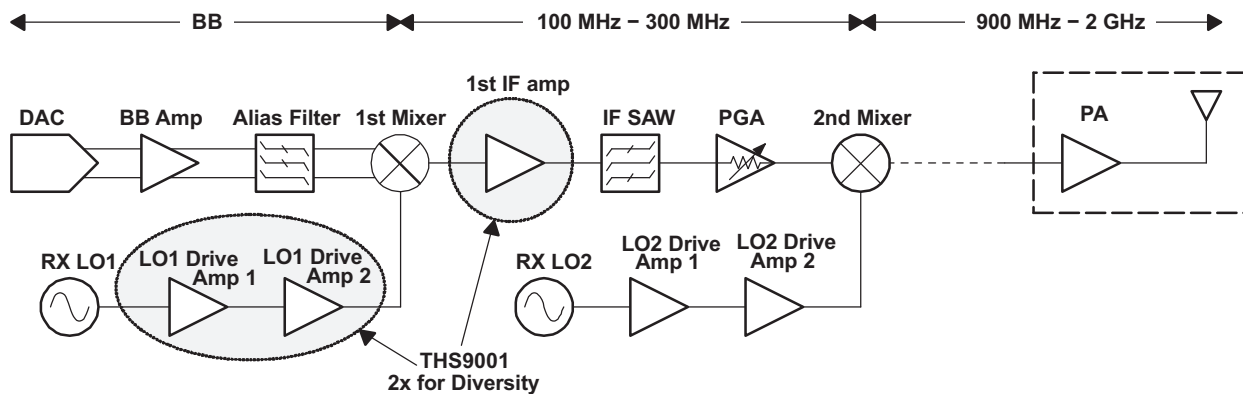
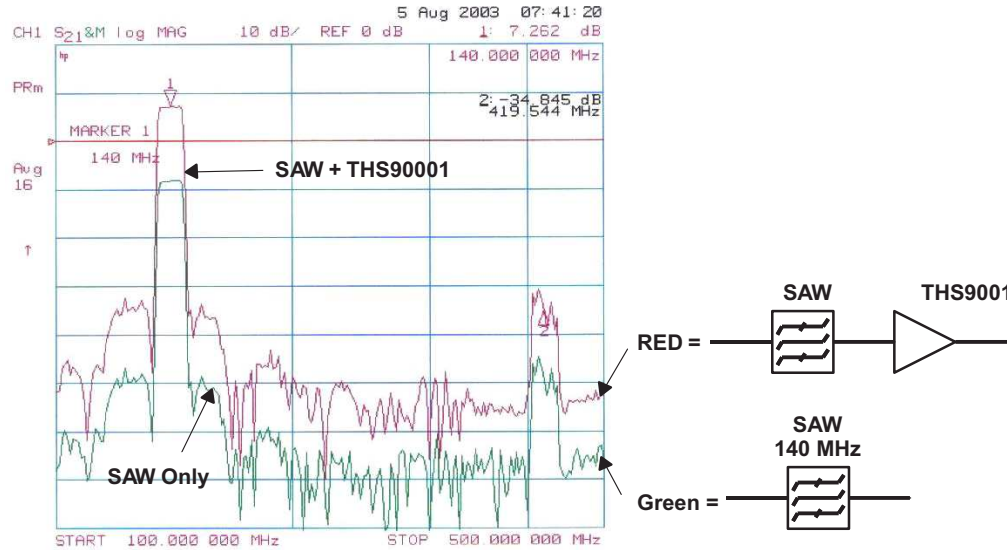


Figure 23. Example Dual Conversion Transmitter Architecture

Figure 24 shows the THS9001 and Sawtek #854916 SAW filter frequency response along with the frequency response of the SAW filter alone. The SAW filter has a center frequency of 140 MHz with 10-MHz bandwidth and 8-dB insertion loss. It can be seen that the frequency response with the THS9001 is the same as with the SAW except for a 15-dB gain. The THS9001 is mounted on the standard EVM with $V_S = 5\text{ V}$, $R_{(BIAS)} = 237\ \Omega$, and $L_{(COL)} = 470\text{ nH}$. Note the amplifier does not add artifacts to the signal.



140 MHz SAW: Sawtek #854916

Figure 24. Frequency Response of the THS9000 and SAW Filter, and SAW Filter Only

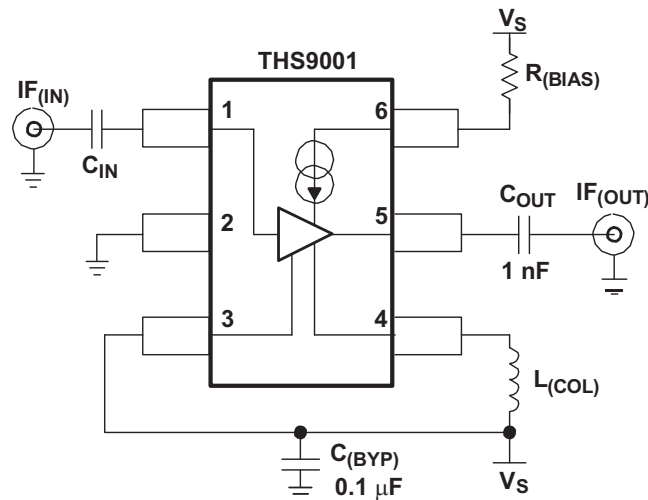


Figure 25. THS9000 Recommended Circuit (used for all tests)

Evaluation Module

[Bill Of Materials](#) is the bill of materials, and [Figure 26](#) and [Figure 27](#) show the EVM layout.

Bill Of Materials

ITEM	DESCRIPTION	REF DES	QTY	PART NUMBER ⁽¹⁾
1	Cap, 0.1 μ F, ceramic, X7R, 50 V	C1	1	(AVX) 08055C104KAT2A
2	Cap, 1000 pF, ceramic, NPO, 100 V	C2, C3	2	(AVX) 08051A102JAT2A
3	Inductor, 470 nH, 5%	L1	1	(Coilcraft) 0805CS-471XJBC
4	Resistor, 237 Ω , 1/8 W, 1%	R1	1	(Phycomp) 9C08052A2370FKHFT
5	Open	TR1	1	
6	Jack, banana receptance, 0.25" dia.	J3, J4	2	(SPC) 813
7	Connector, edge, SMA PCB jack	J1, J2	2	(Johnson) 142-0701-801
8	Standoff, 4-40 Hex, 0.625" Length		4	(KEYSTONE) 1808
9	Screw, Phillips, 4-40, .250"		4	SHR-0440-016-SN
10	IC, THS90001	U1	1	(TI) THS9001DBV
11	Board, printed-circuit		1	(TI) EDGE # 6453522 Rev.A

(1) The manufacturer's part numbers are used for test purposes only.

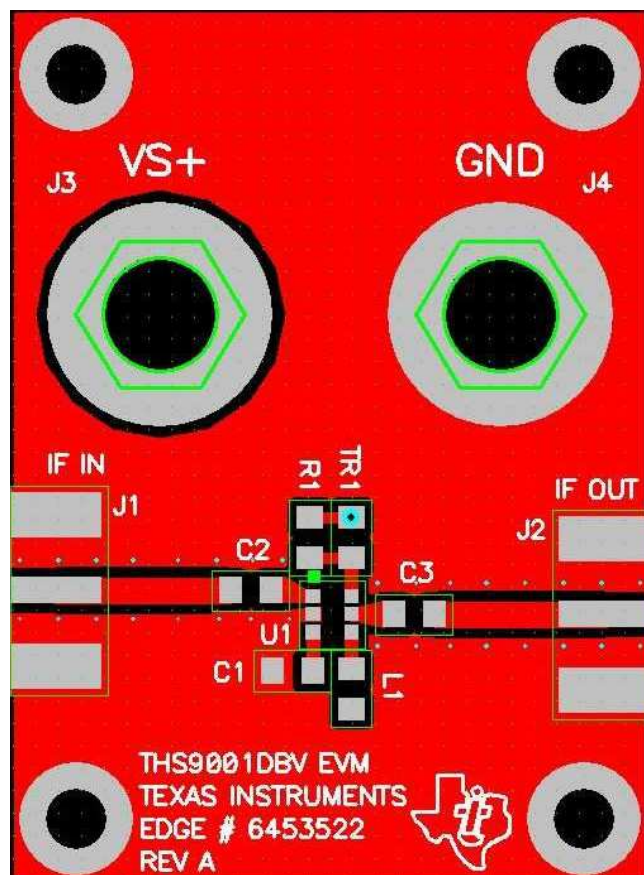


Figure 26. EVM Top Layout

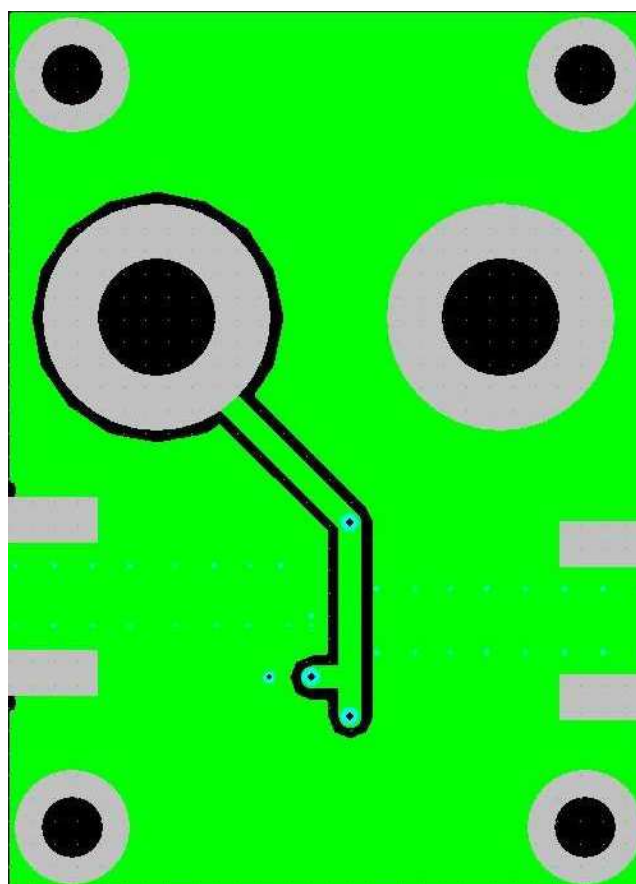


Figure 27. EVM Bottom Layout

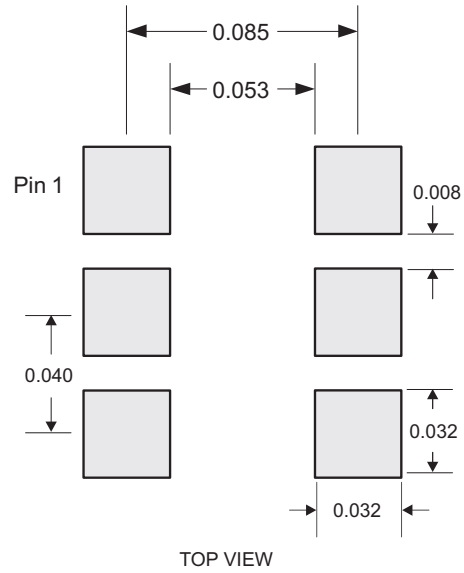


Figure 28. THS9000 Recommended Footprint dimensions are in inches (millimeters)

REVISION HISTORY

Changes from Revision B (January 2007) to Revision C	Page
<ul style="list-style-type: none">Changed the data sheet title From: 50 MHz to 400 MHz CASCADEABLE AMPLIFIER To: 50 MHz to 750 MHz CASCADEABLE AMPLIFIER	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS9001DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWL	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS9001DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS9001DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0

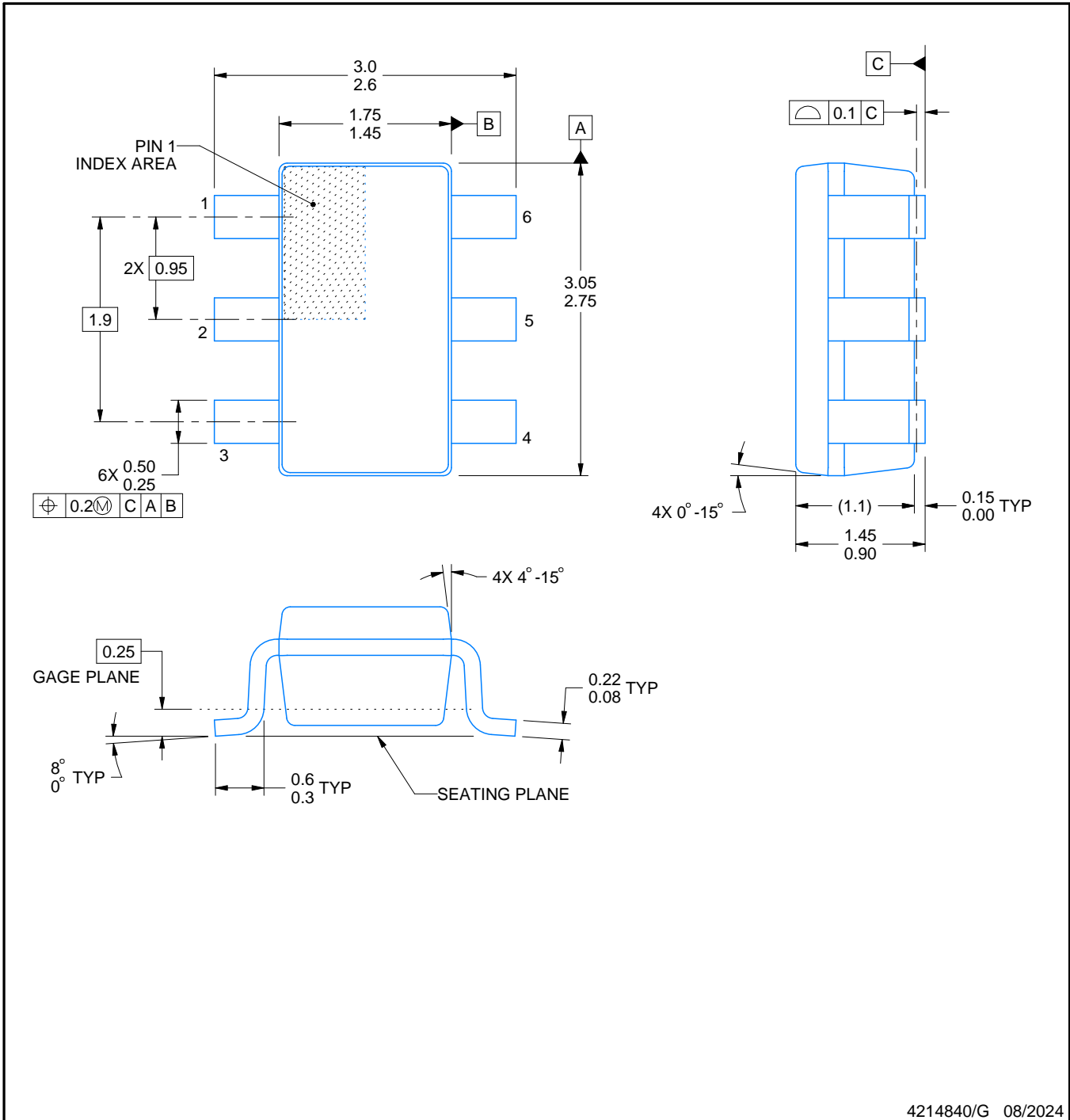


DBV0006A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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