TEXAS INSTRUMENTS

Universal Operational Amplifier Single, Dual, Quad (MSOP/TSSOP) Evaluation Module With Shutdown

User's Guide

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Mixed-Signal Products

SLOU055

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Preface

Related Documentation From Texas Instruments

- ***Amplifiers, Comparators, and Special Functions Data Book*** (literature number SLYD011 and SLYD012). This data book contains data sheets and other information on the TI operational amplifiers that can be used with this evaluation module.

- ***Operational Amplifier Supplement Data Book*** (literature number SLOD002). This data book contains data sheets and other information on the TI operational amplifiers that can be used with this evaluation module.

- ***Power Management Products Data Book*** (literature numbers SLVD003, SLVD004, and SLVD005). This data book contains data sheets and other information on the TI shunt regulators that can be used with this evaluation module.

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Chapter 1

Introduction

This user's guide describes the universal operational amplifier single, dual, quad (MSOP/TSSOP) evaluation module (EVM) with shutdown (SLOP247). The EVM simplifies evaluation of Texas Instruments surface-mount op amps with or without shutdown feature.

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1.1 Design Features

The EVM board design allows many circuits to be constructed easily and quickly. There are three circuit development areas on the board. Area 100 is for a single operational amplifier (op amp), with or without shutdown. It also features offset nulling pin pads and can use the MSOP PowerPAD package. Area 200 is for a dual op amp, with shutdown. Like area 100, it uses the MSOP PowerPAD package. Area 300 is for a quad op amp, with or without shutdown, and is designed for the TSSOP PowerPAD package. Although all three areas are designed for PowerPAD devices, non-PowerPAD packages will work on the EVM PCB as well. A few possible circuits include:

- Voltage follower
- Noninverting amplifier
- Inverting amplifier
- Simple or algebraic summing amplifier
- Difference amplifier
- Current to voltage converter
- Voltage to current converter
- Integrator/low-pass filter
- Differentiator/high-pass filter
- Instrumentation amplifier
- Sallen-Key filter

The EVM PCB is of two-layer construction, with a ground plane on the solder side. Circuit performance should be comparable to final production designs.

1.2 Power Requirements

The devices and designs that are used dictate the input power requirements. Three input terminals are provided for each area of the board:

Vx+	Positive input power for area x00	i.e., V1+ ⇒ area 100
GNDx	Ground reference for area x00	i.e., GND2 ⇒ area 200
Vx–	Negative input power for area x00	i.e., V3– ⇒ area 300

Each area has four bypass capacitors – two for the positive supply, and two for the negative supply. Each supply should have a 1-µF to 10-µF capacitor for low frequency bypassing and a 0.01-µF to 0.1-µF capacitor for high frequency bypassing.

When using single-supply circuits, the negative supply is shorted to ground by bridging C104 or C105 in area 100, C209 or C210 in area 200, or C311 or C312 in area 300. Power input is between Vx+ and GNDx. The voltage reference circuitry is provided for single-supply applications that require a reference voltage to be generated.

Chapter 2

Evaluation Module Layout

This chapter shows the universal operational amplifier single, dual, quad (MSOP/TSSOP) evaluation module (EVM) with shutdown board layout, schematics of each area, and describes the relationships between the three areas.

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2.1 Physical Considerations

The EVM board has three circuit development areas. Each area can be separated from the others by breaking along the score lines. The circuit layout in each area supports an op amp package, voltage reference, and ancillary devices. The op amp package is unique to each area as described in the following paragraphs. The voltage reference and supporting devices are the same for all areas. Surface-mount or through-hole components can be used for all capacitors and resistors on the board.

The voltage reference can be either surface-mount or through-hole. If surface mount is desired, the TLV431ACDBV5 or TLV431AIDBV5 adjustable shunt regulators can be used. If through hole is desired, the TLV431ACLP, TLV431AILP, TL431CLP, TL431ACLP, TL431ILP or TL431AILP adjustable shunt regulators can be used. Refer to Texas Instruments' *Power Supply Circuits Data Book* (literature number SLVD002) for details on usage of these shunt regulators.

Each passive component (resistor or capacitor) has a surface-mount 1206 footprint with through holes at 0.2″ spacing on the outside of the 1206 pads. C105, C106, C107, C207, C208, C209, C312, C314, and C315 have a surface-mount 1210 footprint with through holes at 0.2″ spacing on the outside of the 1210 pads. Therefore, either surface-mount or through-hole parts can be used. The potentiometer for the offset nulling feature in area 100 can also be either a surface-mount or a through-hole unit.

Figures 2–1 through 2–3 show schematics for each of the board areas. The schematics show all components that the board layout can accommodate. These should only be used as reference, since not all components will be used at any one time.

2.2 Area 100—Single Device MSOP

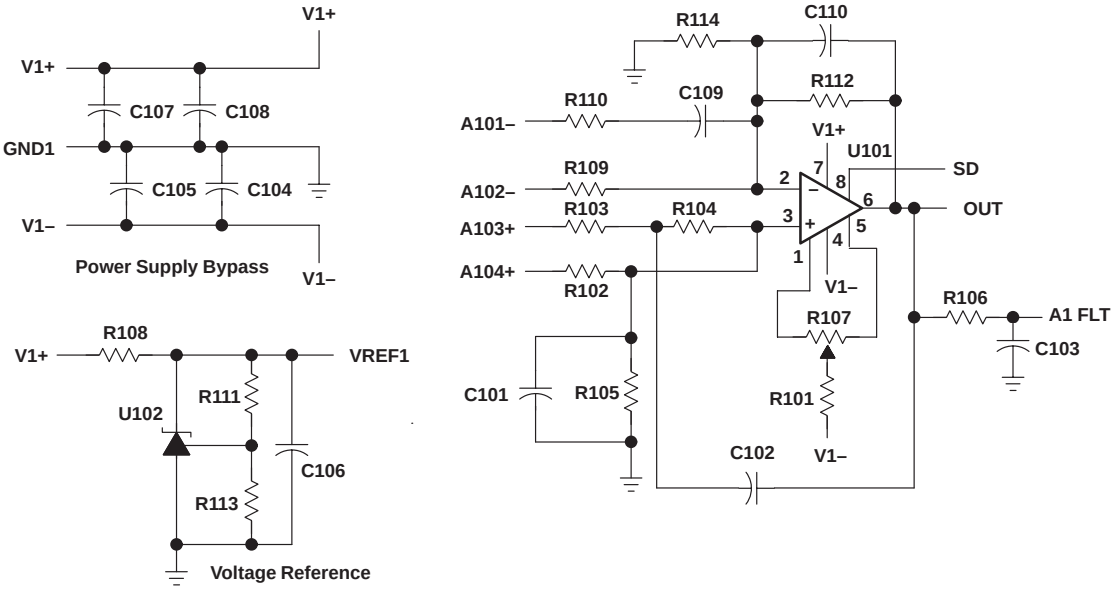
Area 100 uses 1xx reference designators, and is compatible with a single op amp, with or without shutdown, packaged as an 8-pin MSOP, with or without PowerPAD. This surface-mount package is designated by a DGK (non-PowerPAD) and DGN (PowerPAD) suffix in TI part numbers, as in TxxxxCDGK, TxxxxIDGN, etc.

Offset nulling can be extremely important in some applications. The EVM accommodates TI IC op amps that provide this feature. The input offset can be adjusted by connecting a 100 kΩ potentiometer between terminals 1 and 5 of the device and connecting the wiper to VCC– via a resistor (R101) as shown below. This resistor is used to fine tune the offset adjustment. For example, when using the TLC070 or TLC071 device and a 100 kΩ nulling potentiometer, the offset voltage adjustment is ±10 mV when R101 is 5.6 kΩ and ±3 mV when R101 is 20 kΩ.

When using the non-shutdown version of the device, pin 8 of the IC is a no connect.

Figure 2–1 shows the area 100 schematic.

Figure 2–1. Area 100 Schematic—Single Device, MSOP (8 pin)

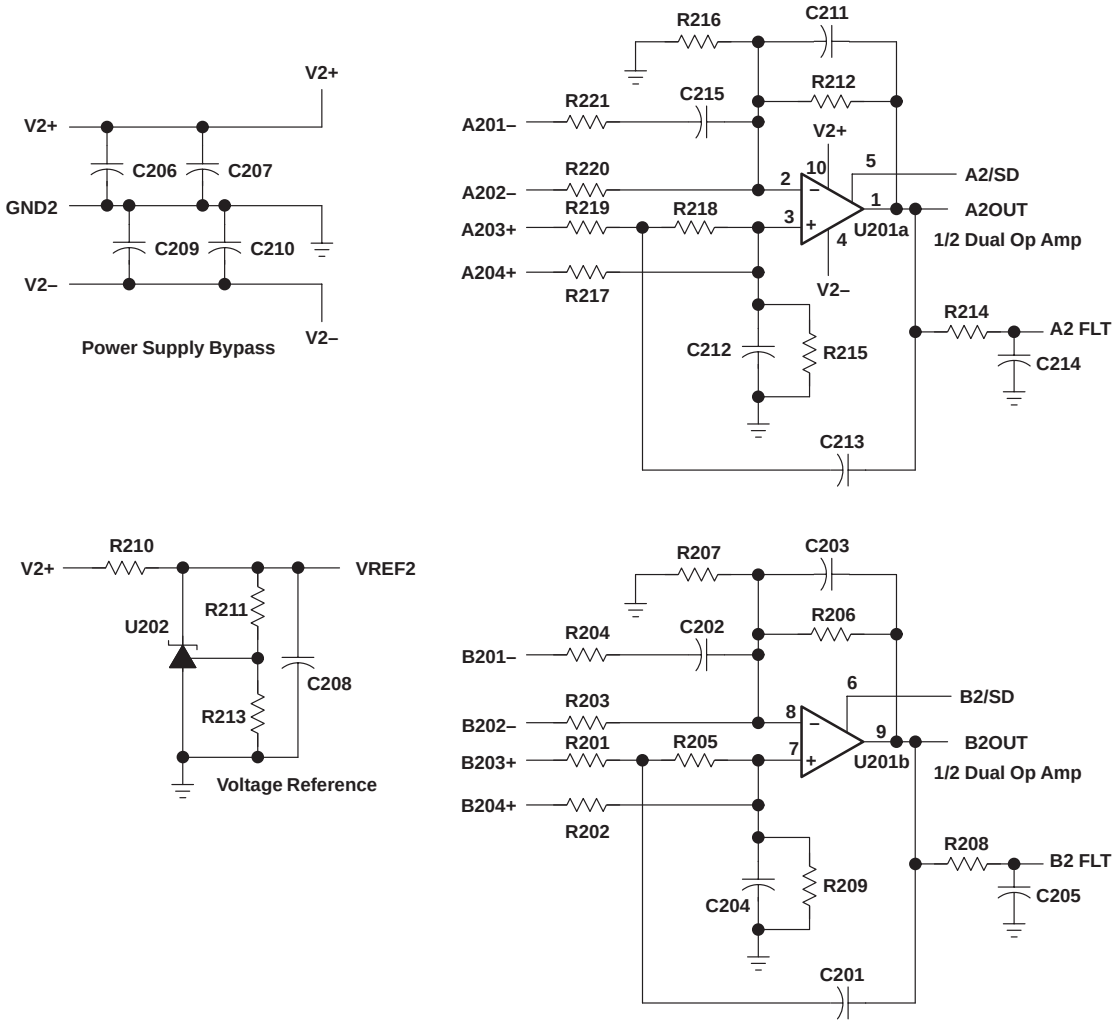


2.3 Area 200—Dual Device MSOP PowerPAD

Area 200 uses 2xx reference designators, and is compatible with dual op amps, with shutdown, packaged as a 10-pin MSOP PowerPAD. This package is designated by a DGS (non-PowerPAD), and DGQ (PowerPAD) suffix in TI part numbers, as in TxxxxCDGQ. When using a PowerPAD device, the PowerPAD on the bottom of the package must be soldered to the PCB. If the appropriate equipment for soldering the PowerPAD to the PCB is not available, thermal grease can be used to improve the heat transfer into the PCB.

Figure 2–2 shows the area 200 schematic.

Figure 2–2. Area 200 Schematic—Dual Device, MSOP PowerPAD (10 pin)



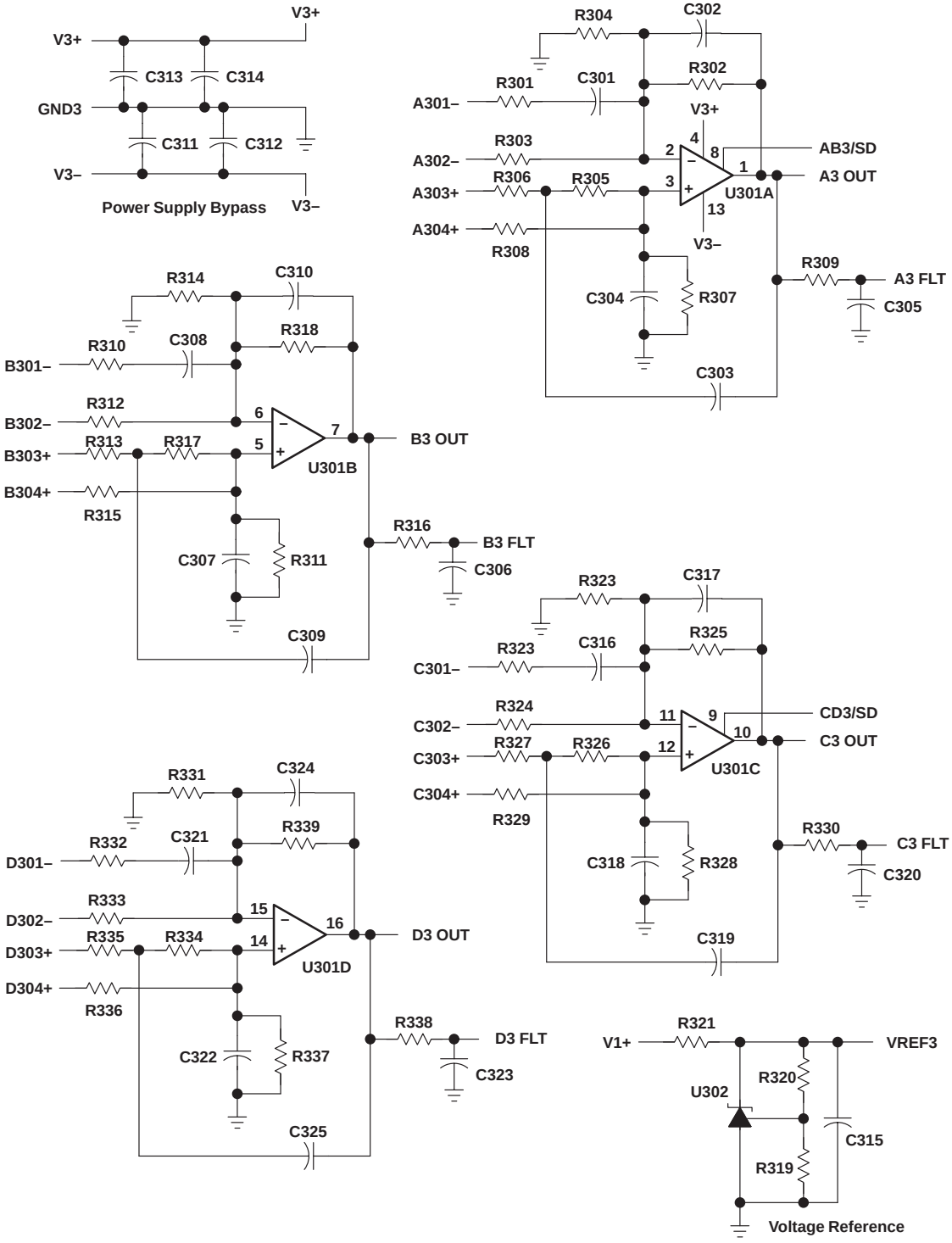
2.4 Area 300—Quad Device TSSOP PowerPAD

Area 300 uses 3xx reference designators, and is compatible with quad op amps, with or without shutdown, packaged in a 16-pin TSSOP PowerPAD. This surface-mount package is designated by a PW (non-PowerPAD) or a PWP (PowerPAD) suffix in TI part numbers, as in TxxxxIPWP. When using a PowerPAD device, the PowerPAD on the bottom of the package must be soldered to the PCB. If the appropriate equipment for soldering the PowerPAD to the PCB is not available, thermal grease can be used to improve the heat transfer into the PCB.

When using the non-shutdown version of the device, ensure that the IC is aligned at the top of the IC pad array—the last two PCB pads will be unused.

Figure 2–3 shows the area 300 schematic.

Figure 2–3. Area 300 Schematic—Quad Device TSSOP PowerPAD (16 pin)



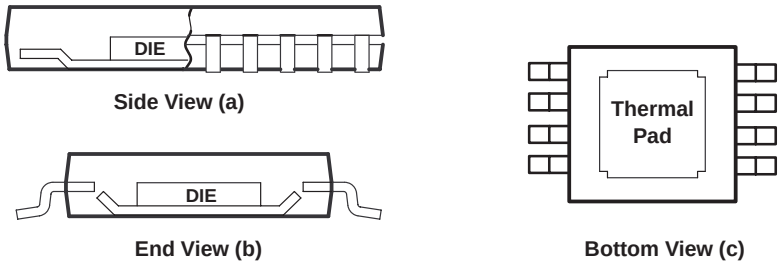
2.5 General PowerPAD Design Considerations

The Texas Instruments thermally-enhanced DGN, DGQ, and PWP packages, which are members of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 2–4(a) and Figure 2–4(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 2–4(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

Figure 2–4. Views of Thermally Enhanced DGN Package

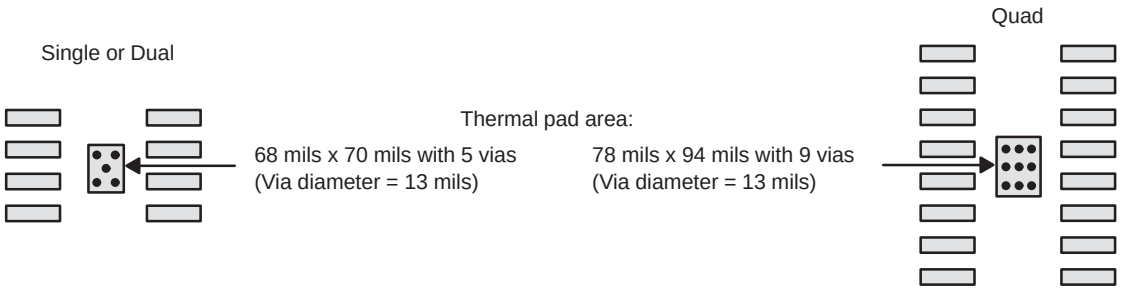


NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

1) Prepare the PCB with a top side etch pattern as shown in Figure 2–5. There should be etch for the leads as well as etch for the thermal pad.

Figure 2–5. PowerPAD PCB Etch and Via Pattern



2) Place five holes (single or dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.

3) Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.

4) Connect all holes to the internal ground plane.

5) When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the device package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

6) The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.

7) Apply solder paste to the exposed thermal pad area and all of the IC terminals.

8) With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

Correct PCB layout and manufacturing techniques are critical for achieving adequate transfer of heat away from the PowerPAD IC package. For more general information on the PowerPAD package and its thermal characteristics, see the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package* (SLMA002).

2.6 General Power Dissipation Considerations

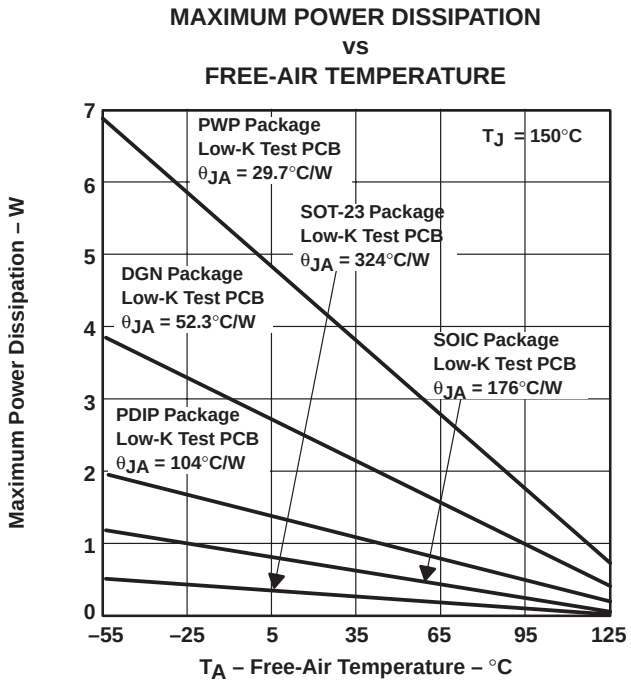
For a given θ_{JA}, the maximum power dissipation is shown in Figure 2–6 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of Txxxx IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

Figure 2–6. Maximum Power Dissipation vs Free-Air Temperature



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

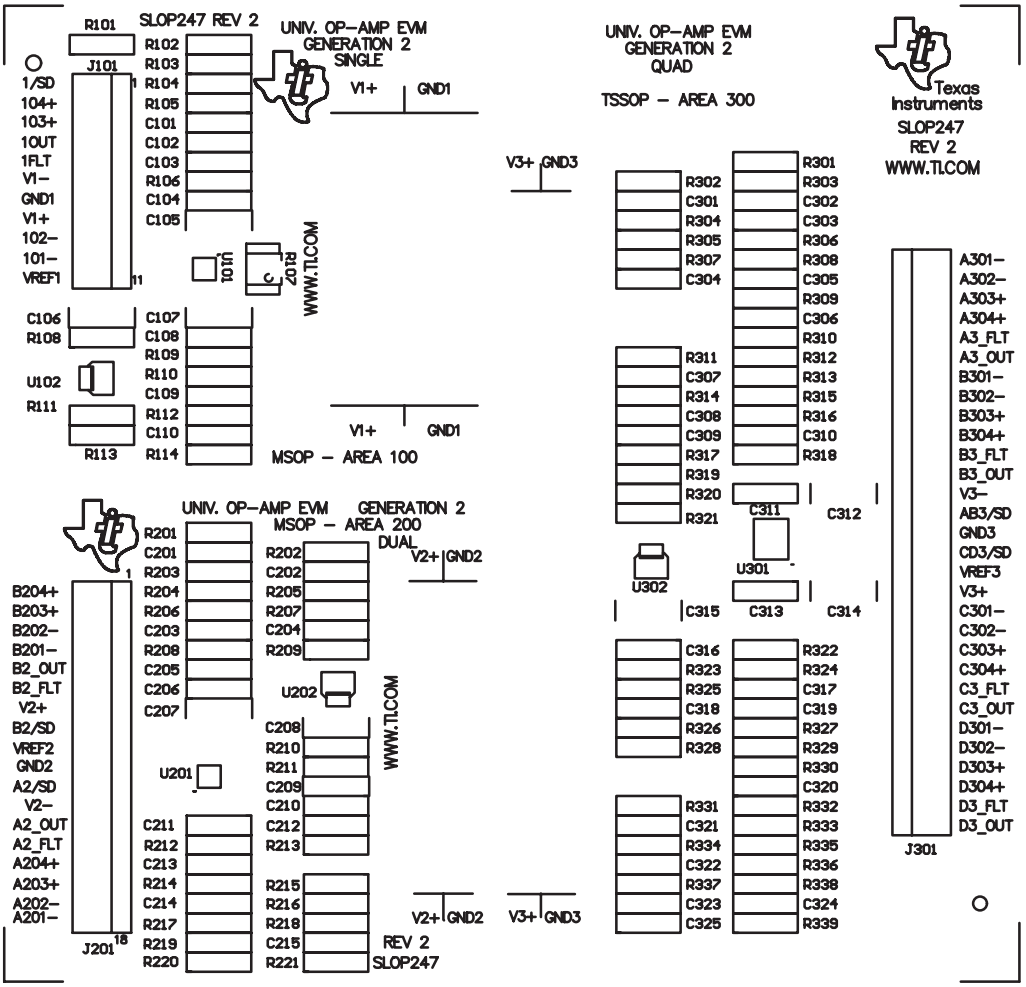
Table 2–1. Dissipation Rating Table

PACKAGE	PowerPAD	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING
DGK (8)		54.23	259.96	424 mW
DGN (8)	YES	4.7	52.7	2.37 W
DGS (10)		54.1	257.71	424 mW
DGQ (10)	YES	4.7	52.3	2.39 W
PW (16)		28.7	161.4	700 mW
PWP (16)	YES	2.07	29.7	4.21 W

2.7 EVM Component Placement

Figure 2–7 shows component placement for the EVM board.

Figure 2–7. EVM Component Placement



2.8 EVM Board Layout

Figures 2–8 and 2–9 show the EVM top and bottom board layouts, respectively.

Figure 2–8. EVM Board Layout—Top

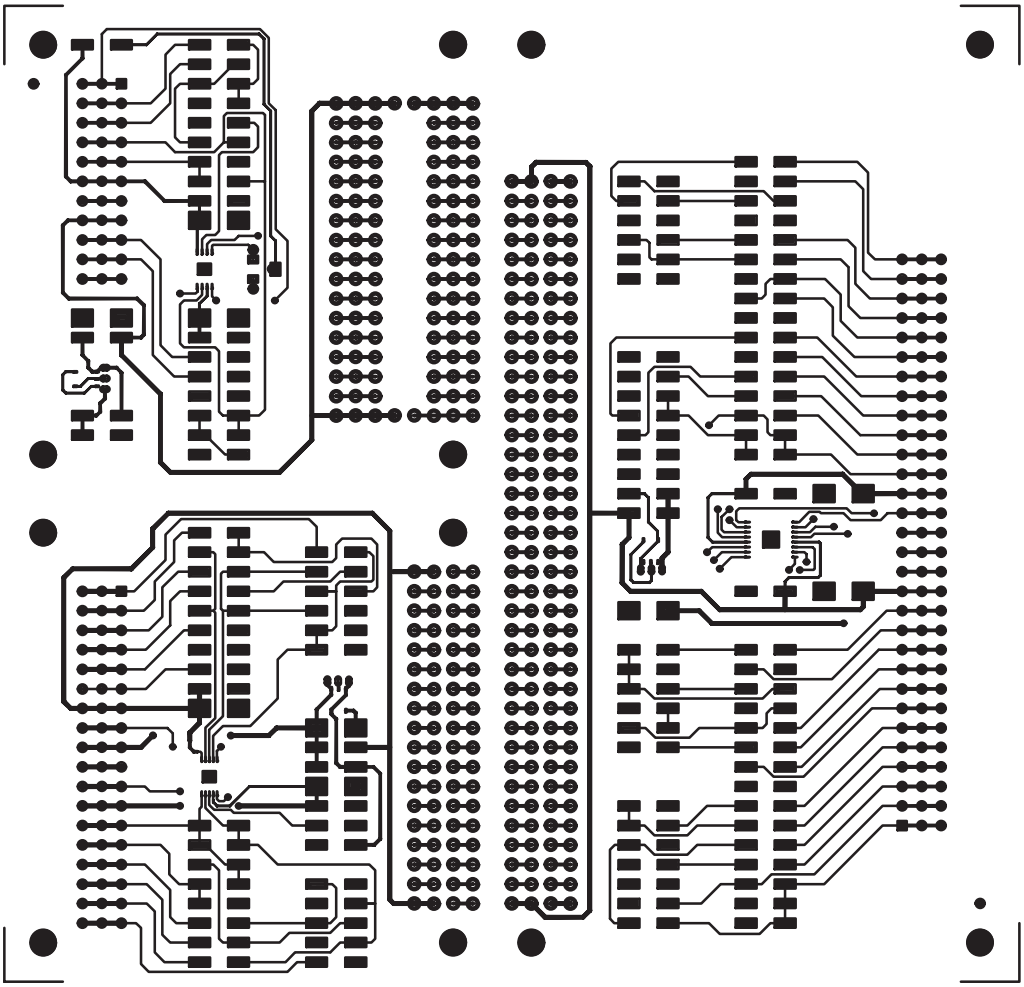
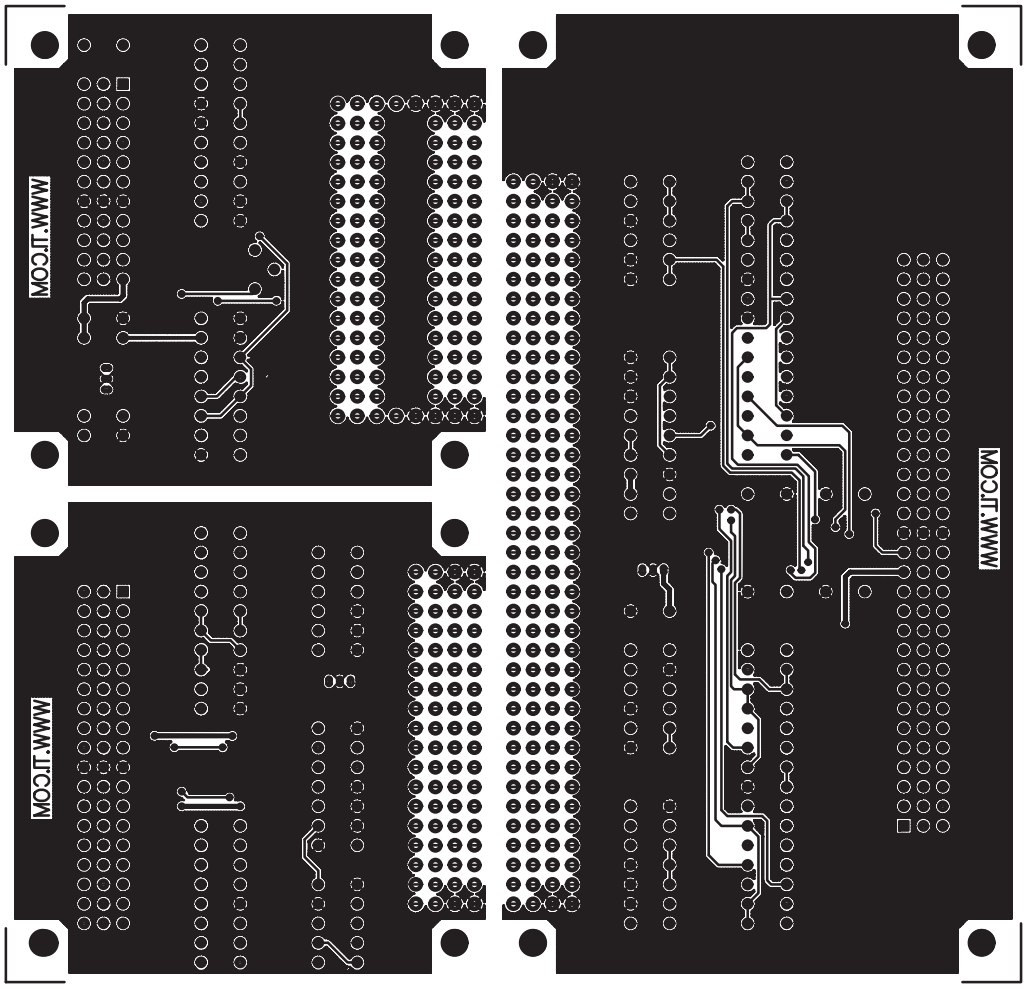


Figure 2–9. EVM Board Layout—Bottom



Chapter 3

Example Circuits

This chapter shows and discusses several example circuits that can be constructed using the universal operational amplifier EVM. The circuits are all classic designs that can be found in most operational amplifier design books.

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3.1 Schematic Conventions

Figures 3–1 through 3–6 show schematic examples of circuits that can be constructed using the universal operational amplifier EVM with shutdown. The components that are placed on the board are shown in bold. Unused components are blanked out. Jumpers and other changes are noted. These examples are only a few of the many circuits that can be built.

3.2 Inverting Amplifier

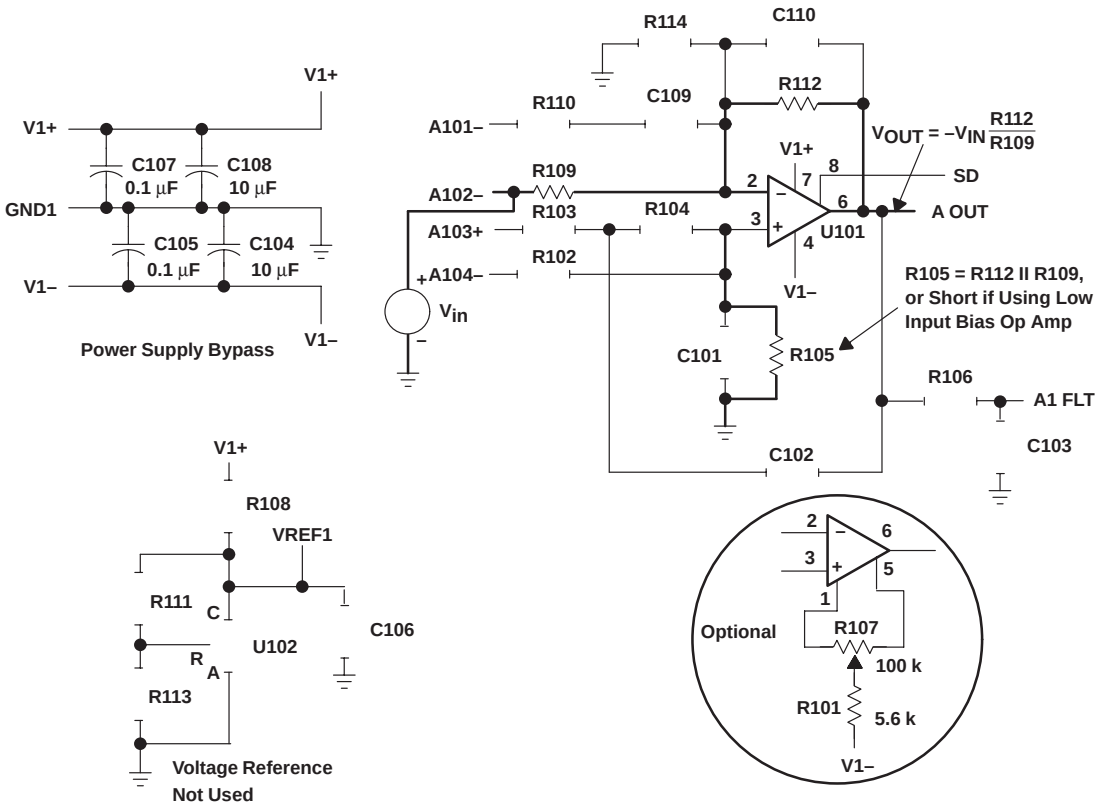
Figure 3–1 shows area 100 equipped with a single operational amplifier configured as an inverting amplifier using dual power supplies.

Basic setup is done by choice of input and feedback resistors. The transfer function for the circuit as shown is:

$$V_{OUT} = -V_{IN}\frac{R112}{R109}$$

To cancel the effects of input bias current, set R105 = R112 || R109, or use a 0-Ω jumper for R105 if the operational amplifier is a low input bias operational amplifier.

Figure 3–1. Inverting Amplifier With Dual Supply Using Area 100



3.3 Noninverting Amplifier

Figure 3–2 shows area 100 equipped with a single operational amplifier configured as a noninverting amplifier with single-supply power input.

Basic setup is done by choice of input and feedback resistors. The transfer function for the circuit as shown is:

$$V_{OUT} = V_{IN}\left(1 + \frac{R112}{R109}\right) + VREF1$$

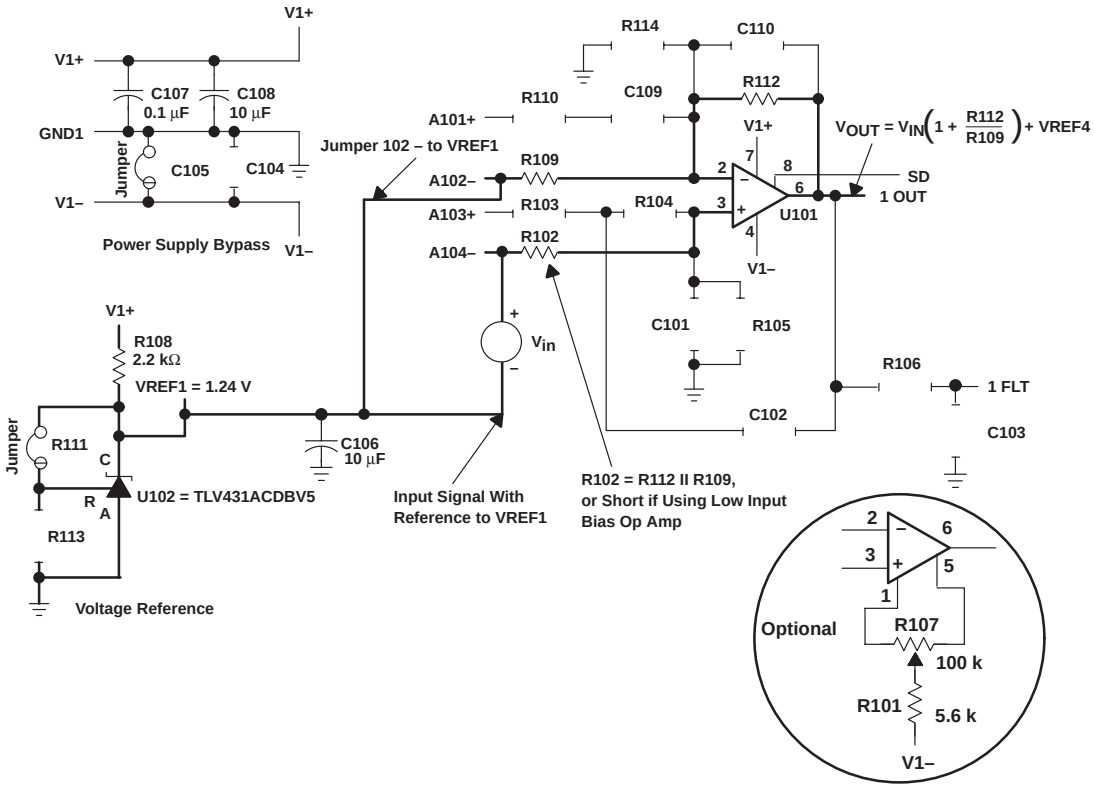
The input signal must be referenced to VREF1.

To cancel the effects of input bias current, set R102 = R112 || R109, or use a 0-Ω jumper for R102 if the operational amplifier is a low input bias operational amplifier.

The TL431 adjustable precision shunt regulator, configured as shown, provides a low impedance reference for the circuit at about 1/2 V1+ in a 3 V system. Another option is to adjust resistors R113 and R111 for the desired VREF1 voltage. The formula for calculating VREF1 is:

$$VREF1 = 1.24\ V\left(\frac{R111 + R113}{R113}\right)$$

Figure 3–2. Noninverting Amplifier With Single Supply Using Area 100



3.4 Differential Amplifier

Figure 3–3 shows area 100 equipped with a single operational amplifier configured as a differential amplifier using a voltage reference and single power supply.

Basic setup is done by choice of input and feedback resistors. The transfer function for the circuit as shown is:

$$V_{OUT} = V_{IN}\left(\frac{R112}{R109}\right) + VREF1$$

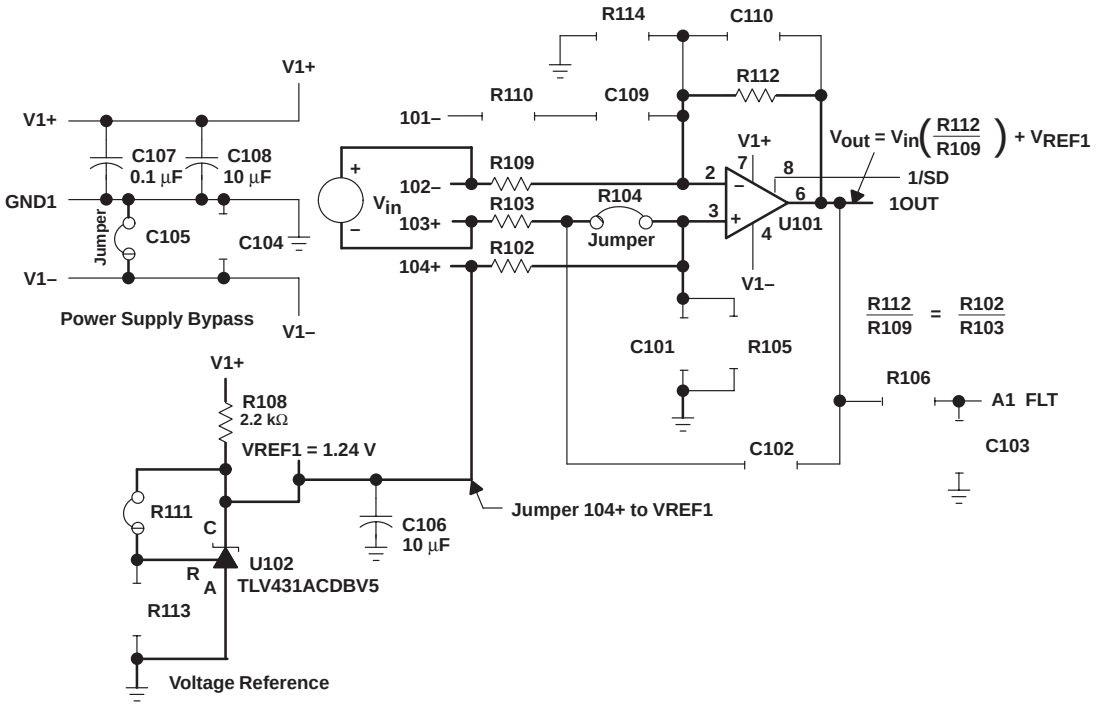
Where

$$\frac{R112}{R109} = \frac{R102}{R103}$$

The TLV431 adjustable precision shunt regulator, configured as shown, provides a low impedance reference for the circuit at about 1/2 V1+ in a 3-V system. Another option is to adjust resistors R111 and R113 for the desired VREF1 voltage. The formula for calculating VREF1 is:

$$VREF1 = 1.24\ V\left(\frac{R111 + R113}{R113}\right)$$

Figure 3–3. Single Operational Amplifier Differential Amplifier With Single Supply Using Area 100



3.5 Sallen-Key Low-Pass Filter

Figure 3–4 shows area 200 equipped with a dual operational amplifier configured as a second-order Sallen-Key low-pass filter using dual-power supplies.

Basic setup is done by proper choice of resistors R and mR and capacitors C and nC. The transfer function is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - \left(\frac{f}{f_o}\right)^2 + \left(\frac{j}{Q}\right)\left(\frac{f}{f_o}\right)}$$

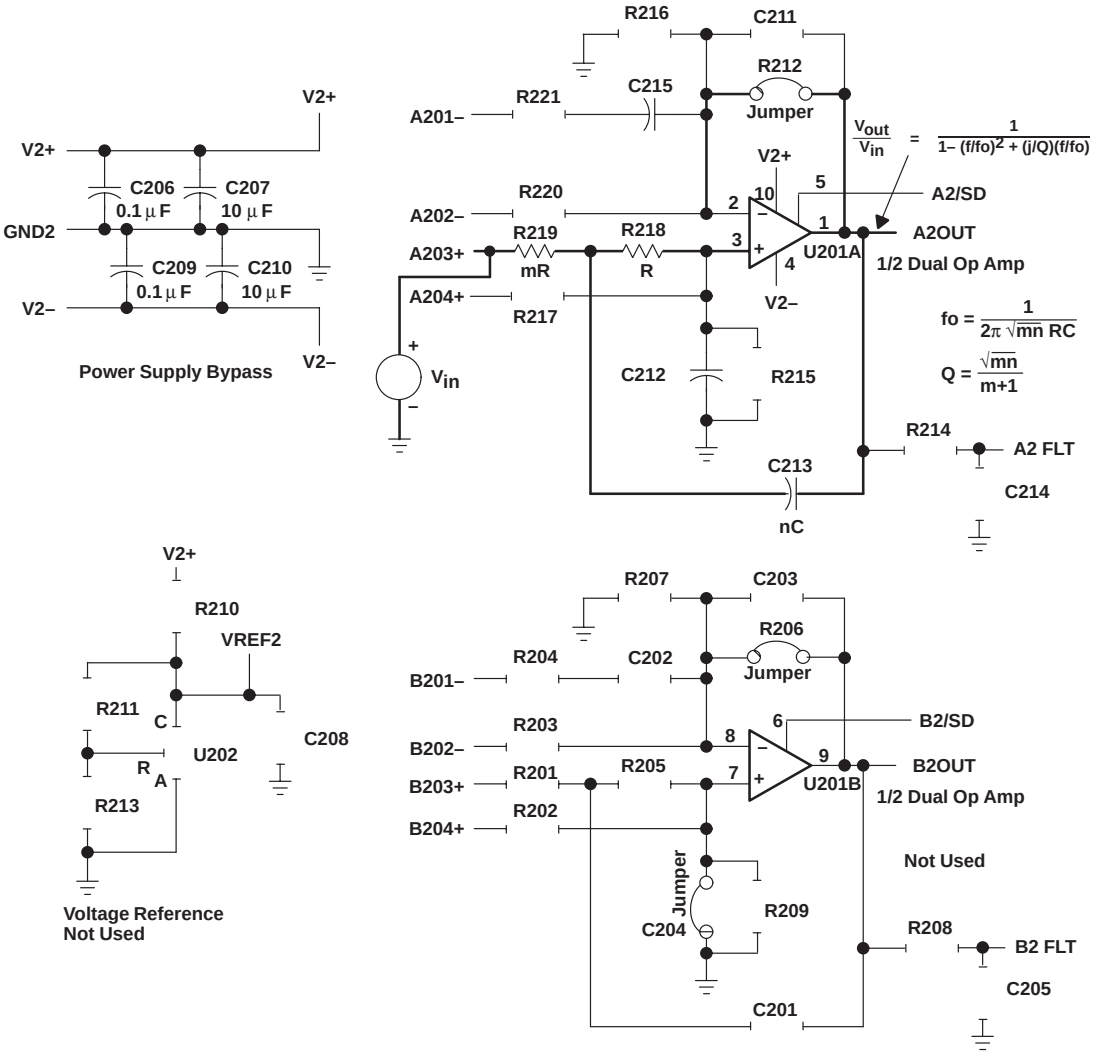
Where:

$$f_o = \frac{1}{2\pi\sqrt{m\ n}\,RC}$$

And

$$Q = \frac{\sqrt{m\ n}}{m + 1}$$

Figure 3–4. Sallen-Key Low-Pass Filter With Dual Supply Using Area 200



3.6 Sallen-Key High-Pass Filter

Figure 3–5 shows area 200 equipped with a dual operational amplifier configured as a second-order Sallen-Key high-pass filter using single-supply power input.

Basic setup is done by proper choice of resistors R and mR and capacitors C and nC. Note that capacitors should be used for components R201 and R205, and a resistor for C201. The transfer function for the circuit as shown is:

$$V_{OUT} = V_{IN} \times \left[\frac{-\left(\frac{f}{f_o}\right)^2}{1 + \left(\frac{j}{Q}\right)\left(\frac{f}{f_o}\right) - \left(\frac{f}{f_o}\right)^2} \right] + \text{VREF2}$$

Where:

$$f_o = \frac{1}{2\pi \sqrt{m\ n}\,RC}$$

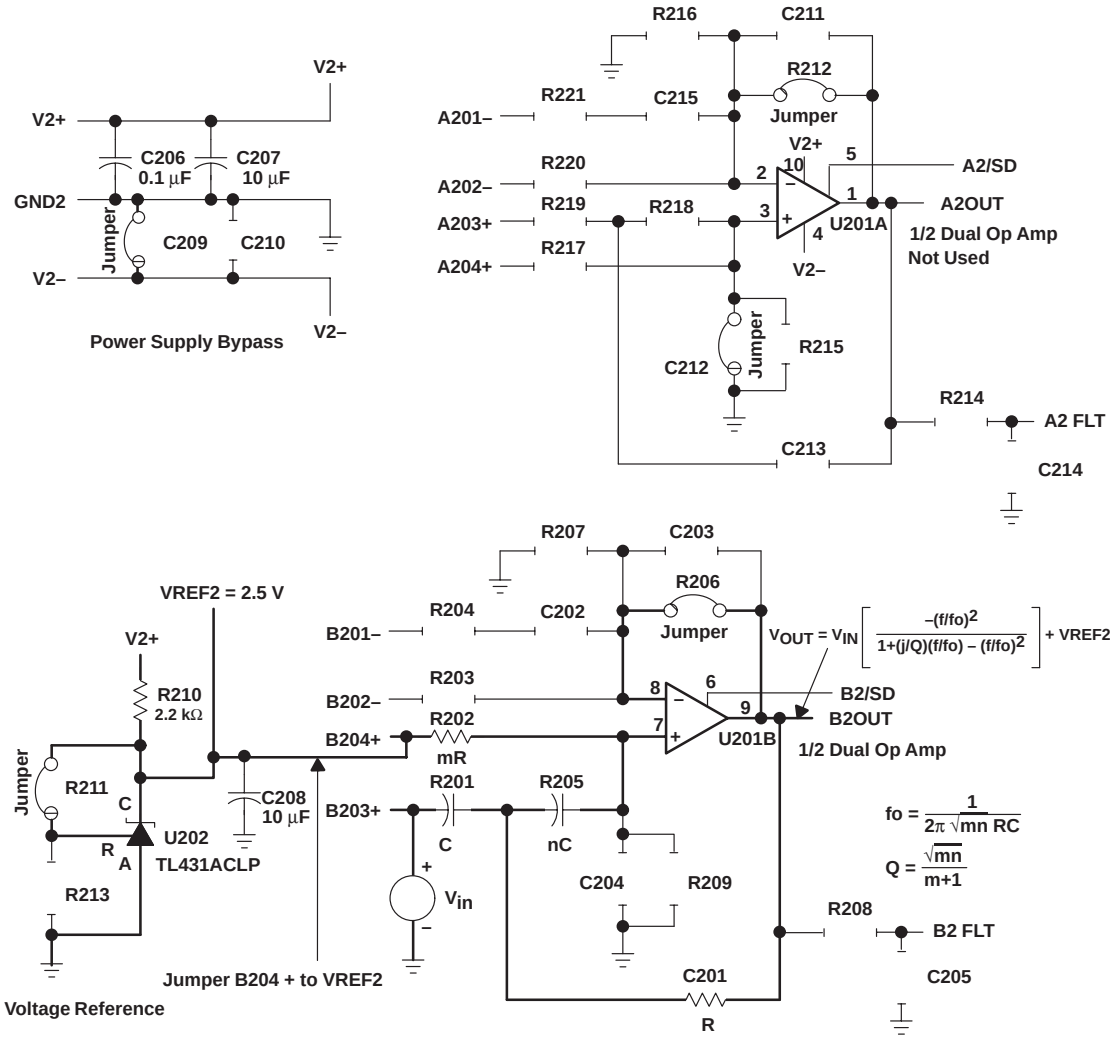
And

$$Q = \frac{\sqrt{m\ n}}{n + 1}$$

The TL431 adjustable precision shunt regulator, configured as shown, provides a low impedance reference for the circuit at about 1/2 V2+ in a 5 V system. Another option is to adjust resistors R211 and R213 for the desired VREF2 voltage. The formula for calculating VREF2 is:

$$\text{VREF2} = 2.50\ \text{V}\left(\frac{\text{R211} + \text{R213}}{\text{R213}}\right)$$

Figure 3–5. Sallen-Key High-Pass Filter With Single Supply Using Area 200



3.7 Two Operational Amplifier Instrumentation Amplifier

Figure 3–6 shows area 200 equipped with a dual operational amplifier configured as a two-operational-amplifier instrumentation amplifier using a voltage reference and single power supply.

Basic setup is done by choice of input and feedback resistors. The transfer function for the circuit as shown is:

$$V_{OUT} = V_{IN}\left(1 + \frac{2R212}{R220} + \frac{R212}{R221}\right) + VREF2$$

Where

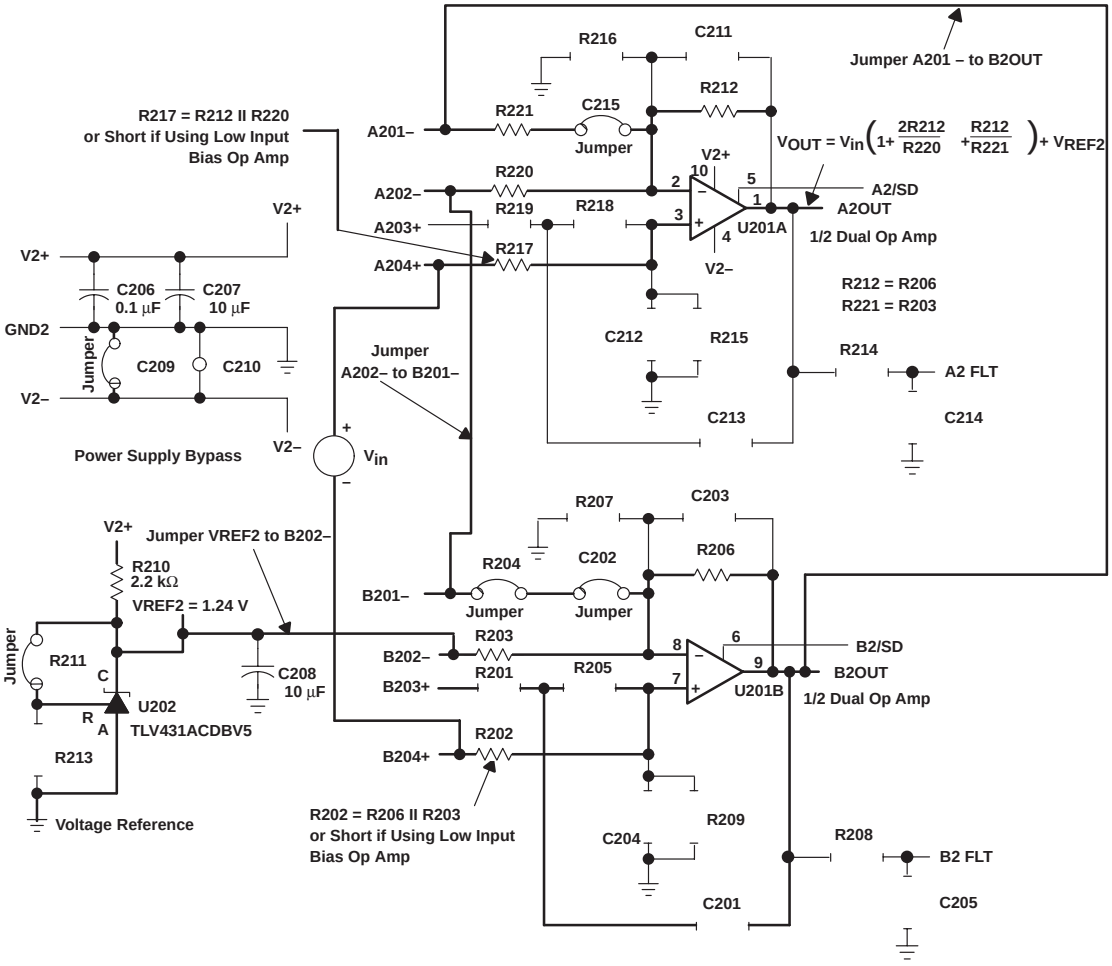
R212 = R206 and R221 = R203

To cancel the effects of input bias current, set R217 = R212 || R220 and set R202 = R206 ||R203, or use a 0-Ω jumper for R217 and R202 if the operational amplifier is a low input bias operational amplifier.

The TLV431 adjustable precision shunt regulator, configured as shown, provides a low impedance reference for the circuit at about 1/2 V2+ in a 3 V system. Another option is to adjust resistors R211 and R213 for the desired VREF2 voltage. The formula for calculating VREF2 is:

$$VREF2 = 1.24\ V\left(\frac{R211 + R213}{R213}\right)$$

Figure 3–6. Two Operational Amplifier Instrumentation Amplifier With Single Supply Using Area 200



3.8 Quad Operational Amplifier Instrumentation Amplifier

Figure 3–7 shows area 300 equipped with a quad operational amplifier configured as a quad-operational-amplifier instrumentation amplifier using a dual power supply.

Basic setup is done by choice of input and feedback resistors. The transfer function for the circuit as shown is:

$$V_{OUT} = \left(V_{INB} - V_{INA}\right)\left(\frac{R303 + 2(R302)}{R303}\right) + \frac{R325}{R309}$$

Where

R302 = R318, R309 = R316, and R325 = R329

$$A_V = \left(\frac{R303 + 2(R302)}{R303}\right) + \frac{R325}{R309} = 101 \quad \text{as shown}$$

To cancel the effects of offset errors, adjust V_{adj} (D304+) by applying an extra signal.

Figure 3–7. Quad Operational Amplifier Instrumentation Amplifier With Dual Supply Using Area 300