U-510 Using the bq2031 to Charge Lead-Acid Batteries

Description of Operation

The bq2031 has two primary functions: lead-acid battery charge control and switch-mode power conversion control. Figure 1 is a block diagram of the bq2031. The charge control circuitry is capable of a variety of full-charge detection techniques and supports three different charging algorithms. The Pulse-Width Modulator (PWM) provides control for high-efficiency current and voltage regulation.

Starting a Charge Cycle and Battery Qualification

When V_{CC} becomes valid (rises past its minimum value), the first activates battery temperature monitoring. Temperature is indicated by the voltage between the pins TS and SNS (V_{TEMP}). If the bq2031 finds the temperature out of range (or the thermistor is absent), it enters the Charge Pending State. In this state, all timers are suspended, charging current is kept off by MOD being held low, and the state is annunciated by LED_3 alternating high and low at approximately 1/6th second intervals.

Temperature checks remain active throughout the charge cycle. They are masked only when the bq2031 is in the Fault state (see below). When the temperature returns to the allowed charging range, timers are restarted (not reset) and the bq2031 returns to the state it was in when the temperature fault occurred.

When the thermistor is present and the temperature is within the allowed range, the bq2031 then checks for the presence of a battery. If the voltage between the BAT and SNS pins (V_{CELL}) is between the Low-Voltage Cut-Off threshold (V_{LCO}) and the High-Voltage Cut-Off (V_{HCO}), the bq2031 perceives a battery to be present and begins pre-charge battery qualification after a 500ms (typical) delay. If any new temperature or voltage faults occur during this time, the bq2031 immediately transitions to the appropriate state.

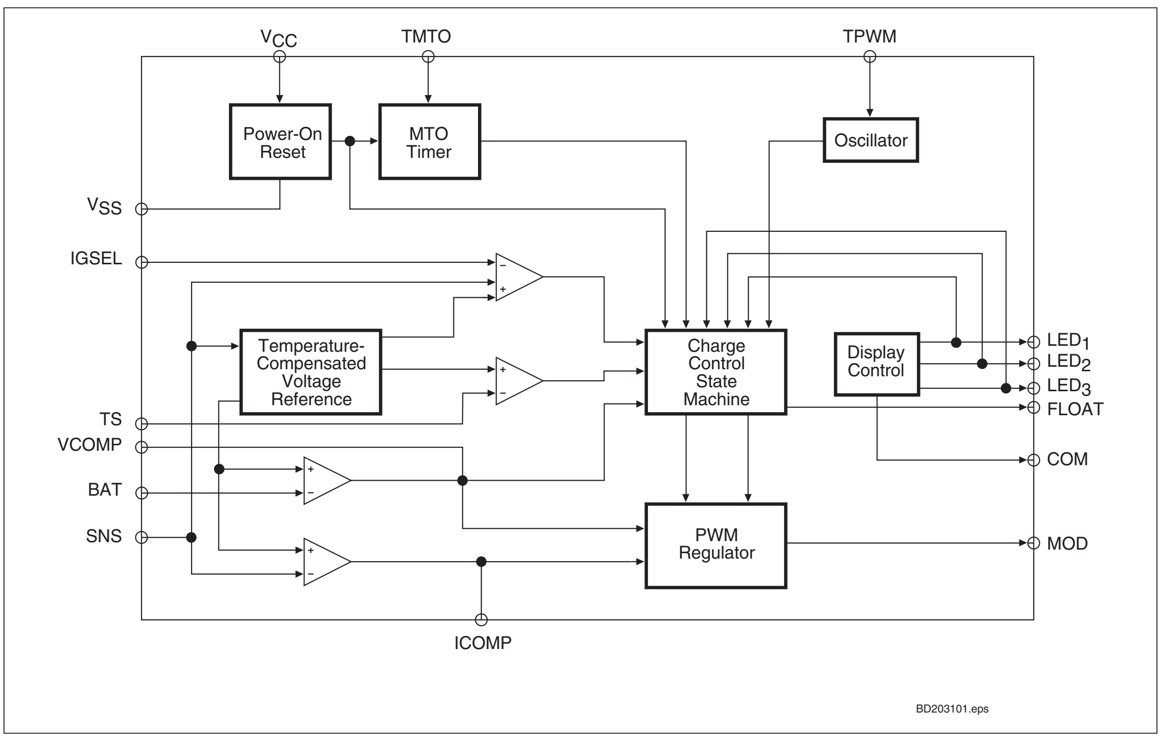

Figure 1. Block Diagram of the bq2031

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If V_{CELL} is less than V_{LCO} or above V_{HCO}, the bq2031 believes no battery is present and enters the Fault state; MOD is held low and LED_3 is turned on. This light gives the customer an indication that the charger is on, even though no battery is present. The bq2031 leaves the Fault state only if it sees V_{BAT} rise past V_{LCO} or fall past V_{HCO}, indicating a new battery insertion. If temperature is within bounds, there will again be a 500ms delay before battery qualification tests start.

Battery Qualification Tests

In test 1, the bq2031 attempts to regulate a voltage = V_{FLT} + 0.25V across the battery pack. The bq2031 monitors the time required for ISNS, the charging current, to rise to $I_{COND} = I_{MAX}/5$. If the current fails to rise to this level before the time-out period t_{QT1} expires (e.g., the battery has failed open), the bq2031 enters the Fault state, indicated by the LED_3 pin going high. Charging current is removed from the battery by driving the MOD pin low, and the bq2031 remains in this state until it detects the conditions to start a new charge cycle; the battery is replaced or V_{CC} is cycled off and then back on.

If test 1 passes, the bq2031 starts test 2 by attempting to regulate a charging current of I_{COND} into the battery pack. It monitors the time required for the pack voltage to rise above V_{MIN} (the voltage may already be over this limit). If the voltage fails to rise to this level before the time out period t_{QT2} expires (e.g., the battery has failed short), the bq2031 again enters the Fault state as described above. If test 2 passes, the bq2031 then begins fast (bulk) charging.

Fast Charging

The user configures the bq2031 for one of three fast charge and maintenance algorithms.

Two-Step Voltage (Figure 3)

This algorithm consists of three phases:

- Fast-Charge phase 1: The charging current is limited at I_{MAX} until the cell voltage rises to V_{BLK}.
- Fast-Charge phase 2: The charging voltage is regulated at V_{BLK} until the charging current drops below I_{MIN}.
- Maintenance phase: The charging voltage is regulated at V_{FLT}.

Two-Step Current (Figure 4)

This algorithm consists of two phases:

- Fast-Charge phase: The charging current is regulated at I_{MAX} until the cell voltage rises to V_{BLK} **or** the "Second Difference" of cell voltage drops below -8mV while V_{BAT} is over 2.0V. Second Difference is the accumulated differences between successive samples of V_{BAT}. The Second Difference technique looks for a negative change in battery voltage as the battery begins overcharging (see Figure 6).
- Maintenance phase: Fixed-width pulses of charging current = I_{COND} are modulated in frequency to achieve an average value of I_{MIN}. See Appendix A for implementation details.

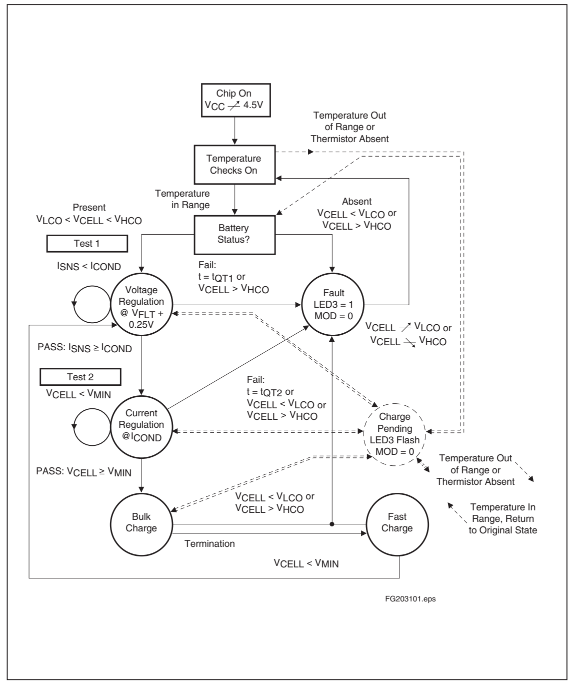

Figure 2. Cycle Start/Battery Qualification State Diagram

Pulsed Current (Figure 5)

This algorithm consists of two phases:

- Fast-Charge phase: The charging current is regulated at I_{MAX} until the cell voltage rises to V_{BLK}.
- Maintenance phase: Charging current is removed until the battery voltage falls to V_{FLT}; charging current is then restored and regulated at I_{MAX} until the battery voltage once again rises to V_{BLK}. This cycle is repeated indefinitely.

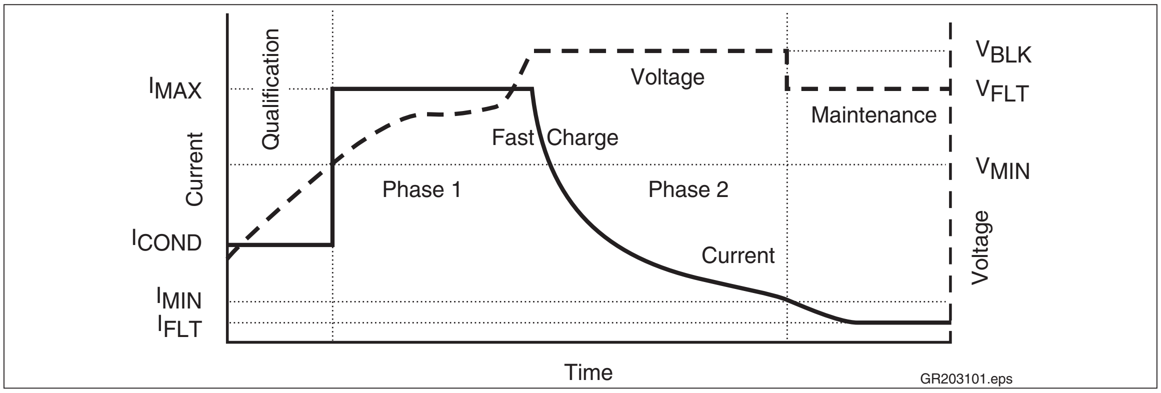

Figure 3. Two-Step Voltage Algorithm

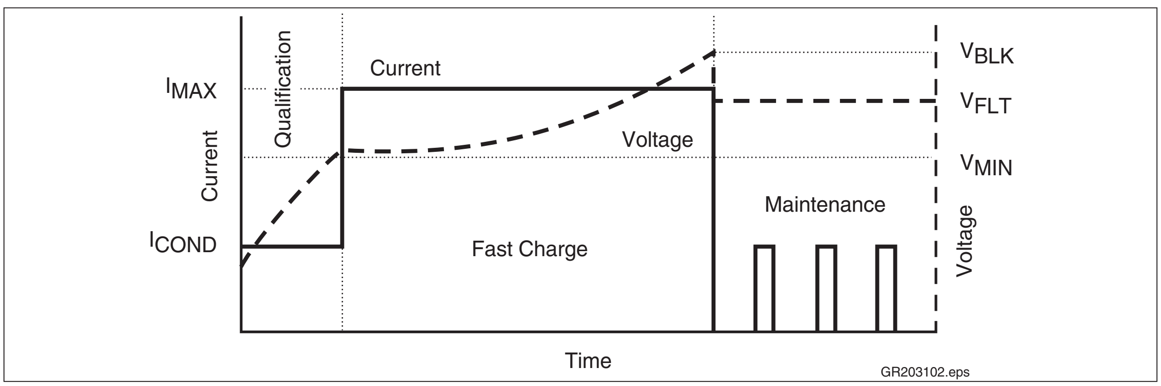

Figure 4. Two-Step Current Algorithm

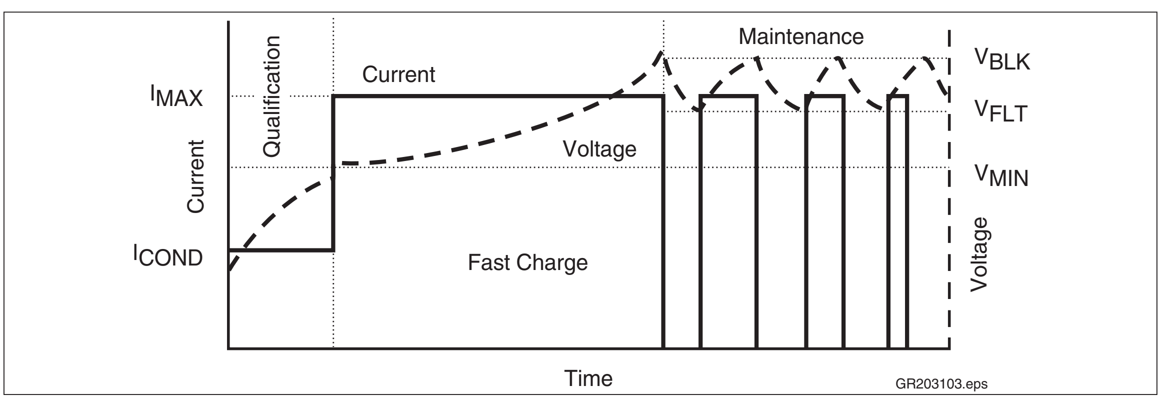

Figure 5. Pulsed Current Algorithm

Safety Time-Out

A safety timer limits the time the charger can spend in any phase of the charging cycle except maintenance. This Maximum Time-Out (MTO) timer is reset at the end of successful pre-charge qualification when the bq2031 begins fast charging1. If MTO times out before a fast charge termination criterion is met, the charging current is turned off (MOD driven low) and the bq2031 enters the Fault state exactly as if it had failed a pre-charge qualification test.

There is one exception. In the Two-Step Voltage algorithm, MTO is reset when the bq2031 transitions from the current-limited phase 1 to the voltage-regulated phase 2 of fast charging. If MTO expires while the bq2031 is still in phase 1, it does not enter the Fault state but instead transitions to maintenance phase.

During maintenance, the MTO timer is reset at the beginning of each new pulse in the Two-Step Current and Pulsed Current algorithms. It expires (and puts the bq2031 in the Fault state) only when the bq2031 beccomes "jammed" with a pulse stuck "on." The MTO timer is not active during the maintenance phase of the Two-Step Voltage algorithm.

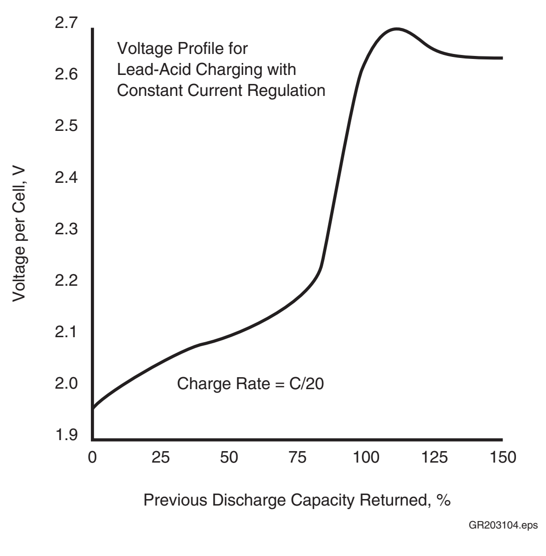

Figure 6. Voltage Roll-Off in Constant-Current Charging Profile

Hold-off Periods

Old age and/or abuse can create conditions in lead-acid batteries that may generate a large transient voltage spike when current-regulated charging is first applied. This spike could cause early termination in the fast charge algorithms by mimicking their voltage-based termination criteria. To prevent this, the bq2031 uses a "hold-off" period at the beginning of the fast charge phase. During this time, all voltage criteria are ignored except cutoff voltages. (Straying outside the range between V_{HCO} and V_{LCO} still causes the bq2031 to believe the battery has been removed, and the bq2031 enters the Fault state and shuts off charging current.) A hold-off period is also enforced during test 2 of pre-charge qualification for the same reason.

Configuration Instructions

Selecting Charge Algorithm and Display Mode

QSEL/LED_3, DSEL/LED_2, and TSEL/LED_1 are bi-directional pins with two functions: they are LED driver pins as outputs and programming pins for the bq2031 as inputs. The selection of pull-up, pull-down, or no pull resistor for these pins programs the charging algorithm on QSEL and TSEL per Table 1 and the display mode on DSEL per Table 2. The bq2031 forces the output driver on these bi-directional pins to their high-impedance state (as well as their common return output pin, COM) and latches the programming data sensed on the inputs when any one of the following three events occurs:

1. V_{CC} rises to a valid level.
2. The bq2031 leaves the Fault state.
3. The bq2031 detects battery insertion.

The LEDs go blank for approximately 0.75s. (typical) while new programming data is latched.

Figure 7 shows the bq2031 configured for the Two-Step Current algorithm and display mode 2.

Table 1. Programming Charge Algorithms

Charge Algorithms	QSEL	TSEL	Programmable Thresholds
Two-Step Voltage	L	H/L*	I_{MAX}, V_{BLK}, V_{FLT}
Two-Step Current	H	L	I_{MAX}, V_{BLK}, I_{MIN}
Pulsed Current	H	H	I_{MAX}, V_{BLK}, V_{FLT}

Note: * Set either high or low; do not float pin.

1 The MTO timer also resets at the beginning of the pre-charge qualification period. However, t_{QT1} or t_{QT2} (the qualification test time limits) expire and put the bq2031 in the Fault state before the MTO limit can be reached. The MTO timer is suspended while the bq2031 is in the Fault state, and is reset by the conditions that allow the bq2031 to exit that state.

Table 2. bq2031 Display Output Summary

Mode	Charge State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Battery absent	Low	Low	High
	Pre-charge qualification	Flash*	Low	Low
	Fast charging	High	Low	Low
	Maintenance charging	Low	High	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High
DSEL = 1 (Mode 2)	Battery absent	Low	Low	High
	Pre-charge qualification	High	High	Low
	Fast charge	Low	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High
DSEL = Float (Mode 3)	Pre-charge qualification	Flash*	Flash*	Low
	Battery absent	Low	Low	High
	Fast charge: current regulation	Low	High	Low
	Fast charge: voltage regulation	High	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High

Notes: 1 = V_{CC}, 0 = V_{SS}, X = LED state when fault occurred.
* Flash = ⅙ sec. low, ⅙ sec. high

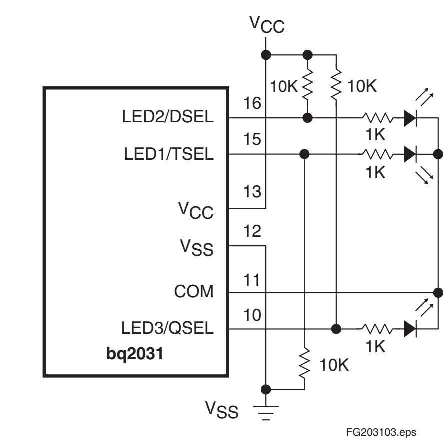

Figure 7. Configuring 10K Two-Step Current Algorithm and Display Mode Selection

Setting Voltage and Current Thresholds

Fixed Thresholds

The bq2031 uses the following fixed thresholds:

- **V_{HCO}**—High-Cutoff Voltage: V_{BAT} rising above this level is interpreted as battery removal, cutting off charging current. $V_{HCO} = 0.6 * V_{CC}$.
- **V_{LCO}**—Low-Cutoff Voltage: V_{BAT} dropping below this level is interpreted as battery removal, cutting off charging current. $V_{LCO} = 0.8V$.
- **V_{MIN}**—Minimum Voltage: Used in pre-charge qualification test 2. $V_{MIN} = 0.34 * V_{CC}$.
- **I_{COND}**—Conditioning Current: Used in the maintenance phase of the Two-Step Current algorithm and pre-charge qualification tests 1 and 2. $I_{COND} = I_{MAX}/5$. I_{MAX} is set by Equation 3.

Configurable Thresholds

The bq2031 uses the following configurable thresholds:

- **V_{BLK}**—Upper voltage limit during fast charge, typically specified by the battery manufacturers to be 2.45V–2.5V per cell @ 25°C.
- **V_{FLT}**—Minimum charge voltage required to compensate for the battery's self-discharge rate and maintain full charge on the battery. A value is usually recommended by the battery manufacturer.
- **I_{MAX}**—Fast charge current specified as a function of "C," the capacity of the battery in Ampere-hours (e.g., a charge rate of 1C for a 5Ah battery is 5A). Typical values range from $^{C}/_{10}$ to C, although some battery vendors may approve higher charge rates.

V_{FLT}, V_{BLK}, and I_{MAX} are configured by the user when selecting resistor values for the battery voltage divider network (see Figure 8). V_{FLT} is set by RB1 and RB2 by:

Equation 1

$$\frac{RB1}{RB2} = \frac{(N * V_{FLT})}{2.2V} - 1$$

VBLK is determined by:

Equation 2

$$\frac{RB1}{RB2} + \frac{RB1}{RB3} = \left(\frac{N * V_{BLK}}{2.2}\right) - 1$$

I_{MAX} is determined by:

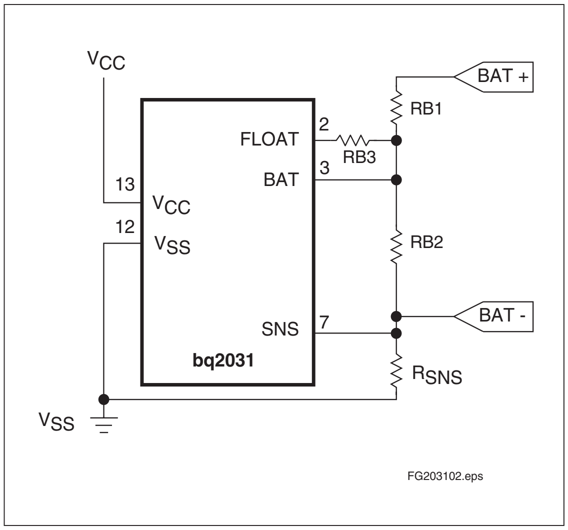

Figure 8. configuring the Battery Divider and Current Sense Circuit

Equation 3

$$I_{MAX} = \frac{0.250V}{R_{SNS}}$$

where:

- N = Number of series cells in the battery pack
- V_{FLT} = Value recommended by manufacturer
- V_{BLK} = Value recommended by manufacturer at 25°C. If you have selected the Two-Step Current algorithm and want Second Difference detection to be your primary fast charge termination criterion, use V_{BLK} = 2.75V.
- I_{MAX} = Desired maximum charge current

The bq2031 internal band-gap reference voltage at 25°C is 2.2V. This reference shifts with temperature at -3.9mV/°C to compensate for the negative temperature coefficient of lead-acid chemistry.

The total resistance presented by the divider between BAT+ and BAT- (RB1 + RB2) should be between 150kΩ and 1MΩ . The minimum value ensures that the divider network does not drain the battery excessively when the power source is disconnected. Exceeding the maximum value increases the noise susceptibility of the BAT pin.

An empirical procedure for setting the values in the resistor network is as follows:

1. Set RB2 to 49.9 kΩ (for 3 to 18 series cells).

2. Determine RB1 from equation 1 given V_{FLT}.
3. Determine RB3 from equation 2 given V_{BLK}.
4. Determine R_{SNS} from equation 3 given I_{MAX}.

Table 3 shows the results of these calculations at several example cell counts for V_{FLT} = 2.25V and V_{BLK} = 2.45V. 1% resistors are recommended.

Table 3. Example Resistor Values by Number of Cells

Number of Cells	RB1 (kΩ)	RB2 (kΩ)	RB3 (kΩ)
3	102.0	49.9	383.0
6	261.0	49.9	475.0
12	562.0	49.9	511.0
18	866.0	49.9	536.0

I_{MIN}—In the Two-Step Voltage algorithm, I_{MIN} is the level to which charging current must drop to terminate fast charge. In the Two-Step Current algorithm, it is the average value of pulsed current in the maintenance phase. I_{MIN} is a fraction of I_{MAX} programmed by the state of the pin IGSEL and the charging algorithm selected, per Table 4.

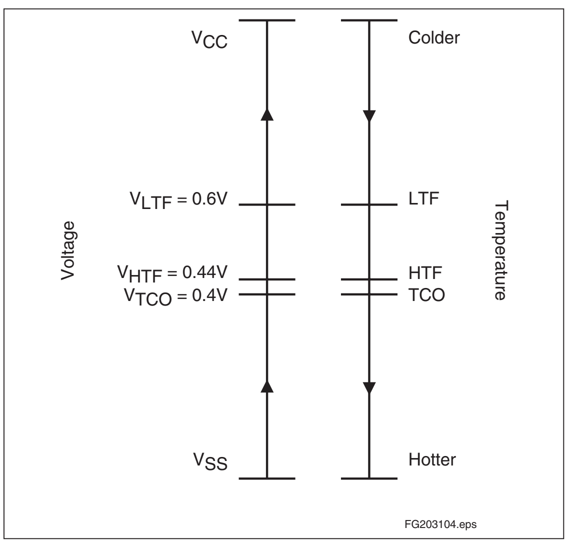

Figure 9. Voltage Equivalent of Current Thresholds

Table 4. Programming I_{MIN}

Two-Step Voltage		Two-Step Current	
IGSEL	I_{MIN}	IGSEL	I_{MIN}
L	$I_{MAX}/10$	L	$I_{MAX}/10$
H	$I_{MAX}/20$	H	$I_{MAX}/20$
Z	$I_{MAX}/30$	Z	$I_{MAX}/40$

Setting Temperature Thresholds

The bq2031 senses temperature by monitoring the voltage between the TS and SNS pins. The bq2031 assumes a Negative Temperature Coefficient (NTC) thermistor, so the voltage on the TS pin is inversely proportional to the temperature (see Figure 9). The temperature thresholds used by the bq2031 and their corresponding TS pin voltage are:

TCO—Temperature Cut-Off: Higher limit of the temperature range in which charging is allowed.
$V_{TCO} = 0.4 * V_{CC}$.

HTF—High-Temperature Fault: Threshold to which temperature must drop after Temperature Cut-Off is exceeded before charging can begin again. $V_{HTF} = 0.44 * V_{CC}$

LTF—Low-Temperature Fault: Lower limit of the temperature range in which charging is allowed.
$V_{LTF} = 0.6 * V_{CC}$.

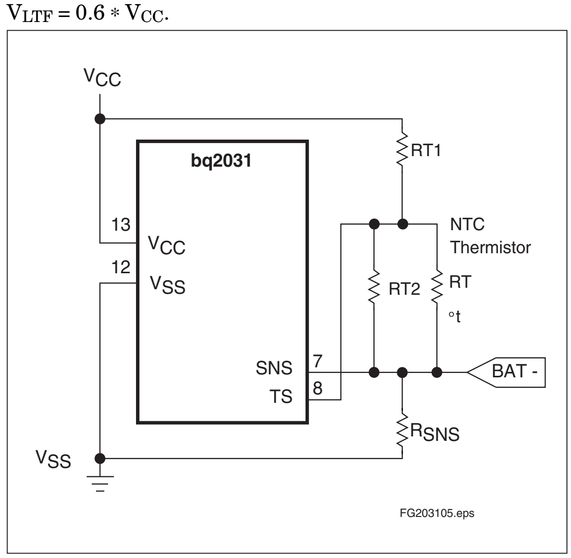

Figure 10. Configuring Temperature Sensing

A resistor-divider network must be implemented that presents the defined voltage levels to the TS pin at the desired temperatures (see Figure 10).

The equations for determining RT1 and RT2 are:

Equation 4

$$0.6 * V_{CC} = \frac{(V_{CC} - 0.250)}{1 + \frac{RT1 * (RT2 + R_{LTF})}{(RT2 * R_{LTF})}}$$

Equation 5

$$0.44 = \frac{1}{1 + \frac{RT1 * (RT2 + R_{HTF})}{(RT2 * R_{HTF})}}$$

where:

- R_{LTF} = Thermistor resistance at LTF
- R_{HTF} = Thermistor resistance at HTF

TCO is determined by the values of RT1 and RT2. 1% resistors are recommended. As an example, the resistor values for several temperature windows computed for a Philips 2333-640-63103 thermistor are shown in Table 5.

Table 5. RT1 and RT2 Values for Temperature Thresholds

LTF (°C)	HTF (°C)	TCO (°C)	RT1 (kΩ)	RT2 (kΩ)
0	45	47	3.57	7.50
5	45	47	3.65	8.66
–5	50	52	2.74	5.36

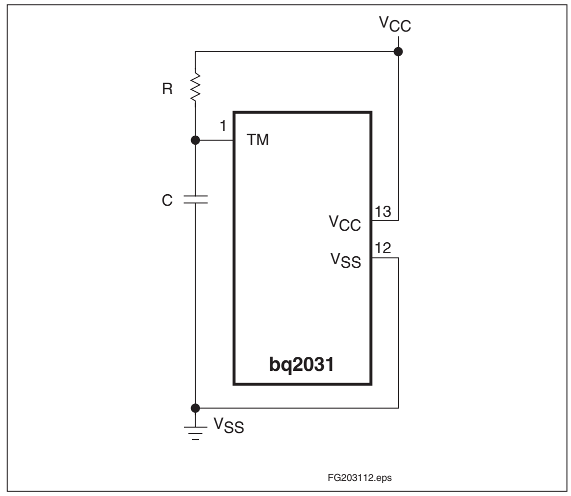

Figure 11. RC Network for Setting MTO

Disabling Temperature Sensing

Temperature sensing may be disabled by removing the thermistor and RT1, and using a value of 100kΩ for RT1 and RT2.

Setting Timers

The user sets the Maximum Time-Out (MTO) value. All other timing periods used in the bq2031 are fixed as fractions of MTO (see Table 6). MTO is set by an R-C network on the TMTO pin as shown in Figure 11.

Table 6. Timing Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{MTO}	Maximum Time Out range	1	-	24	hours
t_{QT1}	Qualification time-out test 1	-	$0.02t_{MTO}$	-	-
t_{QT2}	Qualification time-out test 2	-	$0.16t_{MTO}$	-	-
t_{DV}	$-\Delta^2V$ termination sample frequency	-	$0.008t_{MTO}$	-	-
t_{HO1}	Qualification test 2 hold-off period	-	$0.002t_{MTO}$	-	-
t_{HO2}	Bulk-charge hold-off period	-	$0.015t_{MTO}$	-	-

The equation for MTO is:

Equation 6

$$MTO\ (in\ hours) = 0.5 * R * C$$

where R is in kΩ and C is in µF. The value for C must not exceed 0.1µF.

Example: An MTO of 5 hours is set by R = 100kΩ and C = 0.1µF

Switch-Mode Power Conversion

The bq2031 incorporates the necessary PWM control circuitry to support switch-mode voltage and current regulation.

Figure 12 shows a functional block diagram of a switch-mode buck topology converter using the bq2031. The battery voltage is divided down to a per-cell equivalent value at the BAT pin. During voltage regulation, the voltage on the BAT pin (V_{BAT}) is regulated to the internal band-gap reference of 2.2V at 25°C (with a temperature drift of -3.9 mV/°C). The charge current through the inductor L is sensed across the resistor R_{SNS}. During current regulation, the bq2031 regulates the voltage on the SNS pin (V_{SNS}) to a temperature-compensated reference of 0.250V.

The passive components C_I on the I_{COMP} pin, R_V and C_V on the V_{COMP} pin, and C_F across the high side of the battery voltage divider form the phase compensation network for the current and voltage control loops, respectively. The diodes (Db1 and Db2) serve to prevent battery drain when VDC is absent, while the pull-up resistor (R_P) is used to detect battery removal. The resistor R_S, typically a few tens of mΩ, is optional and depends on the battery impedance and the resistance of the battery leads to and from the charger board.

Pulse-Width Modulator

The bq2031 incorporates two PWM circuits, one for each control loop (voltage and current, see Figure 13). Each PWM circuit runs off a common saw-tooth waveform (V_S) whose time-base is controlled by a timing capacitor (CPWM) on the TPWM pin.

The relationship between CPWM and the switching frequency (F_S) is given by :

Equation 7

$$F_S = \frac{0.1}{C_{PWM}}\ kHz$$

where CPWM is in µF.

Each PWM loop starts with a comparator whose positive terminal is driven by V_S. The negative terminal is driven by the output of an Operational Transconductance Amplifier (OTA) which, with the compensation network connected via V_{COMP} or I_{COMP}, generates the control signal V_C. The OTA characteristics are: R_O = 250kΩ; G_M = 0.42m-mho; gain bandwidth = 80MHz. The output of each comparator, along with the ramp waveform (V_S), is used to generate a pulse-width modulated waveform at a constant frequency on the MOD output. Figure 14 shows the relationship of MOD with V_C and V_S.

The MOD output swings rail-to-rail and can source and sink 10mA. It is used to control the drive circuitry of the switching transistor.

The pulse-width modulated square-wave signal on the MOD pin is synchronized to the internal sawtooth ramp signal. The ramp-down time (T_D) is fixed at approximately 20% of the ramp time-period (T_P). This limits the maximum duty-cycle achievable to approximately 80%. See Figure 14.

Example: At a switching frequency of F_S = 100kHz, T_D = 2µs.

Inductor Selection

The inductor selection criteria for a DC-DC buck converter vary depending on the charging algorithm used. For the Two-Step Current and Pulsed Current charge algorithms, the inductor equation is:

Equation 8

$$L = \frac{(N * V_{BLK} * 0.5)}{F * \Delta I}$$

where:

- N = Number of cells
- V_{BLK} = Bulk voltage per cell, in volts
- F_S = Switching frequency, in Hertz
- ΔI = Ripple current at I_{MAX}, in amperes

The ripple current is usually set between 20–25% of I_{MAX}.

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Pulsed Current mode. Assuming a ripple = 25% of I_{MAX}, the inductor value required is:

Equation 9

$$L = \frac{(6 * 2.45 * 0.5)}{(100000 * 0.6875)} = 107\mu H$$

The inductor formula for the Two-Step Voltage charge algorithm is dictated by the inductor current, which must remain continuous down to I_{MIN} during Fast Charge phase 2 (voltage regulation phase).

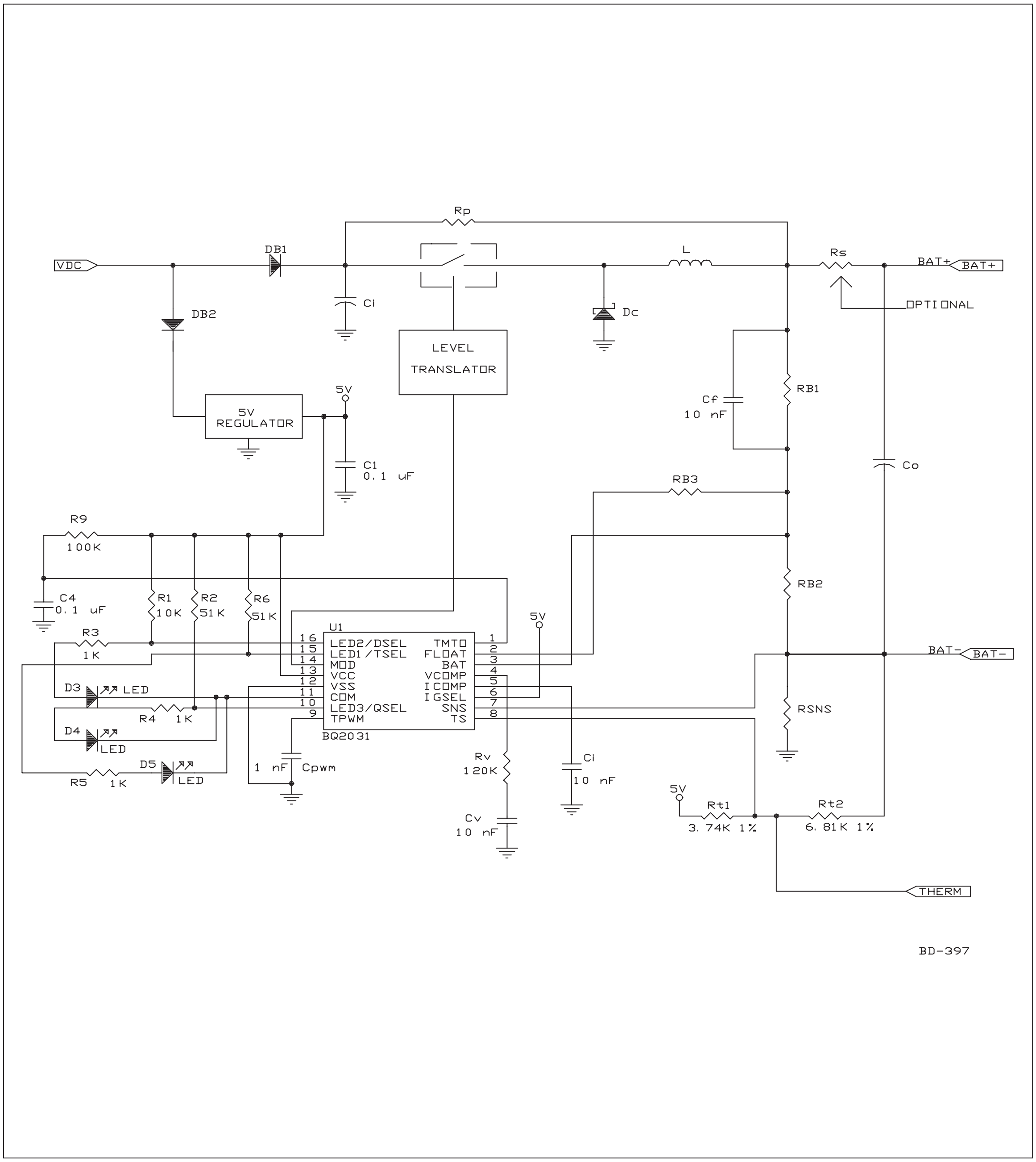

Figure 12. Functional Diagram of a Switch-Mode Buck Regulator Lead-Acid Charger Using the bq2031

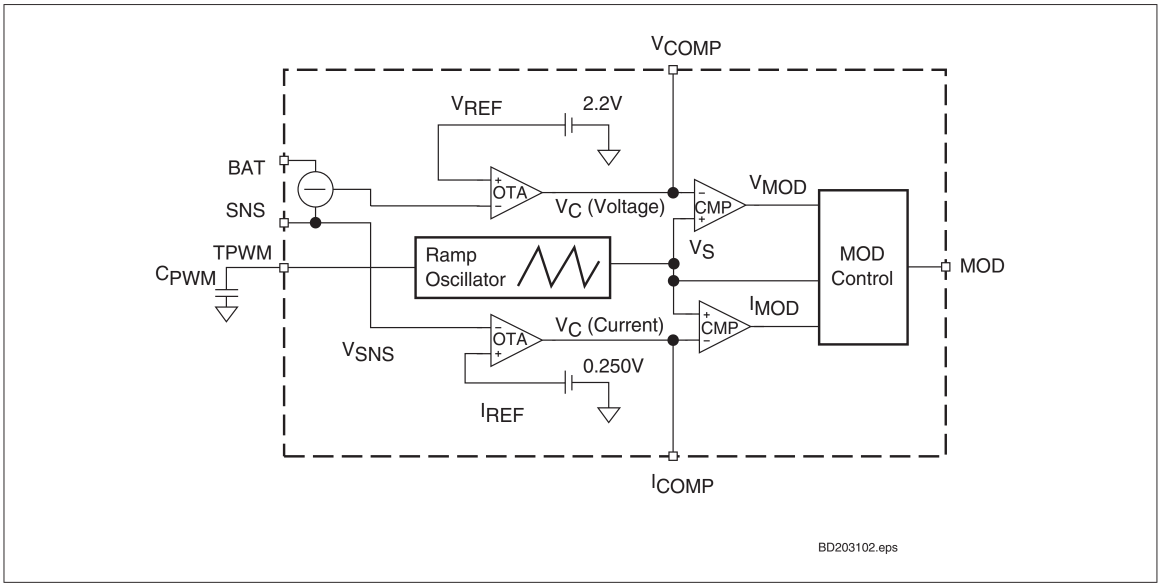

Figure 13. Block Diagram of the bq2031 PWM Control Circuitry

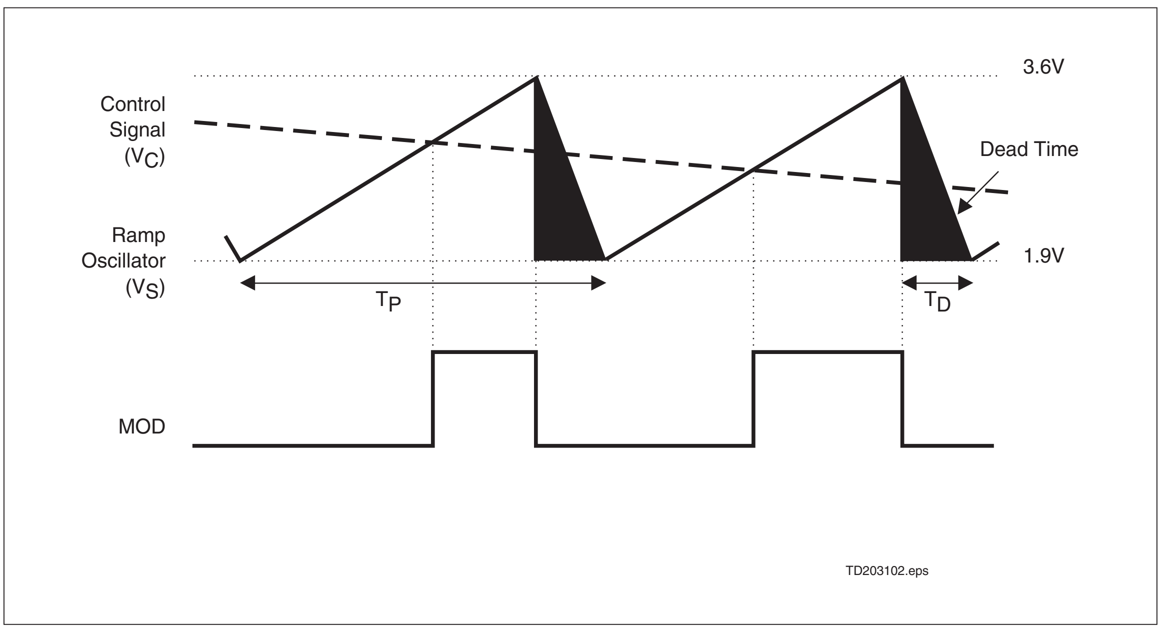

Figure 14. Relationship of MOD Output to Sawtooth Waveform V_S and Control Signal V_C

Equation 10

$$L = \frac{N * V_{BLK} * 0.5}{F_S * 2 * I_{MIN}}$$

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Two-Step Voltage mode, with I_{MIN} = I_{MAX}/20. The inductor value required is:

Equation 11

$$L = \frac{6 * 2.45 * 0.5}{(100000 * 2 * 0.1375)} = 267\mu H$$

Phase Compensation

For buck-mode switching applications, the suggested component values shown in Figure 12 are good starting points. More details on the calculations used in this program are available in the application note entitled "Switch-Mode Power Converson Using the bq2031." For assistance with other power supply topologies, contact one of our field application engineers.

Miscellaneous Issues

V_{CC} Supply

The V_{CC} supply provides bq2031 power and serves as the reference voltage for all temperature sense thresholds (V_{LTF}, V_{HTF}, and V_{TCO}) and the battery voltage thresholds V_{HCO} and V_{MIN}. The timer thresholds (MTO and its derivatives) are trimmed within 5% of the typical value with V_{CC} = 5V.

The V_{BLK} and V_{FLT} thresholds are set from an external divider network powered by the battery. These thresholds are referenced to an internal band-gap reference, and the accuracy of voltage regulation will not be adversely affected by variation in V_{CC}. The current regulation threshold (I_{MAX}) is referenced to a temperature compensated reference and is also unaffected by V_{CC}.

DC Power Supply

The DC power supply voltage (V_{DC}) for a switch-mode application must satisfy the following criterion:

Equation 12

$$V_{DC} = (N * V_{BLK} * 1.2) + 2$$

where:

- N = Number of cells
- V_{BLK} = Bulk voltage threshold per cell

Logical Control of Charging

Charge Inhibit

An inhibit input may be implemented by connecting the cathode of a small-signal diode to the TS pin. A CMOS logic-level "1" applied to the anode of the diode then functions as an inhibit input, by driving the temperature sense voltage out of its allowed range and simulating an under-temperature condition. The bq2031 enters the Charge Pending state, shutting off charging current (driving MOD low) and suspending all timers. When the Inhibit signal is allowed to float, the bq2031 returns to its previous state (as long as the temperature is still within the allowed range). The bq2031 restarts (but does not reset) its timers, and the suspended charge cycle resumes at the point where it stopped.

Reset

A logical Reset signal for the bq2031 can be created in a manner similar to the Charge Inhibit input described above. Instead of being connected to the T_S pin, however, the diode is connected to the BAT input. In this configuration, a logic "1" on the diode drives V_{BAT} above V_{HCO}, simulating battery removal. The bq2031 enters the Fault state and waits to see a battery insertion; V_{BAT} rising past V_{LCO} or falling past V_{HCO}. Removing the logic "1" from the diode creates this transition (as long as a battery is still present), and the bq2031 starts a new charge cycle.

Caution: To avoid damage to the bq2031, always keep the voltage applied to the anode of the diode below V_{CC} for either the Charge Inhibit or Reset implementations.

Layout Guidelines

Printed circuit board layout must adhere to the following guidelines to minimize noise injection on the high-impedance pins (BAT, V_{COMP}, I_{COMP}, and SNS).

1. Use a single-point grounding technique such that the isolated small-signal ground path and the high-current power ground path return to the power supply ground.
2. The charging path components and traces must be isolated from the voltage and current feedback small signal paths.
3. 0.1µF and 10µF decoupling capacitors must be placed close to the V_{CC} pin. This also helps to prevent voltage dips while the bq2031 is driving the LEDs.
4. A 100pF capacitor, if used for coupling the BAT and SNS pins, must be placed close to those pins.
5. The compensation network on I_{COMP} and V_{COMP} must be placed close to their respective pins.

6. Minimize loop area in paths with high pulsating currents.

Battery Removal Detection

The bq2031 interprets V_{BAT} rising past V_{HCO} or falling past V_{LCO} as battery removal, and the bq2031 enters the Fault state until a new battery insertion is seen. The battery removal transitions are precluded during periods of voltage regulation unless circuitry (e.g., a pull-up to V_{DC}) is provided to pull V_{BAT} out of the "battery present" range.

Voltage regulation occurs during phase 2 of the Two-Step Voltage fast charge algorithm and in battery qualification test 1 which precedes all three algorithms. The time-out period of this test (= 0.02 * MTO) is at least 1.2 minutes and may be as long as 28.8 minutes. Unless waiting through this period before detecting battery removal is acceptable, the pull-up is required in the purely current regulated algorithms as well. A diode should also be installed in the path of the pull-up to prevent the power supply from draining the battery when the supply is turned off. Refer to resistor R12 and diode D3 in the example design in Figure 15.

This pull-up creates a background trickle charge current to the battery that can be minimized by minimizing the voltage overhead; that is, the voltage difference between the V_{DC} supply and the battery stack.

Load-Only Operation

The bq2031 supports the case in which the charger must supply the load in the absence of a battery, provided the load can pass the two pre-charge qualifications tests (draw current of at least I_{COND} when regulated at V_{FLT} + 0.25V and maintain voltage of at least V_{MIN} when regulated at I_{COND}). Further, the load must not create conditions that cause fast charge termination or it must be able to tolerate the conditions of maintenance regulation for the charge algorithm selected. This is regulation at V_{FLT} in the case of the Two-Step Voltage algorithm or constant or hysteretic pulsed current supply in the case of the Two-Step Current and Pulsed Current algorithms, respectively. This can be a problem for intermittent loads unless circuitry is provided to maintain these conditions during the low-load or no-load periods.

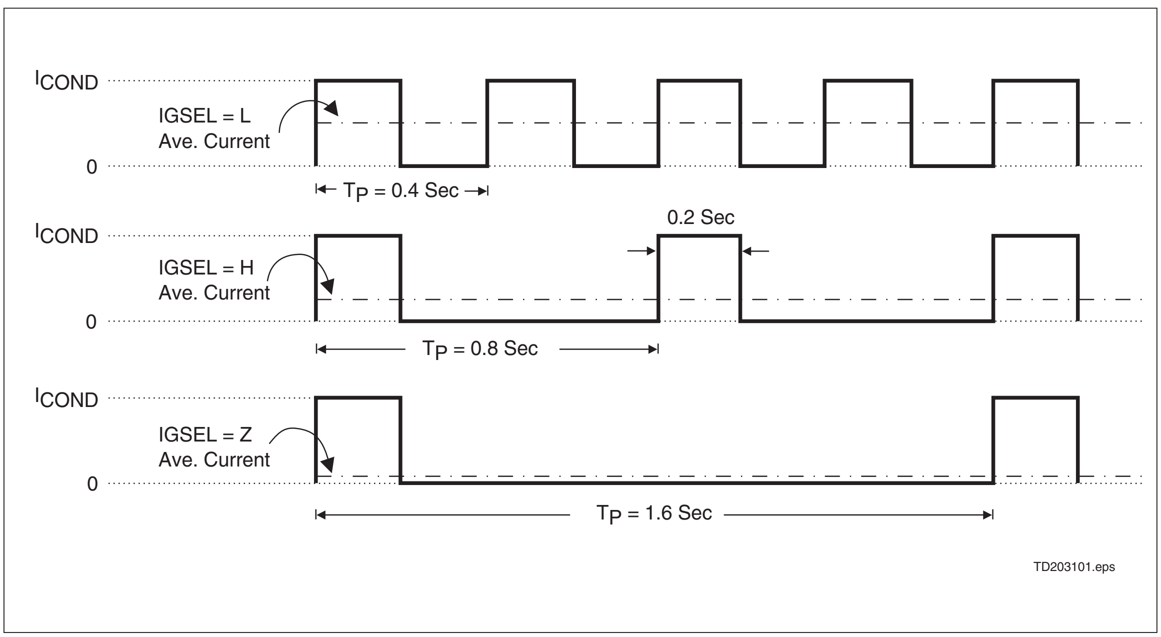

Figure 15. Implementation of Fixed-Pulse Maintenance Charge

Back-up Supply Regulation

To protect the system from damage during periods of fast charge voltage regulation, the bq2031 regulates to I_{MAX} if the current tries to rise above that level, and has an absolute current limit of 1.25 * I_{MAX}. Similarly, during periods of fast charge current regulation, the bq2031 enforces a V_{BLK} upper limit on voltage, and regulates to V_{BLK} if the voltage tries to rise above this level. During the maintenance phase, the bq2031 regulates to V_{FLT} and I_{COND} during periods of current or voltage regulation, respectively.

Applications Example: Single-Ended Buck Charger

For an application example, please see the DV2031S1 data sheet and schematic.

Appendix A: Implementation Details of Pulsed Maintenance Charging

Two-Step Current Algorithm

Maintenance charging in the Two-Step Current Algorithm is implemented by varying the period (TP) of a fixed current ($I_{COND} = I_{MAX}/5$) and duration (0.2 second) pulse to achieve the configured average maintenance current value. See Figure 16.

Maintenance current can be calculated by:

Equation 14

$$\text{Maintenance current} = \frac{((0.2) * I_{COND})}{T_P} = \frac{((0.04) * I_{MAX})}{T_P}$$

where TP is the period of the waveform in seconds.

Table 7 gives the values of TP programmed by IGSEL.

Table 7. Fixed-Pulse Period by IGSEL

IGSEL	T_P (s)
L	0.4
H	0.8
Z	1.6

Revision History

Charge No.	Page No.	Description	Nature of Change
1	4, 5	Renamed	Figure 7 was: Pulsed Current; Is: Two-Step Current
1	6, 8	Changed values in Equations 3 and 4	Was: 0.275V; is now 0.250V
1	9	Under Switch-Mode Power Conversion	Changed value, was: 0.275V; is now 0.250V
1	11	Figure 13 changed	Block diagram has been reconfigured. VC was 0.275V; us biw 0.250V
1	13	Applications Example changed	Changed to: For an application example, please see the DV2031S1 datasheet and schmatic
1	14	Figure 15. Example Schematic of a Single-Ended Buck Topology Charger	Deleted
1	15	Table 7. Parts List for Single-Ended Buck Charger	Deleted
2	8	Equation 4	Was: -0.275 Is: -0.250
2	9	Temperature-compensated reference	Was: 0.275V Is: 0.250V
2	12	Equation 12	Was: $V_{DC} = (N * V_{BLK}) + 3V$ Is: $V_{DC} = (N * V_{BLK} * 1.2) + 2$
3	12	Clarify description for phase compensation	

Notes: Change 1 = April 1997 B changes from Dec. 1995.
Change 2 = Oct. 1997 C changes from April 1997 B.

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