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A Revolutionary Power Management Solution for Highly Efficient, Multiple Output Applications

Application Note

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Power Supply Control Products

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A Revolutionary Power Management Solution for Highly Efficient, Multiple Output Applications

Bill Andreycak *Power Supply Control Products*

1 Abstract

Radical changes in the implementation of distributed power in many new high power, high reliability applications are taking place. The conventional approach of bussing around several individual voltages on elaborate backplanes is quickly being abandoned in lieu of numerous point-of-load power supplies, each developing the multiple, on-card voltages required. The abrupt change in direction toward localized point-of-load power conversion within newer distributed power architectures certainly adds an interesting twist to power management implementation. In high reliability applications, the conventional approach of bussing around numerous outputs of redundant power modules is giving way to a far more streamlined, single supply voltage. Gone soon could be the multitude of high current bus bars in exchange for a single 24-V to 48-V distributed dc source.

2 Topology and Converter Fundamentals

This new power conversion technique incorporates a cascaded arrangement of a push-pull converter using synchronous rectification followed by a buck regulator, as shown in Figure 1. There are numerous differences, however, between this adaptation and the conventional versions of both converters. The list of significant advantages includes zero voltage switching of the push-pull converter switches and rectifiers and near-lossless turn-on of the buck regulator switch. Also, strategically located leakage inductance, present on the secondary side defines the rate of change in current (dI/dt) at turn-off of the buck's commutation rectifier switch. Each of these items contributes to developing a power management solution with significantly higher overall efficiency with lower EMI/RFI. Complete circuit details including voltage, current and timing waveforms are well documented in References 1 and 2.

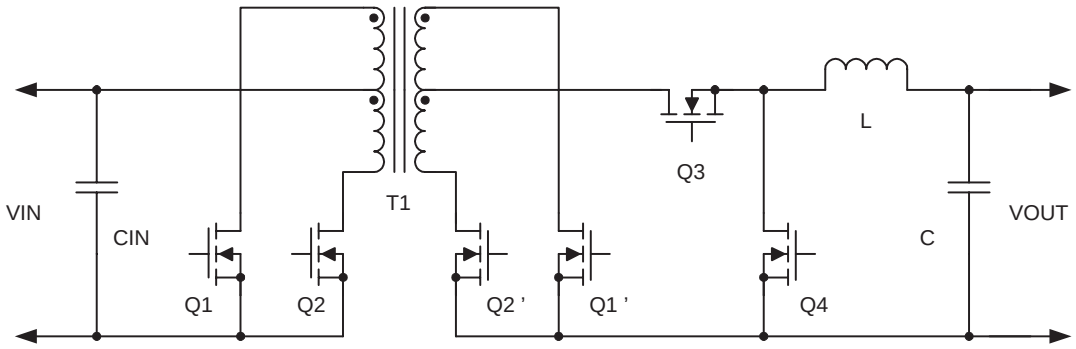

Figure 1. Push-Pull Converter Using Synchronous Rectification Followed by a Buck Regulator

3 Push-Pull Stage

The push-pull converter runs continuously at approximately a 50% to 50% duty cycle at each switch, thus using all of the available conversion cycle for processing power. A small amount of deliberate off-time (dead-time) prior to activation of the opposite switch is incorporated to facilitate lossless zero voltage switching of the primary switches, Q1 and Q2. Once a switch is turned off, the established magnetizing current of the transformer's primary inductance propels the opposite transistor's drain voltage to reach zero volts every switching cycle. The exact off-time to achieve this is determined by the circuit's stored and opposing energy requirements, as defined by the values of magnitizing current, MOSFET output capacitance, transformer and parasitic circuit capacitance, and input supply voltage. (References 3 and 4) But zero voltage switching is both achievable and incorporated to minimize primary side power loss. Voltage mode control is utilized primarily for its simplicity, accompanied by cycle-by-cycle over-current limiting protection.

On the secondary side of the transformer, note the particular detail regarding the transformer's windings and connections, especially the center-tap. The utility of this configuration is that both synchronous rectifiers are ground referenced, thus simplifying the gate drives significantly. In fact, it is possible with many low voltage outputs to use a self driven gate drive where the gates are driven straight from the opposing secondary side transformer winding output. But universally, the synchronous rectifiers Q1 and Q2 can be driven from isolated versions of the same commands to the primary side switches, Q1 and Q2. If a secondary-side referenced control circuit is used, then the opposite is also true. The primary switches Q1 and Q2 can be driven from isolated versions of the gate drives to Q1 and Q2. Since the duty cycle involved is constant, a simple transformer coupled circuit suffices for either variety. The operating waveforms for this conversion technique are shown in Figure 2.

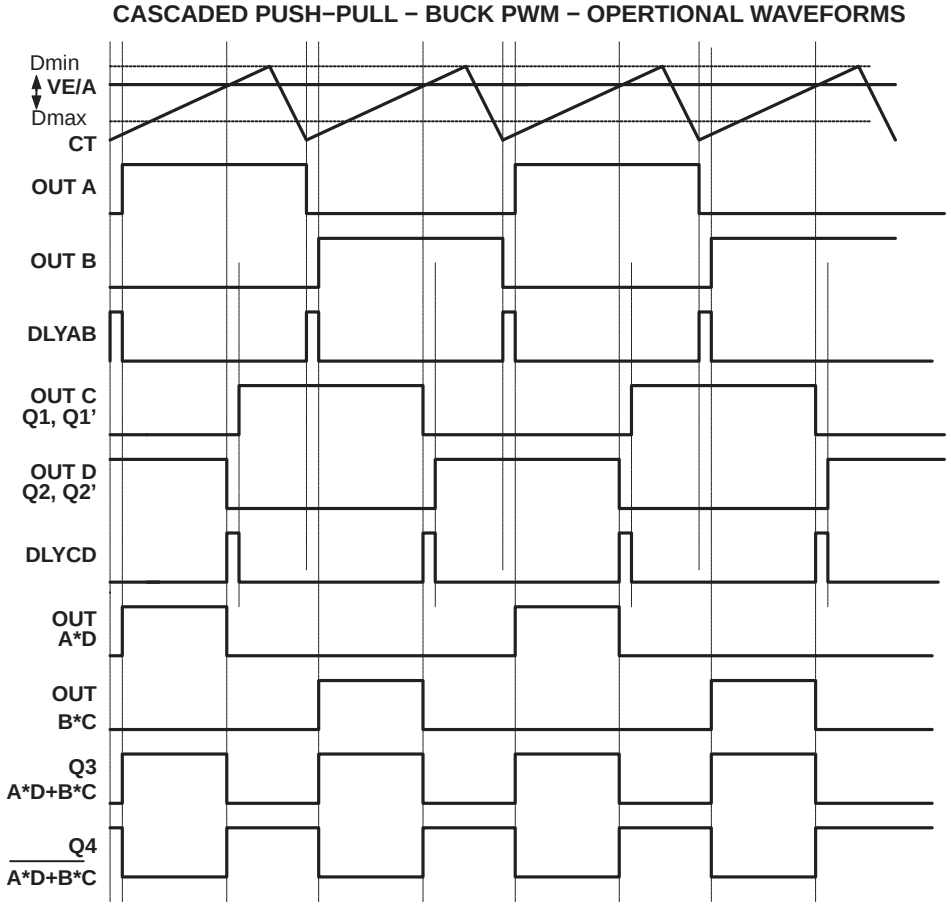

Figure 2. Operating Waveforms

4 Buck Regulator

Further differences between this cascaded adaptation and conventional approaches are evident in the buck regulator section as well. Note that there is no output filter inductor or capacitor between the secondary side of the transformer and the input to the buck regulator. Therefore, the buck stage is fed by a pulse-train comprised of the rectified secondary voltage rather than a more normal dc voltage. Although somewhat unconventional, this technique works quite advantageously, given the right control circuitry. Particular attention should be paid to the simplicity of this configuration when multiple outputs are to be generated. The transformer's turns ratio is designed to supply the secondary with the highest output voltage required. All other lower output voltages are separately derived using buck regulators from the same output node, yet no additional secondary windings, filter stages or push-pull synchronous rectifiers are required.

Combining a control strategy with low-loss switching, the buck regulator switch is driven to turn off coincidentally each switching cycle with the collapse of the rectified transformer secondary voltage. A technique known as *Leading Edge Modulation* is implemented as opposed to the traditional PWM technique of *trailing edge modulation*. Synchronization of the buck control circuit to the main converter is forced to coincide with turn-off of the push-pull converter switches. Turn-on of the buck's forward switch is near lossless due to the finite leakage inductance of the transformer's secondary winding. Extracting the buck's commutating synchronous rectifier gate drive from the PWM control circuit can be done at the gate driver devices.

5 Control Circuits

Most PWM controllers are designed to regulate a single power supply output and are therefore unlikely to house all of the decoding logic required to implement the numerous gate drive signals for this multiple output application. Any alternating, dual output PWM is configurable to address the fixed frequency, 50% to 50% duty cycle gate drives needed for the push-pull section. Popular choices are the 8-pin UCC3808A, along with several 16-pin robust choices; devices such as the UC3825A, UC3856, UCC3806 and UC3846.

Finding a synchronizeable leading edge modulation PWM for the buck regulator is more difficult. Referred to as *secondary side post regulator* controllers, two PWM devices devised specifically for this application already exist; the UCC3583 and UC3584, (see Figure 3). The uniqueness of these controllers is in their ability to perform leading edge modulation while maintaining a standard error amplifier configuration. Ideally, an increasing error voltage corresponds to an increased duty cycle; Likewise, a decreasing error voltage commands less duty cycle. To accomplish this, the internal architecture must be designed with the PWM's logic essentially reversed in comparison to standard convention. The final controller requirement is the ability to synchronize on a cycle-by-cycle basis to the trailing edge of the push-pull converter's pulse train. Any combination of PWM's from each of the push-pull and SSPR categories properly supports the overall control aspects of this novel technique.

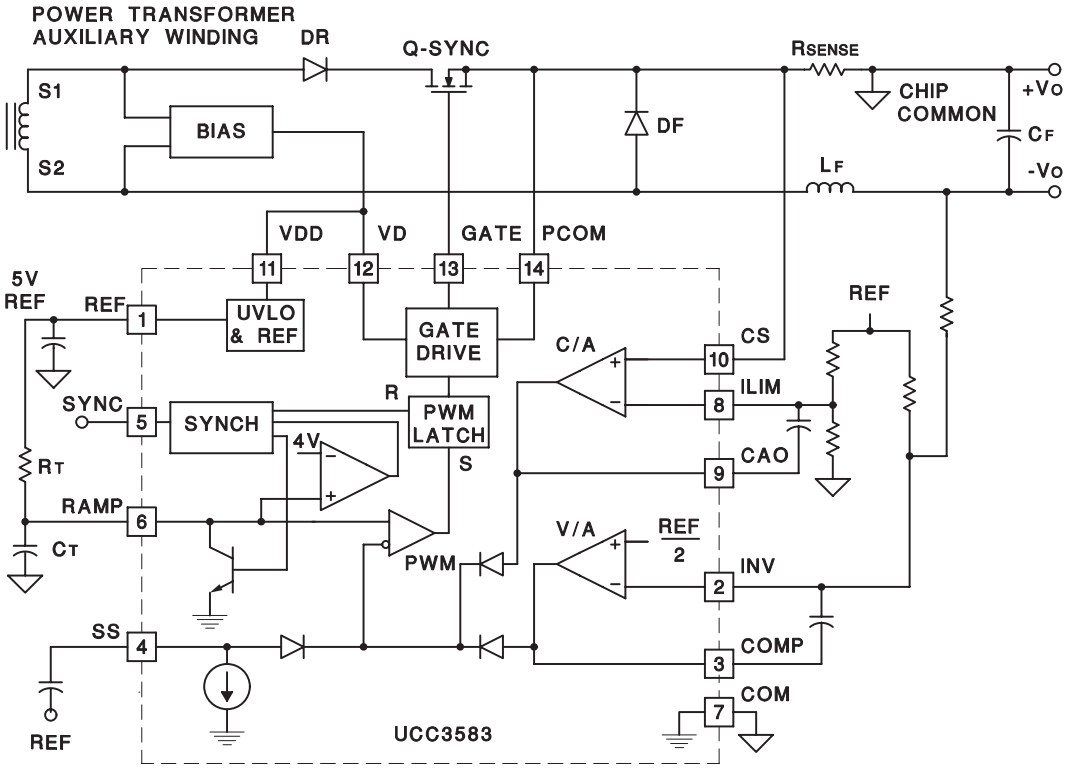

Figure 3. UCC3583 Application Diagram

A single chip PWM solution to control and drive both the push-pull and buck regulator stages does exist − the UCC3895 phase shift controller. Although intended for controlling zero voltage transition full bridge converters, the device is equally well suited for this particular application. The UCC3895 block diagram is shown in Figure 4.

The UCC3895 PWM controller features four outputs labeled A,B,C, and D arranged as two pairs (A,B and C,D) of half-bridge drivers for driving the four switches of a full bridge converter. Each output within the pairs alternately switches at approximately 50% duty cycle. A brief off-time between the transition edges is programmed via the respective DELAY SET pin to accurately match the timing requirements as dictated by the circuit parameters. The second set of half bridge drivers, outputs C and D, are phase shifted with respect to the output pair A and B. As the pulse width is commanded wider by the error amplifier output voltage, the phase shift relationship between outputs A/B and C/D is increased. This lengthens the simultaneous on-time of the diagonal switches in the full bridge converter, thus widening the delivered duty cycle to the secondary. The opposite mode of operation is also true. As the error amplifier commands a narrower duty cycle, the simultaneous on-time of the diagonal switches is reduced. True zero duty cycle through nearly 100% duty cycle is achievable.

Implementation of the control strategy incorporates a rather unorthodox use of the devices four PWM outputs to achieve the desired three commands for the push-pull and buck gate drives. Since the four device outputs are constantly switching at nearly 50% to 50% duty cycle each, obtaining the command signals for the push-pull is obvious. However, extracting the effective duty cycle for use in the buck stage signal requires minor gating of the four PWM outputs using standard digital logic gates. An interesting and useful fact is that the UCC3895's effective pulse width is trailing edge modulated with respect to outputs A and B, yet leading edge modulated with respect to outputs C and D. This feature proves to be very useful later as the multiple outputs are added.

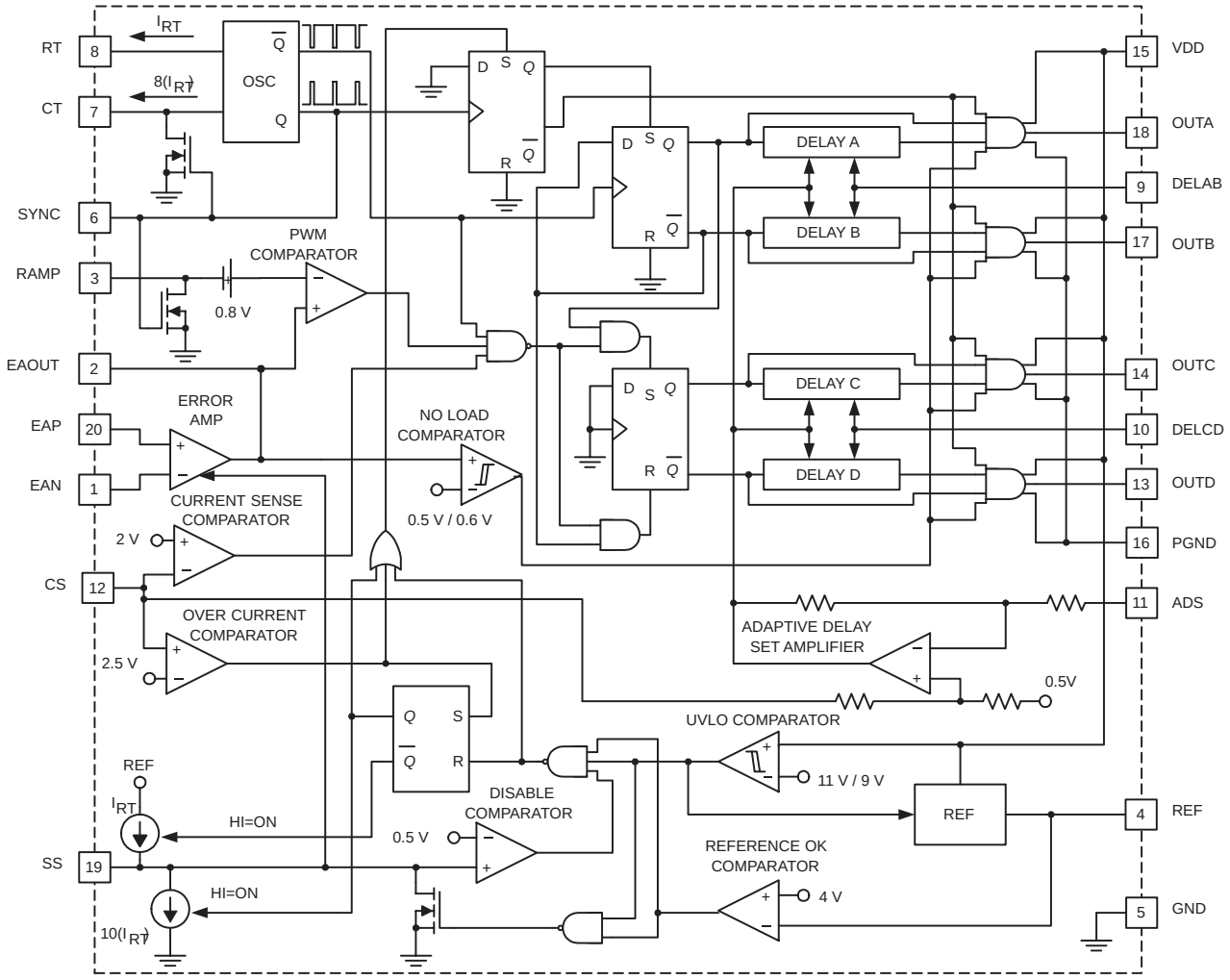

Figure 4. UCC3895 Block Diagram

The buck regulator's correct pulse width can be deciphered by logically ANDing output A with D on one clock cycle, and ANDing output B with C for the next switching cycle. These two pulse trains are logically ORd together to produce a cycle-by-cycle pulse width signal to drive the buck's switch. The free-running push-pull gate drives are obtained using the controller's outputs C and D. While outputs A and B might first seem like the more logical choice to drive the push-pull switches, they are not. In order to achieve the desired leading edge modulation of the buck regulator with respect to the push-pull converter's timing cycles, outputs C and D must be used − not outputs A and B.

The specific circuit implementation, using NAND gates instead of AND and OR logic is shown in Figure 5. This choice was swayed based upon the desire to synchronize the downstream buck controllers to the push-pull control circuit. The SYNC pulse to the buck controllers uses one less gate, hence a shorter delay to compensate for the brief synchronization delay inherent to the buck PWMs. In actual practice, the buck PWMs can be synchronized to push-pull secondary waveforms instead. But for the purpose of developing a complete control circuit for this multiple output application, a generated sync pulse is used throughout. The converter's fundamental timing waveforms are shown in Figure 6. Note that outputs A and B are not used to drive any of the switches in this application, however, they do contain vital information to generate the correct pulse width for the buck regulator.

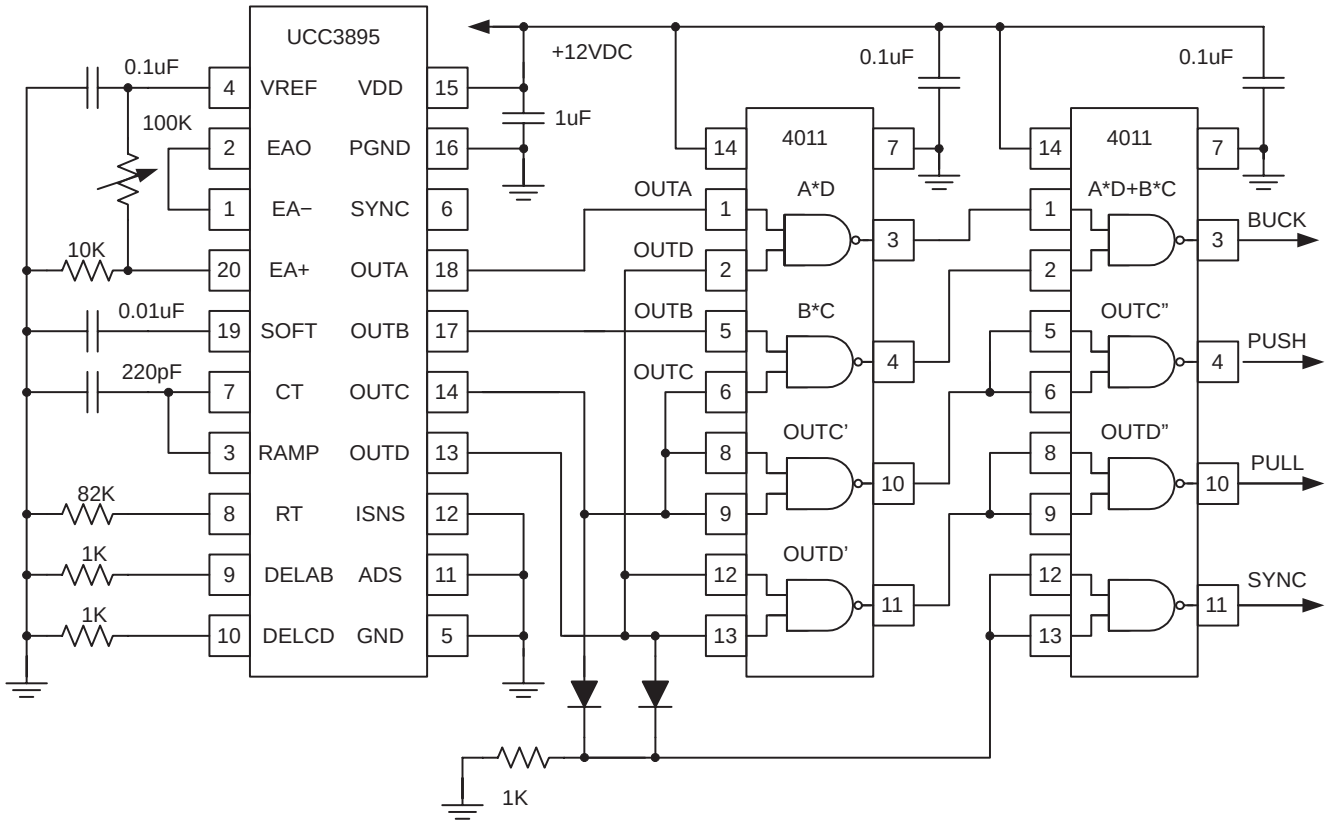

Figure 5. Circuit Implementation Using NAND Gates

FUNDAMENTAL TIMING WAVEFORM

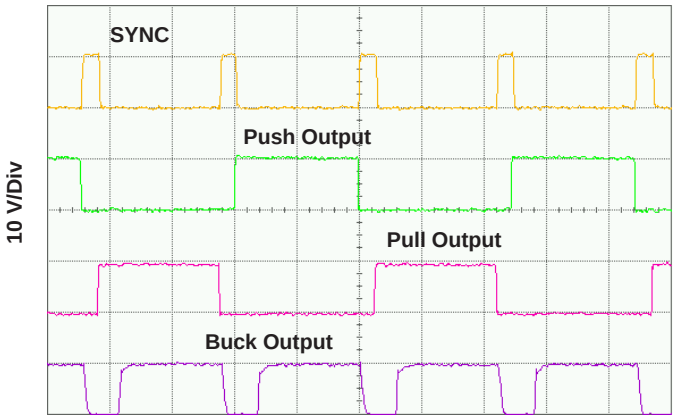

Figure 6

6 UCC3895 Controlled PWM Circuitry Summary

- All three required control and drive signals for the push-pull and main buck channels are generated using one PWM controller
- The programmable RAMP input allows for the implementation of several control strategies: voltage mode, peak current mode or average current mode control
- Programmable output delays and adaptive delay set circuits facilitate optimizing the push-pull converter's off-time to its external resonant tank parameters
- Programmable oscillator frequency with bidirectional synchronization
- Programmable soft-start and soft-stop with disable

7 Multiple Outputs

The UCC3583 secondary side PWM controllers are used to regulate all additional switch-

mode outputs. Designed exclusively for this type of application, its ease of synchronization, leading edge modulation and protection features make it a logical choice. This controller is also used in an unorthodox configuration in comparison to the example shown in its datasheet. For this application, the UCC3583 is ground referenced and the positive output supply voltage is used to achieve regulation.

The noninverting input of the devices voltage error amplifier is internally tied to one-half of the reference voltage, or 2.5 V. Also housed within the device is a programmable current amplifier that can provide an over-current limiting function. Note that the outputs of both amplifiers along with the soft-start function are essentially wired together to the PWM ramp comparator inverting input. These *ORing* diodes allow for an override of the other two inputs by any one amplifier or function commanding a narrower duty cycle. Zero duty cycle is reached with a *high* amplifier output and a full duty cycle is commanded by a *low* amplifier output. This is inverted with respect to most conventional PWMs, but the same is true for the timing capacitor waveform used as the positive input to the PWM comparator, or RAMP. The cycle begins with the capacitor charged to its upper threshold and is linearly discharged during the remainder of the switching cycle. This arrangement works well to provide the leading edge modulation required for this synchronous type of power conversion. Due to the unusual use of the UCC3583 PWM, an external operational amplifier is used simply to invert the output voltage feedback signal.

To minimize the number of passive components used, a 2.0-V reference threshold is incorporated in both the voltage feedback and over-current circuitry. Accordingly, for output voltages above 2.0 V, a simple resistor divider network from the output voltage to to ground is fed into the external error amplifier inverting input. For output voltages below 2.0 V, a resistor divider network from VOUT to the devicess reference voltage is used to increase the feedback voltage to 2.0 V. Resistor locations RV2 and RV3 get populated for outputs greater than 2.0 V, whereas resistors RV1 and RV3 are used for sub 2.0-V outputs.

The same biasing principles apply to the current amplifier used to provide over-current limiting. It has a maximum input common mode specification of 2.0 V, so resistor divider networks either to ground or VREF might be needed. This specification leds to the common 2.0-V reference threshold used. Enhanced current limiting is achieved by using a differential current sensing technique across the current sense resistor. The output voltage should be used to develop a portion of the current amplifier's voltage threshold set at ILIM. Avoid using a divider directly from VREF to ground, as this does not provide protection should the output voltage decrease − as in the case of many over-current faults. For output voltages above 2.0 V, use locations RC2 and RC3 to set the output voltage information and RC5 and RC6 as the current amplifier input for current. With output voltages below 2.0 V, use locations RC1 and RC3 to program the output voltage information and RC4 and RC6 as the input for current information. Take into account a typical input offset voltage for the current amplifier of +/− 8 mV in addition to the resistor tolerances.

Synchronization of the UCC3583 buck PWM controllers can be achieved in several ways. The simplest technique is to divide down the output of the push-pull synchronous rectifier waveform, forcing synchronization to the beginning of each switching cycle. The SYNC threshold of the device is 1 V and is triggered by a positive going signal. There is also 1-V of hysteresis in the SYNC circuit comparator, therefore, it is best to capacitively couple the synchronization stream into the pin. Since the purpose of this paper is to demonstrate the feasibility of a control strategy with hardware implementation, the synchronization pulse is developed at the UCC3895 PWM and bussed around to the UCC3583 buck PWMs instead.

The exact timing between turn-off of the buck switch and turn-on of the push-pull's next switching cycle can be precisely controlled using the UCC3895 C−D delay function. This delay circuitry actually serves three purposes in this application. First, it sets the delay time to match the resonant transitions of the push-pull gate drive to the exact resonant tank timing. Second, it defines the maximum duty cycle of the principal UCC3895 controlled buck regulator. Finally, the C−D delay function can also be used to delay the turn-on of the next push-pull switching cycle to match actual circuit and propagation delays in the UCC3583 controlled auxiliary buck regulator stages. The exact delay time to yield maximum efficiency and performance can be determined using empirical measurements of the buck gate drive and drain current.

8 Synchronous Buck Applications

Higher efficiency multiple outputs can be obtained by converting the buck regulator power stages to incorporate synchronous rectification. High current gate drive devices with internal decoding logic are available to drive both switches from a single input, such as the TPS2813 dual complementary driver. Featuring a peak output current of 2 A, this device also has crisp transitions of 15 nanoseconds and brief propagation delays of 25 nanoseconds. This driver is used for each of the buck regulator power stages.

Proper signal timing is critical, especially in synchronous rectifier drive applications. There should be no overlap between the complementary gate drives, and sufficient time should be made for complete removal of the gate charge before the opposing synchronous switch is activated. This can be implemented by adding a delay to the turn-on of each switch. However, in this zero voltage switching application, the bigger concern is turning on the forward buck switch before the commutating switch channel is fully turned off. One implementation is to add a brief delay to the turn-on of the forward buck switch only. A 68 nanosecond time constant is arbitrarily chosen for this example, and a series resistor-capacitor network of 68 pF and 1 kΩ between the UCC3583 output and the TPS2813 gate driver device is inserted. To keep this delay from affecting the quick turnoff of the forward buck switch, a diode is placed in parallel with the resistor, and no delay is added to the turn-off command. This 68-ns time constant is used initially for each buck regulator's gate drive, and can later be optimized based on empirical results and efficiency measurements. The associated waveforms are shown in Figure 7 for the second buck output and the delay shown is applicable to output 3 as well.

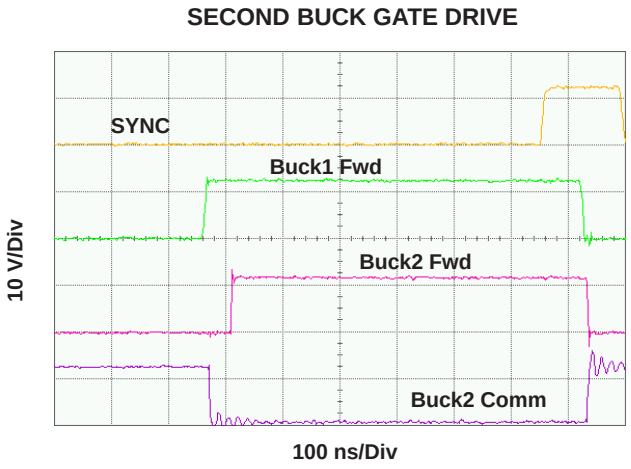

Figure 7

The complete circuit schematic of the buck stages, gating logic and driver devices is shown in Figure 8. The three buck regulators, operating at different duty cycles corresponding to different output voltages are shown in Figure 9. Figure 10 demonstrates the second and third buck stages' ability to fully maintain regulation with the main buck running at zero duty cycle.

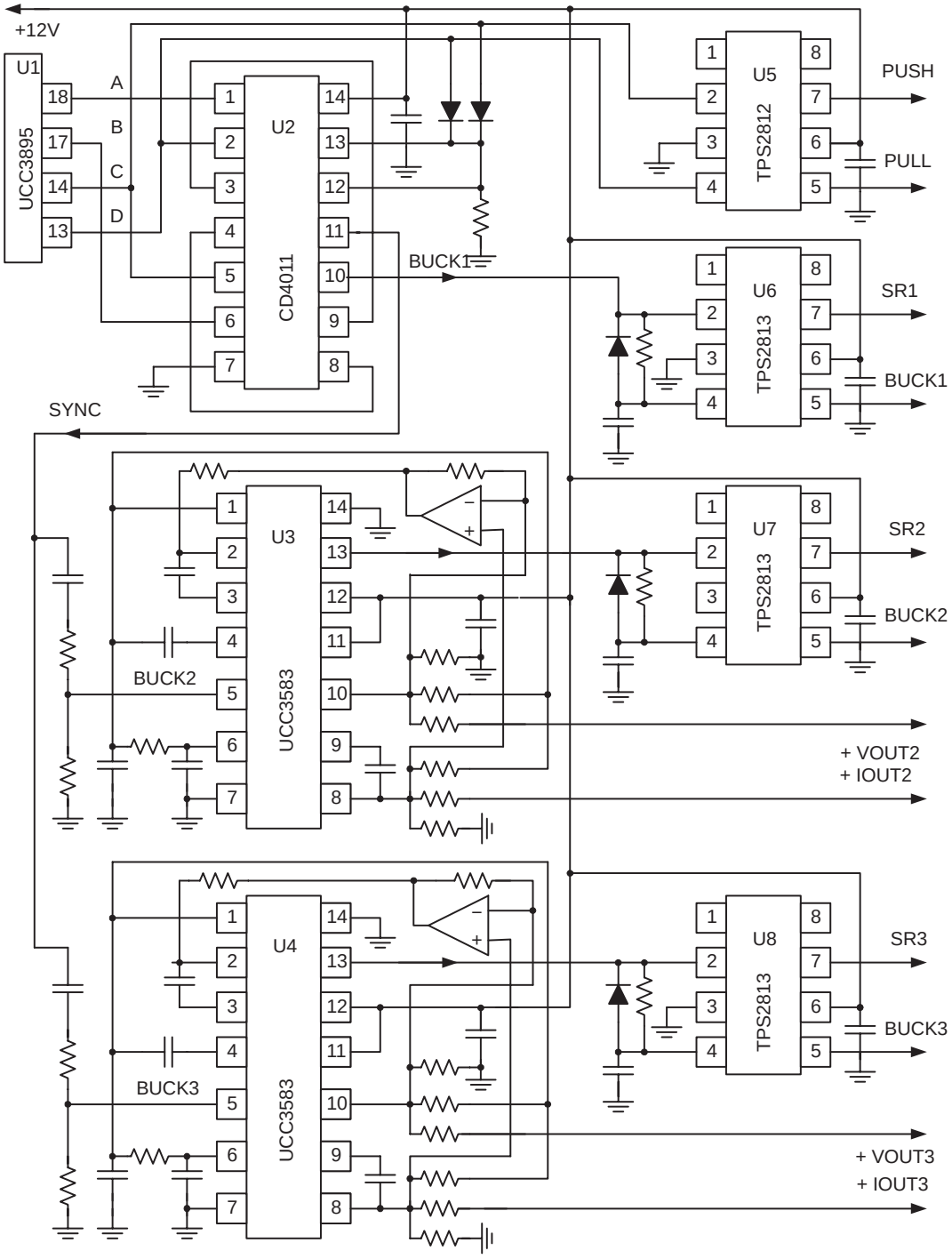

Figure 8. Circuit Schematic

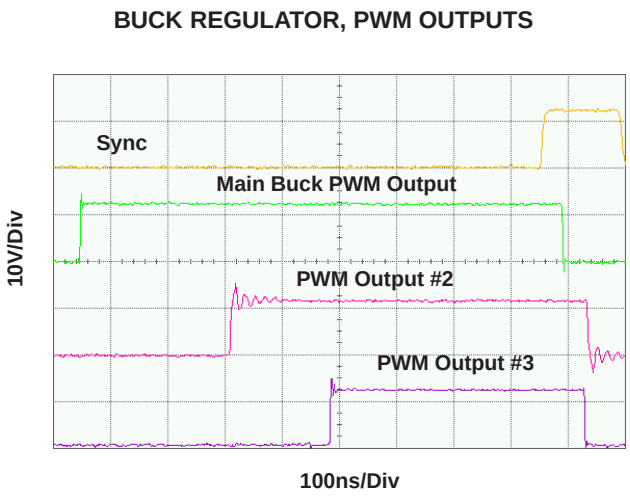

Figure 9

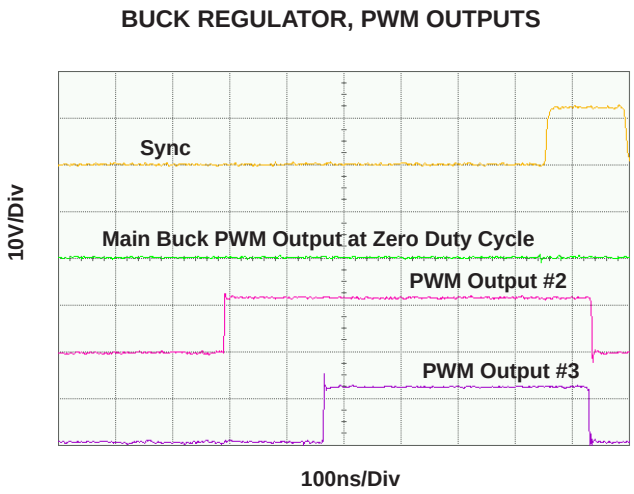

Figure 10

9 Summary

A unique power stage implementation with PWM control techniques for demanding multiple output converters has been demonstrated. Previous design efforts of an isolated 48-V to 1.5-V at 20-A single output version of this technique resulted in an overall efficiency of 80.5% at half load and 78% at full load while operating at 500 kHz. Future development using this control strategy includes the design of a 48-V input to three low-voltage output converter.

10 References

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