Application Report
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Varying UCC27221 and UCC27222 Gate Drive Voltage by Overriding the VLO Regulator

Steve Mappus
Power Supply Control Products

ABSTRACT

The UCC2722x contains an internal 6.5-V regulator, from which the gate drive voltages for the high and low-side MOSFETs of a synchronous buck power stage are derived. In some instances it may be desirable to drive the MOSFET gates with a voltage other than 6.5 V. The output driver stage of the UCC2722x has an absolute maximum voltage rating of 10 V. However it is still possible to bypass the internal regulator and produce gate drive voltages other than 6.5 V, but limited to 9 V.

Contents

1 Introduction

Synchronous rectifiers are often used in place of the freewheeling diode commonly found in a classical buck converter. Using a synchronous buck driver that includes Predictive Gate Drive™ technology to drive the upper control MOSFET and lower synchronous MOSFET, can result in a substantial overall efficiency increase for high-frequency, low-voltage applications. While most of the efficiency savings is attributed to the non-existence of body-diode conduction, additional increases can sometimes be gained by properly matching the optimal gate drive voltage with the MOSFETs being driven. Driving the MOSFET gate with a higher voltage, results in a lower associated on-resistance, $R_{DS(on)}$. There are however, additional factors such as gate charge losses and switching losses that must also be considered. Lowering the MOSFET on-resistance is especially critical for the synchronous rectifier, since in most cases the power loss due to the freewheeling current through the MOSFET channel resistance is the highest single contributor to total power dissipated within the synchronous rectifier.

2 Inside the UCC2722x

As shown in Figure 1, the UCC27222 contains an internal 6.5 V regulator designated as VLO, and is available externally on pin 4. Externally connecting VLO (pin 4), to PVLO (pin 5), directly provides the 6.5-V drive voltage needed for the G2, synchronous rectifier output. Also, the VHI (pin 14) floating supply voltage necessary to drive the G1, control MOSFET is normally derived from VLO/PVLO.

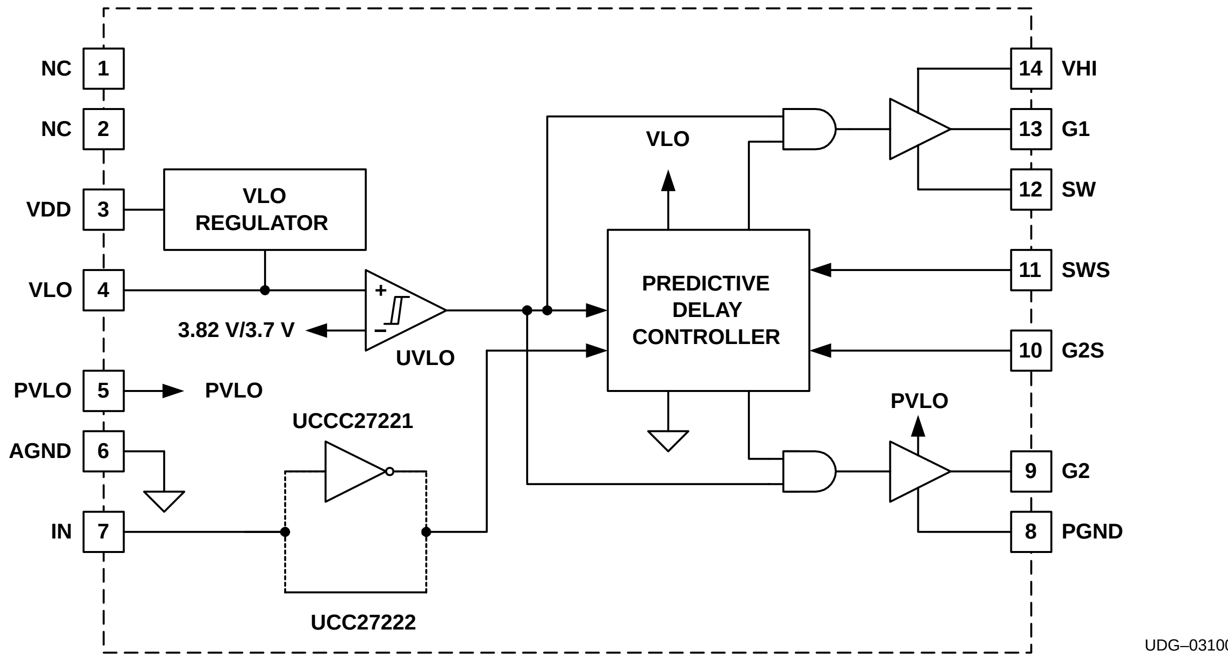

Figure 1. Simplified Block Diagram

3 Recommended VLO/PVLO Configuration

Configuring the UCC27222 VLO/PVLO drive as recommended in the data sheet makes 6.5V available for driving both gates of the synchronous buck. A typical application example is shown in Figure 2.

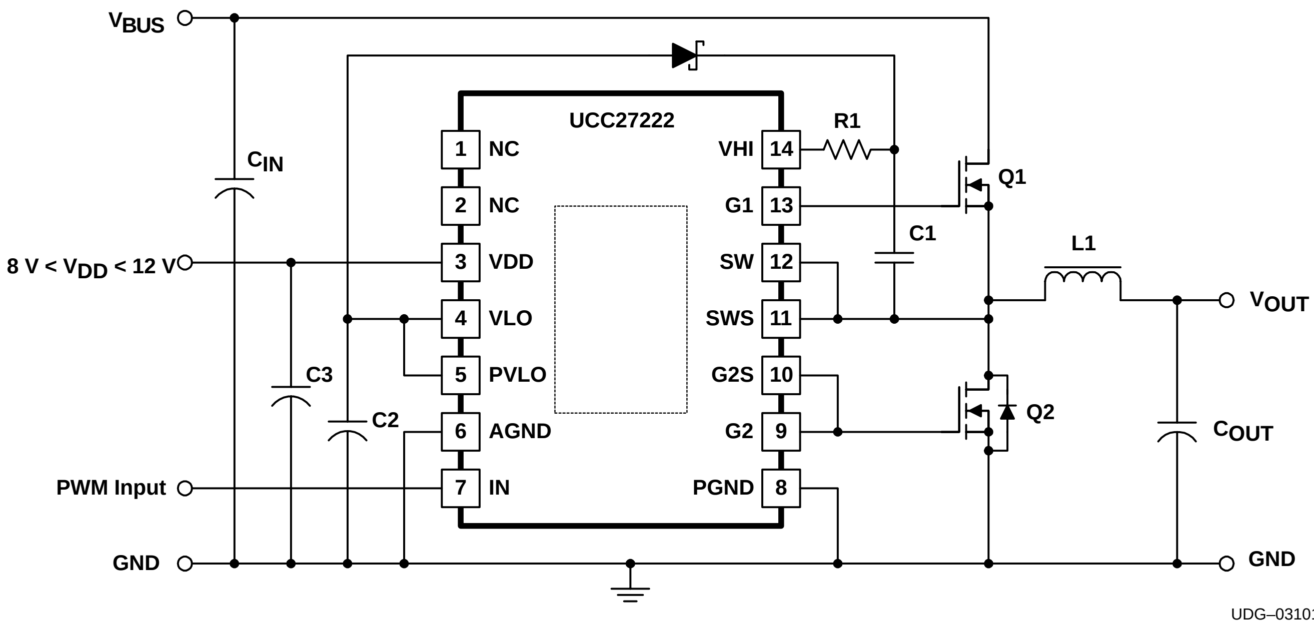

Figure 2. Gate Voltage Provided From VLO/PVLO

6.5 V was chosen as an optimal voltage for driving logic level MOSFETs typically found in most synchronous low-voltage, buck power stages. As the gate voltage is increased the on resistance of the MOSFET decreases. However, the trade-off lies in the fact that as the gate voltage increases, the associated gate charge also increases. Higher gate charge and gate drive voltage results in increased switching losses and losses in the UCC2722x driver device. By numerically characterizing gate voltage versus charge and gate voltage versus on resistance, the optimal gate drive voltage was found to be 6.5 V and so became the defined voltage for the VLO regulator.

4 Driving PVLO and VHI With External Voltage Sources

In some instances it may be desirable to drive the MOSFETs with a voltage either higher or lower than VLO. However, the output drive stage of the UCC2722x, has an absolute maximum voltage limit of 10 V. For applications desiring a gate drive other than 6.5 V, the UCC2722x can be configured as shown in Figure 3.

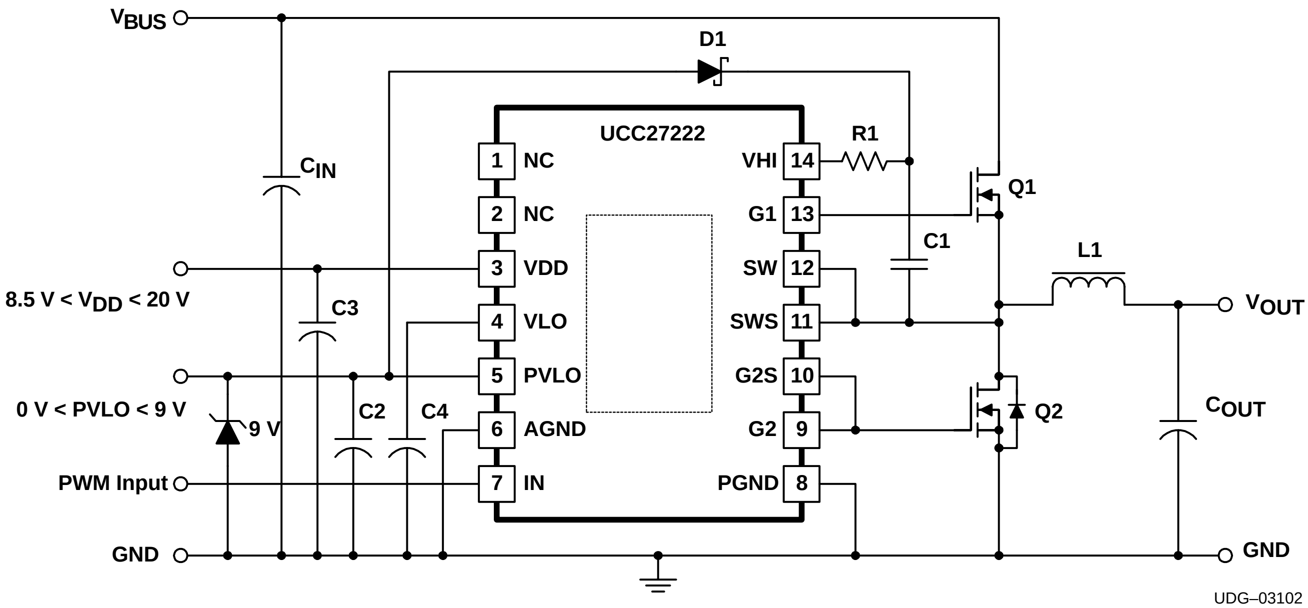

Figure 3. PVLO and VHI Gate Voltage Provided From External Sources

For the application circuit shown in Figure 3, the PVLO voltage is supplied by some other available bias source up to 9 V. To prevent possible damage to the output stage of the UCC2722x, It is advisable to clamp the PVLO voltage with a 9-V zener diode, as shown in Figure 3. For this configuration, the VLO regulator output is now used strictly for biasing the predictive delay control circuitry internal to the device, while PVLO provides the necessary gate drive voltage for G1 and G2.

5 Driving PVLO and VHI With Independent External Voltage Sources

To drive the gates of Q1 and Q2 using different gate drive voltages, the UCC2722x can be configured as shown in Figure 4.

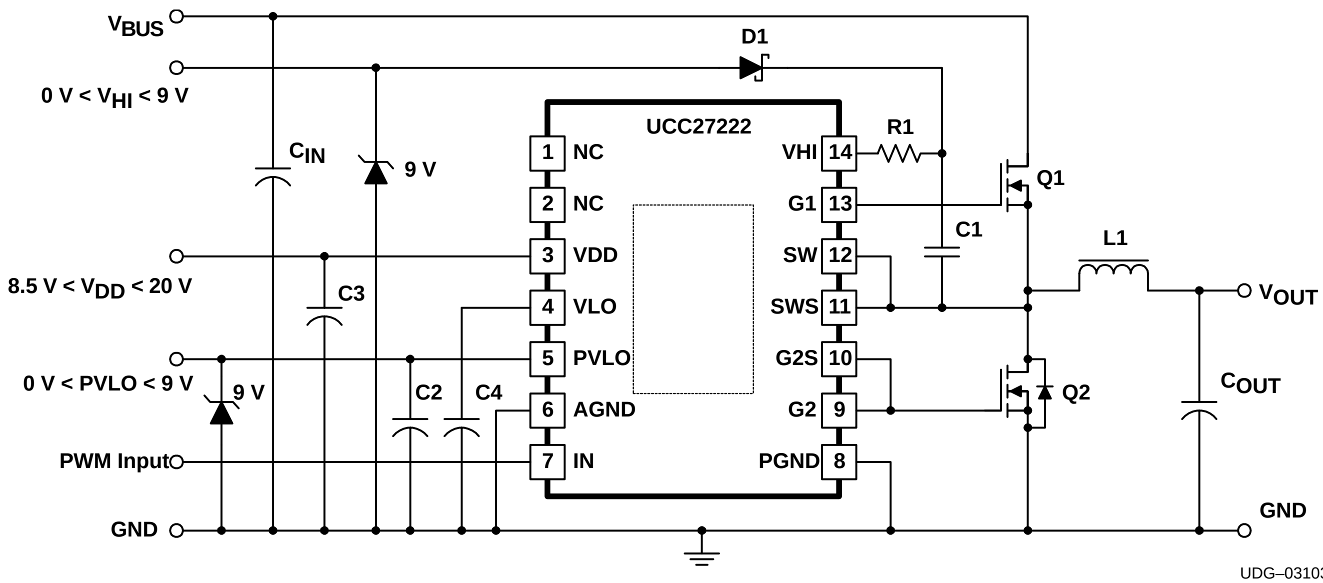

Figure 4. PVLO and VHI Gate Voltage Provided From Independent Sources

Similar to the application circuit shown in Figure 3, it is recommended to clamp VHI and PVLO voltage sources with a 9-V zener protection diode. VHI is now boosted to a voltage equal to VHI above V_{BUS} making the gate to source voltage to Q1 equal to VHI minus the diode drop associate with D1. For the low-side MOSFET, the gate to source voltage of Q1 is now provided directly from the external PVLO voltage source.

6 Conclusion

For most applications where the UCC2722/1/2 is used to drive low voltage, logic level MOSFETs, 6.5 V should be very close to an optimal gate drive voltage amplitude. However, if system voltages other than 6.5 V are readily available, and the $R_{DS(on)}$ of the synchronous MOSFET can be lowered enough to offset the additional gate charge loss introduced by increasing the gate drive voltage amplitude, then there may be some cases that would benefit from using the application circuits introduced in Figure 3 or Figure 4.

7 References

UCC27221/UCC27222 High-Efficiency Predictive Synchronous Buck Driver Datasheet, (SLUS486A)

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