

## ABSTRACT

This application report describes how to use an external circuit to improve the soft-start performance of the [UCC28060](#) and [UCC28061](#) PFC controllers. Using a soft-start circuit can reduce a large start-up current and decrease the PFC output overshoot voltage.

## 1 Introduction

With its advantages of high efficiency, low ripple, and good electromagnetic interference (EMI) performance, the UCC28060 and UCC28061 (UCC2806x) interleaved power factor correction (PFC) controllers are well received by many customers. However, if the start-up current is too large, the power supply can easily go into fault protection, or even be damaged. Additionally, the PFC output voltage should be a small overshoot voltage to improve the safety of the switch components and the downturn dc/dc converter circuits.

In order to maintain a low overall cost and reduce the number of interconnections, the UCC2806x has no soft-start (SS) pin. As a result, the UCC2806x typically uses a voltage-loop compensation circuit for device start-up. As a result, there is a tradeoff between the loop stability and using the soft-start technique in the usual manner.

## 2 Theory of UCC2806x Operation

The UCC2806x contains the control circuits for two boost pulse-width modulation (PWM) power converters. The boost PWM power converters ramp current in the boost inductors for a time period proportional to the voltage on the error amplifier output. Each power converter then turns off the power MOSFET until current in the boost inductor decays to 0, as sensed on the zero current detection inputs (ZCD<sub>A</sub> and ZCD<sub>B</sub>). Once the inductor current decays to 0, the power converter starts another cycle. This on/off cycling produces a triangular current wave, with the peak current set by the on-time and the main power input voltage, as shown in [Equation 1](#).

$$I_{\text{PEAK}}(t) = \frac{V_{\text{INAC}}(t) \cdot T_{\text{ON}}}{L} \quad (1)$$

The average line current is exactly equal to half of the peak line current, as shown by [Equation 2](#).

$$I_{\text{AVG}}(t) = \frac{V_{\text{INAC}}(t) \cdot T_{\text{ON}}}{2 \cdot L} \quad (2)$$

With  $T_{\text{ON}}$  and  $L$  essentially staying constant during an ac line period, the resulting triangular current waveform during each switching cycle has an average value that is proportional to the instantaneous value of the rectified ac line voltage. This architecture, in turn, results in a resistive input impedance characteristic at the line frequency and a near-unity power factor.

The outputs of the two PWMs operate 180° out-of-phase so that the power-line ripple current for the two PWMs is greatly reduced from the ripple current of each individual PWM. This design reduces ripple current at the input and output, and allows a noticeable reduction in both size and cost of input and output filters.

## 2.1 Theory of On-Time Control of UCC2806x

Gate drive on-time varies with the error amplifier output voltage by a factor called  $K_T$ , as shown in Equation 3.

$$T_{ON} = K_T(V_{COMP} - 125 \text{ mV}) \quad (3)$$

Where:

$V_{COMP}$  is the output of the error amplifier, and 125 mV is a modulator offset.

For a given  $K_T$ , from Equation 3, we can see that the gate drive on-time only varies with the voltage of the COMP pin.

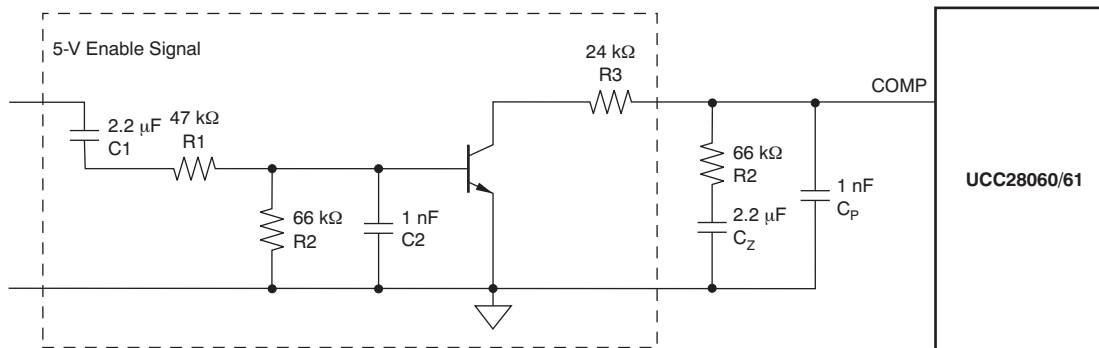
## 2.2 UCC2806x Soft-Start

The PWM gradually ramps from zero on-time to normal on-time as the compensation capacitor from COMP to AGND charges from a low level to the final value. This process implements a soft-start technique, with a time constant set by the output current of the error amplifier and the value of the compensation capacitors.

Using this description, the soft-start circuit will both use and be limited by the voltage compensation circuit if there is no external soft-start circuit available. If the circuit meets the soft-start requirement, it may possibly result in worse loop stability and increased audible noise. On the other hand, if the circuit meets the loop stability requirement, it may produce a greater startup current and higher overshoot voltage.

## 2.3 External Soft-Start Circuit for UCC2806x

To secure the stability of the PFC converter, we can easily change the soft-start circuit in order to reduce startup current and decrease the startup overshoot voltage by adding the external circuit, as Figure 1 illustrates.



**Figure 1. External Soft-Start Circuit Configuration with UCC2806x**

When the PFC Enable signal goes from low to high, the current will charge capacitor  $C_1$  through  $R_1$ ,  $R_2$ ,  $C_2$ , and  $Q_1$ . Note that capacitor  $C_2$  is much smaller than  $C_1$ ; it is only used to filter the noise. The voltage across  $C_1$  will increase from zero to the high level of the Enable signal while the voltage across the  $R_2$  will decrease from a high divide voltage to zero during the charging time. When the divider voltage across resistor  $R_2$  is greater than the threshold of the  $Q_1$  turn-on voltage,  $Q_1$  will operate normally.  $R_3$  will divide the COMP source current during the  $Q_1$  on-time so that the COMP voltage will increase slowly. From Equation 3, the  $T_{ON}$  is increased slowly as the COMP voltage also increases. Thus, the output power will be increased slowly. This approach results in a lower start-up current and lower output overshoot voltage.

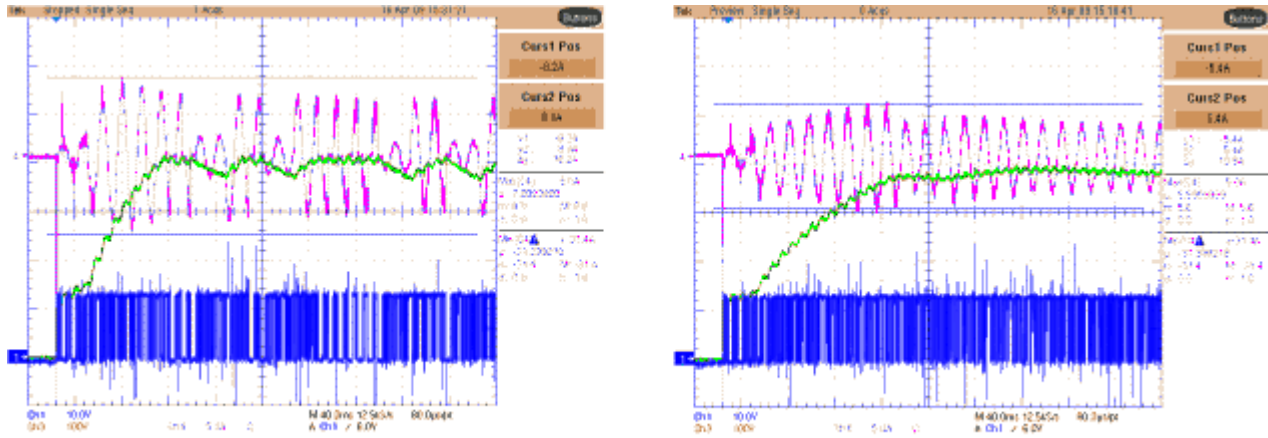
If we define the input voltage of the Enable signal ( $V_{CC}$ ) as  $V_S$ , and the minimum voltage to make the  $Q_1$  conduct as  $V_T$ , then the external soft-start time can be calculated as shown in Equation 4.

$$t_s = (R_1 + R_2) \cdot C_1 \cdot \ln \left[ \frac{R_2 V_S}{(R_1 + R_2) \cdot V_T} \right] \quad (4)$$

For example, refer to [Figure 1](#); here,  $V_S = 5\text{ V}$ ,  $C_1 = 2.2\ \mu\text{F}$ ,  $R_1 = 47\ \text{k}\Omega$ ,  $R_2 = 66\ \text{k}\Omega$ , and  $V_T = 0.6\ \text{V}$ . We can then calculate the added external soft-start time from [Equation 4](#) to be approximately 393 ms.

After the soft-start, the voltage across  $C_1$  is the same as the enable voltage, while the voltage across  $R_2$  will be 0 V.  $Q_1$  will be turned off.  $R_3$  will not work after the soft-start process ends. So the voltage-loop compensation circuit is only  $R_Z$ ,  $C_Z$ , and  $C_P$ . The stability of the PFC converter will not be affected by the external soft-start circuit when the start-up has finished.

[Figure 2a](#) is the start-up waveform of the UCC28060EVM at 90-V ac input (the input power is 220 W) without using an external soft-start circuit. [Figure 2b](#) shows the start-up waveform of the UCC28060EVM after adding an external soft-start circuit (again, the input power is 220 W). For both images, Ch1 is the PWM drive out waveform; Ch3 is the PFC output waveform; and Ch4 is the input current waveform.



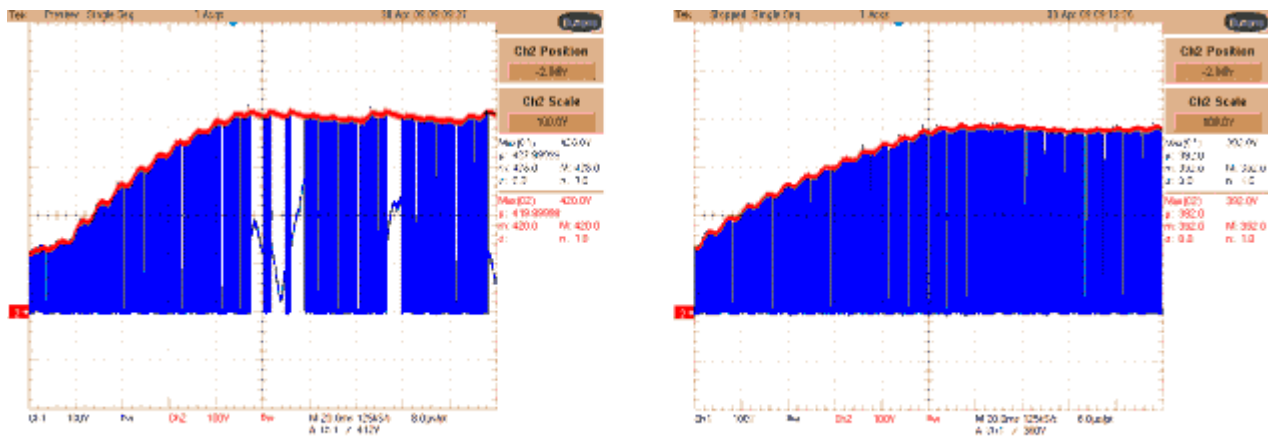
a) No external soft-start

b) With external soft-start

**Figure 2. External Soft-Start Waveforms: Start-Up at 90-V Input**

We can find that the maximum input current is approximately 16.2 A if there is no external soft-start circuit, while the maximum input current drops to approximately 10.8 A if an external soft-start circuit is added. The lower input start-up current enables the use of cheaper input/output filters and less expensive switching components, while offering better EMI performance and improved safety.

[Figure 3a](#) shows the PFC output waveform of the UCC28060EVM at 90-V ac input (the output current is 0.32 A). [Figure 3b](#) presents the PFC output waveform of the UCC28060EVM with the external soft-start circuit from [Figure 1](#) at 90-V ac input (again, the output current is 0.32 A). For both images, Ch1 is the  $V_{DS}$  waveform of the MOSFET, and Ch2 is the PFC output waveform.



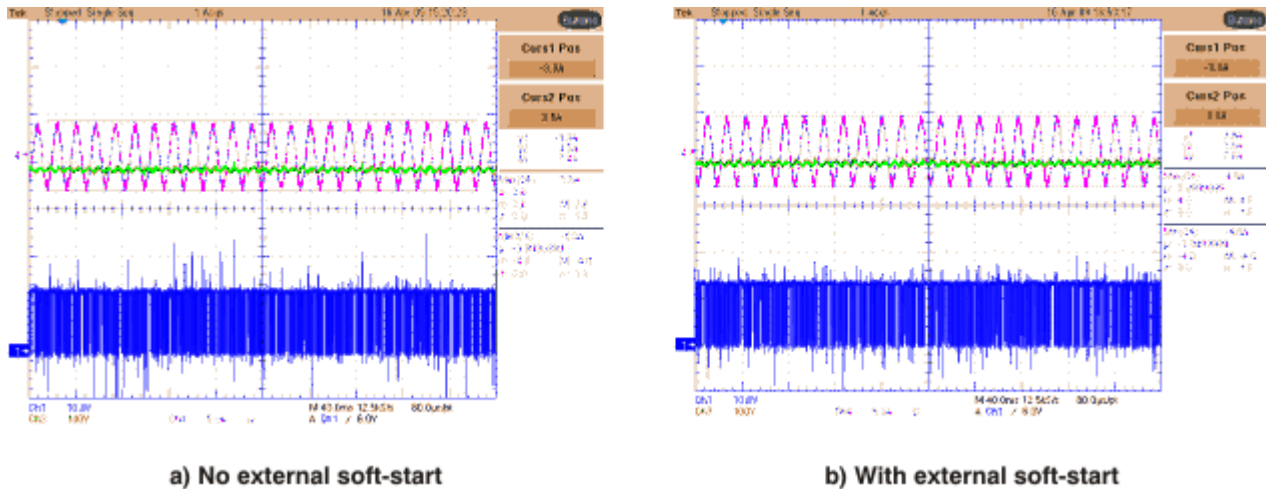
a) No external soft-start

b) With external soft-start

**Figure 3. PFC Output Waveforms at 90-V AC Input**

From these demonstrations and the above discussion, we can show that the maximum overshoot voltage is approximately 428 V, and the converter will easily go into overvoltage protection if there is no external soft-start circuit used. If the external soft-start circuit from [Figure 1](#) is included, the maximum overshoot voltage is approximately 392 V, and the converter is stable. There will be a 36-V overshoot voltage gap between the two examples (that is, with and without the soft-start circuit).

[Figure 4a](#) shows the waveform of the UCC28060EVM after start-up at 90-V ac input (again, the input power is 220 W). [Figure 4b](#) shows the waveform of the UCC28060EVM with the addition of the external soft-start circuit. For both waveforms, Ch1 is the PWM drive out waveform; Ch3 is the PFC output waveform; and Ch4 is the input current waveform.



**Figure 4. Normal Operation for Soft-Start Circuit at 90-V AC Input**

From this example, we can conclude that the waveform of a circuit with no external soft-start and the waveform of a circuit with external soft-start are very similar when both circuits are operating in a normal state. In other words, the external soft-start circuit will not affect the loop stability of the PFC converter when the PFC converter goes into normal operating mode.

### 3 Summary

Because of lower-cost components, improved safety, and better EMI performance, many applications require a low input start-up current and a low PFC output overshoot voltage. Both theory and testing verified that an external soft-start circuit can be used to successfully reduce the start-up input current and decrease the overshoot voltage without causing poorer loop stability.

### 4 References

Unless otherwise noted, all documents are available for download at [www.ti.com](http://www.ti.com).

1. UCC28060 product data sheet from Texas Instruments ([SLUS767E](#)).
2. UCC28061 product data sheet from Texas Instruments ([SLUS837A](#)).
3. UCC28060 300-W Interleaved PFC Pre-Regulator User Guide ([SLUU280B](#)).
4. UCC28061 300-W Interleaved PFC Pre-Regulator User Guide ([SLUU316](#)).

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