Application Report

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Synchronizing Three or More UCC28950 Phase-Shifted, Full-Bridge Controllers

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High-Performance Isolated Power

ABSTRACT

One of the key features of the UCC28950 phase-shifted, full-bridge controller is its ability to synchronize its main oscillator to an external clock source. In this way, multiple controllers can be synchronized to improve performance criteria of the end power supply. This application report expands the details of the synchronization capability of the UCC28950, provides examples of simple circuits used to generate the proper clock inputs to the UCC28950, and gives examples of the input and output signaling that can be expected with three- and four-phase applications.

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1 Introduction

Synchronization serves several purposes in electronics power supplies. These include lowering EMI, simplifying the filtering, allowing for smaller and less expensive components by using offset phases to lower the input current, and lowering the output ripple voltage for an equivalent power stage through ripple current cancellation. This application report explains and characterizes the synchronization capability of the Texas Instruments UCC28950 phase-shifted, full-bridge controller and provides two examples with three and four control cards.

The UCC28950 employs a synchronization capability through the use of its SYNC pin. As such, in two-phase architectures one UCC28950 controller is configured as the master and the other UCC28950 controller is configured as the slave. For the master, the SYNC pin serves as an output pin, and for the slave it serves as an input. In this configuration, the output of the master is 90 degrees phase-shifted from the output of the slave. Note that the synchronization discussion throughout this document is about the phase-adjusting/shifting of the main clock of a single UCC28950 controller relative to another UCC28950 controller. This is not to be confused with the phase-shifting between the individual output signals of a single UCC28950 as part of its internal logic.

This concept is expanded when discussing three or more UCC28950 phases that must be synchronized. In this case, the master clock must be generated from separate logic such as a *TLC555* timer configured in astable mode or with a microcontroller, (such as an *MSP430*). This clock, used with a serial-in/parallel-out shift register such as a *CD4015*, (shown in Figure 9), can be used to generate all the input SYNC signals needed. With this master clock available, the three or more UCC28950 controllers are all configured as slaves with a certain phase-adjustment among them and then otherwise be used similarly to a two-supply system. One thing to note is that the UCC28950 does not have a load-sharing control capability; so, for certain applications it may be beneficial to consider using a discrete load-share controller such as the *UCC39002* with the UCC28950 supplies.

2 Characteristics of the SYNC Capability in the UCC28950

For the testing discussed in this document, the following equipment was used:

Equipment:

1. Oscilloscope: Tektronix TDS3054 at full BW of 500 MHz
2. Function Generator: Tektronix AFG3102 (5-ns leading and trailing edge rates for signal to SYNC)
3. Scope Probes: Tek5050, 500 MHz, 11.1 pF, 10 MΩ, 10X

Before attempting to synchronize the UCC28950, read the Synchronization section in the UCC28950 data sheet (SLUSAG4). To set the UCC28950 in slave mode, connect the RT resistor between the RT pin and GND, and place an 825-kΩ resistor from the SS_EN pin and GND.

The following specifications serve as a guideline for using the UCC28950 as slaves driven by an external signal.

When synchronizing from an external clock, all controllers must be configured as slaves:

SYNC Input: CMOS logic gate supplied by internal Vref = 5 V
SYNC Input Thresholds:

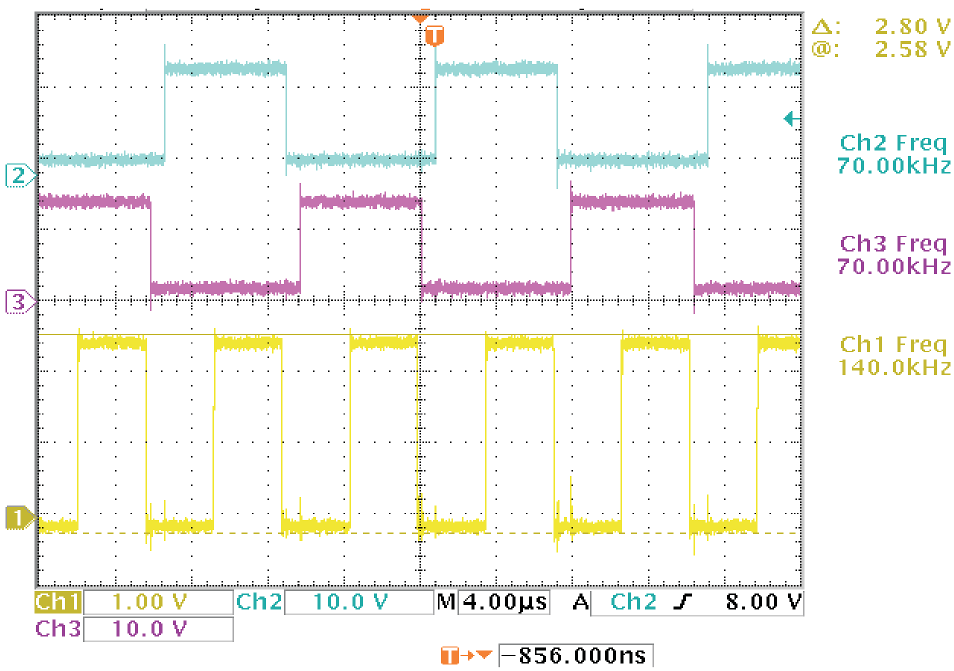
SYNC_in_H min: 2.8 V
SYNC_in_H max: 5 V
SYNC_in_L max: 1.75 V
SYNC_in_L min: 0 V

SYNC Input Impedance: 500 kΩ (nominal)
SYNC Input Rise and Fall Times: <50 ns
SYNC Input Frequency: >1.8X the converter output frequency
SYNC Input Pulse Width: >300 ns

2.1 Minimum SYNC_IN Frequency

With the controller set in slave mode, note that for proper operation, the frequency of the signal to the SYNC input pin must be greater than or equal to 1.8 times the converter frequency of the slave itself that is set by the RT resistor. (Note that the converter frequency of the UCC28950 is equal to the frequency of its output pulses.)

For the UCC28950 control card used, the RT resistor is 43.2 kΩ + 51 kΩ = 94.2 kΩ, which results in a free-running converter output frequency of ~80 kHz. For synchronization purposes, that means that the signal coming into the slave's SYNC pin must be greater than 1.8 × 80 kHz = 144 kHz. This is verified in Figure 1, where the 50% duty-cycle SYNC signal is 140 kHz and is the lowest frequency (at ~2.8-V amplitude) before the UCC28950 becomes unsynchronized and runs freely at the converter frequency set by the RT resistor. Recall that for a given input signal above the required minimum frequency, the frequency of this input signal is twice that of the converter output frequency.



Ch. 1: Input to SYNC pin of slave UCC28950 (originating from function generator)
Ch. 2: J8 connector on UCC28950 control board = OUTA signal of IC
Ch. 3: J9 connector on UCC28950 control board = OUTB signal of IC

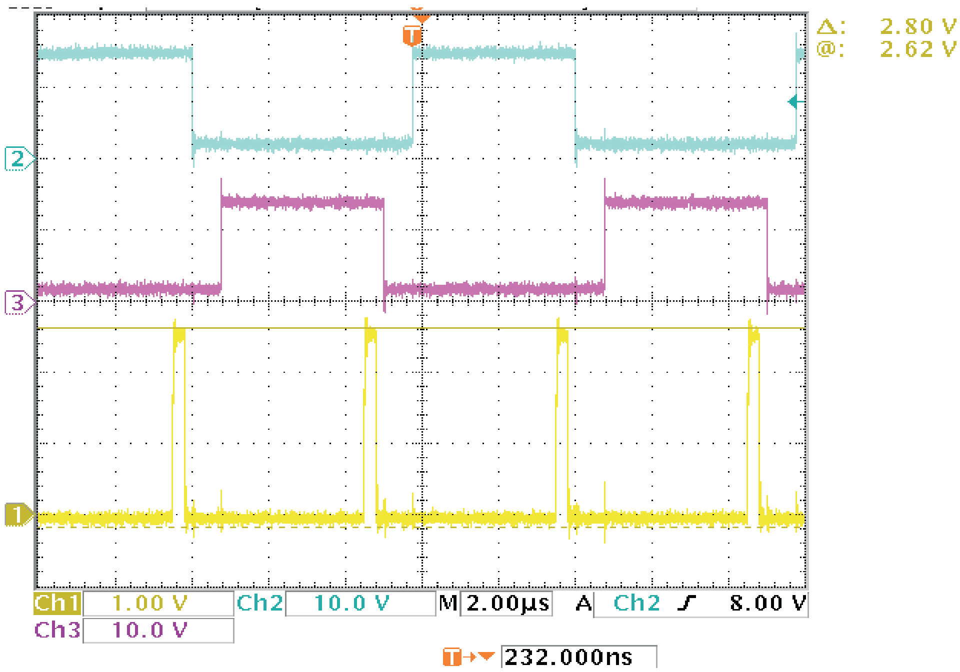
Figure 1. Minimum SYNC Frequency

Although the measurement shown in Figure 1 is at a nominal 12-V input, the minimum frequency for the chosen RT resistance holds true for a 8-V to 17-V input as well.

NOTE: For detailed SYNC_IN timing diagrams for comparison, see Figure 18 and Figure 19 in the UCC28950 (SLUSAG4) data sheet. In those figures, note the slight delay between the falling edge of the SYNC signal and the rising edge of the respective output. This is due to the internal oscillator delay.

2.2 Minimum SYNC_IN Amplitude

Although the maximum voltage of the SYNC pin is listed in the UCC28950 data sheet, the minimum amplitude threshold for synchronizing is examined further in this document. With a 8-V to 17-V input, a 200-kHz to 600-kHz function generator frequency (100-kHz to 300-kHz converter frequency), and with a 300-ns pulse width, you can see in Figure 2 that for this example and operating conditions, the input signal to SYNC must be at least 2.8 V.

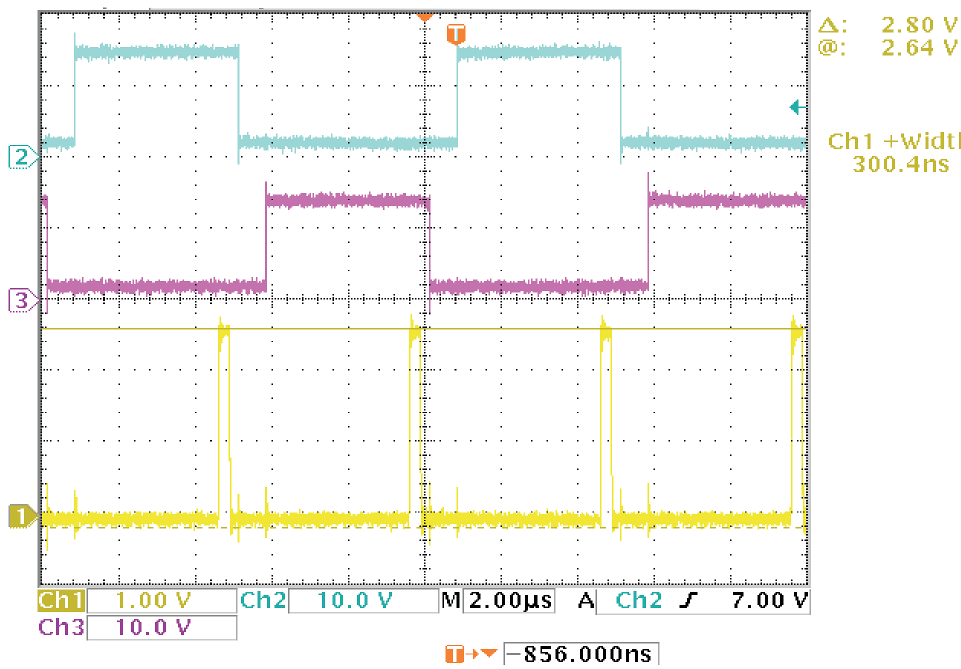


Ch. 1: Input to SYNC pin of slave UCC28950 (originating from function generator)
Ch. 2: J8 connector on UCC28950 control board = OUTA signal of IC
Ch. 3: J9 connector on UCC28950 control board = OUTB signal of IC

Figure 2. Minimum Amplitude to SYNC (at 12 Vin, 300-ns PW, and 200 kHz)

2.3 Minimum SYNC_IN Pulse Width

In Figure 3, an example of the minimum pulse width needed to synchronize is illustrated that holds true for 2.8-V amplitude input signal, from 200 V to 600 kHz, and from 8 Vin to 17 Vin. From this illustration it is seen that a minimum pulse width of 300 ns is required to properly synchronize a slave UCC28950. At pulse widths of less than 300 ns, the controller loses synchronization and it appears that whichever signals are not the trigger signal on the oscilloscope appear to run freely. A pulse width of 300 ns must be considered as an absolute minimum, and it is suggested that applications use a signal with a pulse width greater than this minimum for reliable operation across varying conditions.



Ch. 1: Input to SYNC pin of slave UCC28950 (originating from function generator)
Ch. 2: J8 connector on UCC28950 control board = OUTA signal of IC
Ch. 3: J9 connector on UCC28950 control board = OUTB signal of IC

Figure 3. Minimum Pulse Width to SYNC (at 12 Vin, 2.8 V, 200 kHz)

3 Example of a Four-Phase UCC28950 PSFB

Using two Tektronix AFG3102 function generators connected to trigger together, the following input signals seen in Figure 4 intended for our four UCC28950 control cards were generated. All four controllers were powered from the same 12-V source with all the connections of equivalent impedance.

With the input SYNC signal to the UCC28950 at 200 kHz, the outputs of the IC are 100 kHz each. For four phases in a multiphase buck application, a 90-degree phase shift is required between subsequent supplies which equates to a 2.5-μs delay between falling edges of subsequent SYNC signals.

However, for a phase-shifted, full-bridge controller, the frequency of the input current ripple is twice the frequency of a single output signal such as OUTA. Therefore, at 100-kHz output frequency, the input current has a frequency of 200 kHz with a 5-μs period, which, divided by the four phases for this application, yields a 1.25-μs desired delay between each subsequent SYNC signal's falling edge. This results in the desired 1.25-μs delay between the rising edges of each output signal OUTB1, OUTB2, OUTB3, OUTB4, OUTA1, OUTA2, OUTA3, and OUTA4 in that order and then this pattern repeats. This timing results in the optimum ripple cancellation to achieve the maximum benefits from synchronization. The timing flow for this specific application is demonstrated in Figure 4.

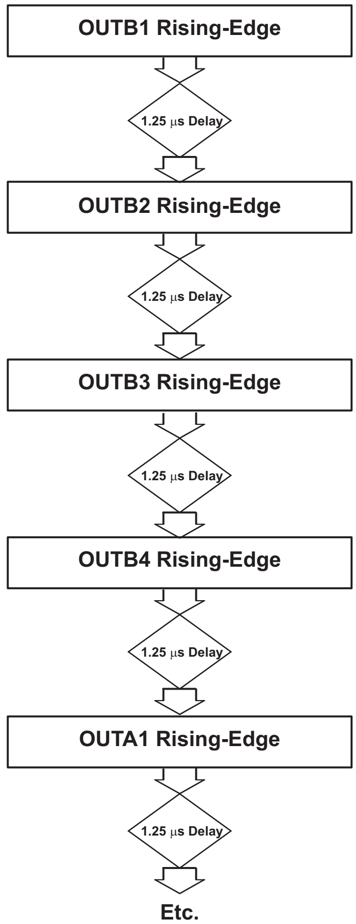
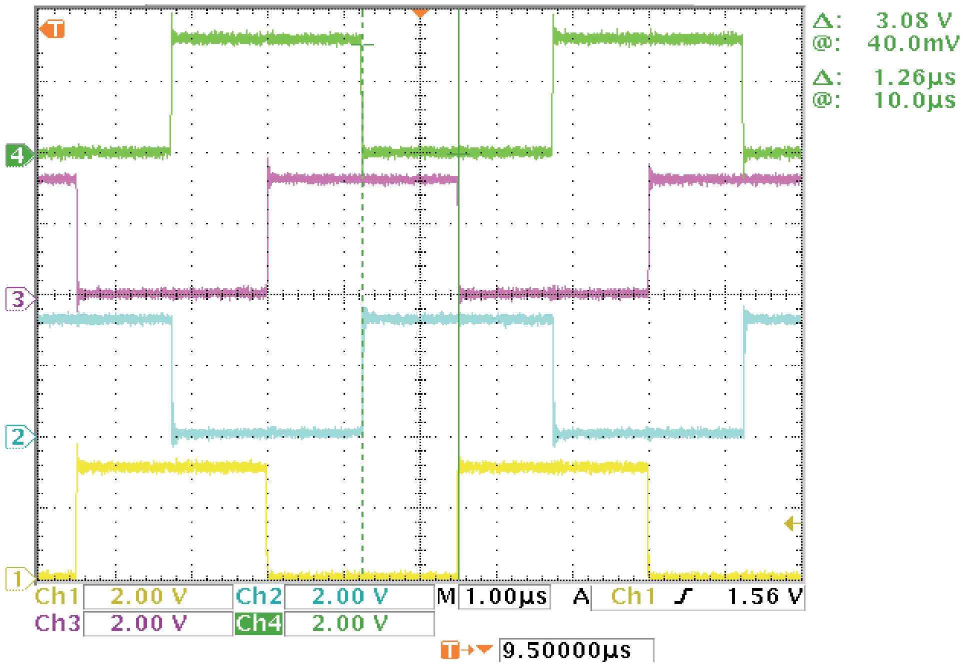


Figure 4. Output Signals Rising-Edge Timing Flow

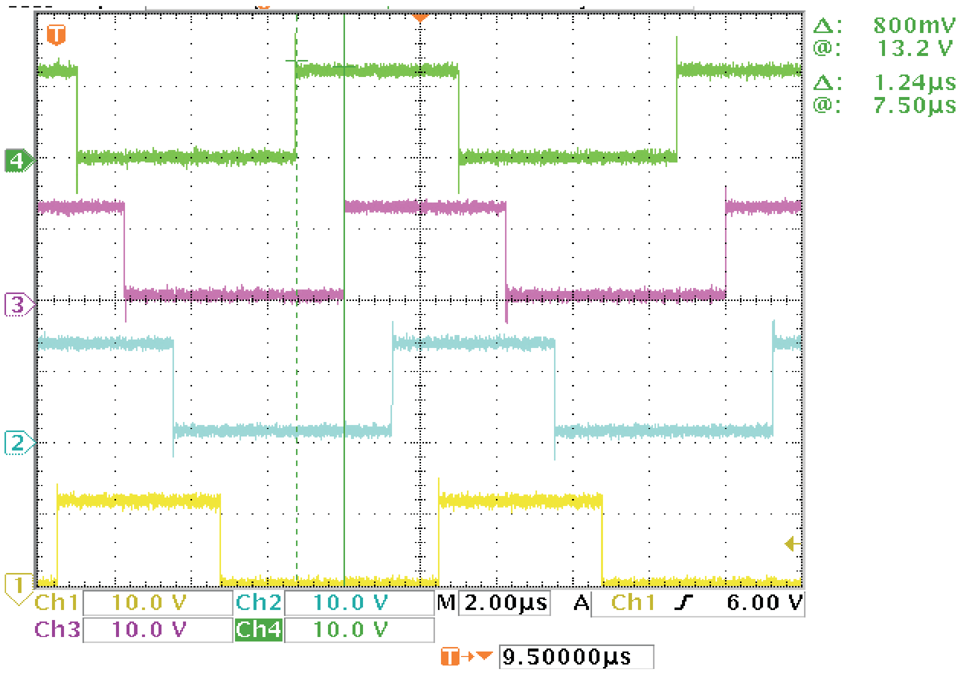
The desired SYNC input signals discussed previously can be seen in Figure 5, which displays the proper delay between the falling edges of Ch.4 and Ch.3.



Ch. 4: SYNC Input Signal Phase 1
Ch. 3: SYNC Input Signal Phase 2
Ch. 2: SYNC Input Signal Phase 3
Ch. 1: SYNC Input Signal Phase 4

Figure 5. Input Signals to SYNC Pins of Four-Phase UCC28950 PSFB Converter (50% D, 200 kHz)

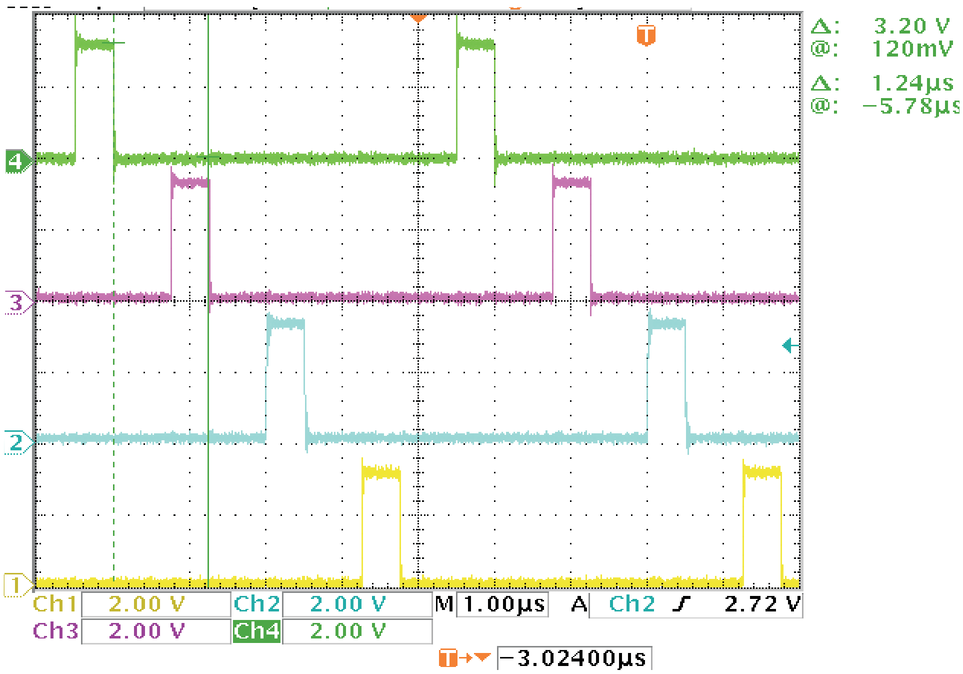
With the inputs of Figure 5, the four resulting output signals are seen in Figure 6. For a given channel in Figure 6, its corresponding input is the equivalent channel number in Figure 5. Recall that if an input pulse were compared to its corresponding output signal, a 90-degree phase shift occurs between them as specified in the data sheet. As this occurs with all four phases, no additional phase offset can be seen between the output signals other than that which was set specifically by the 1.25-µs shift of input signals.



Ch. 4: Output Signal Phase 1 (OUTA1)
Ch. 3: Output Signal Phase 2 (OUTA2)
Ch. 2: Output Signal Phase 3 (OUTA3)
Ch. 1: Output Signal Phase 4 (OUTA4)

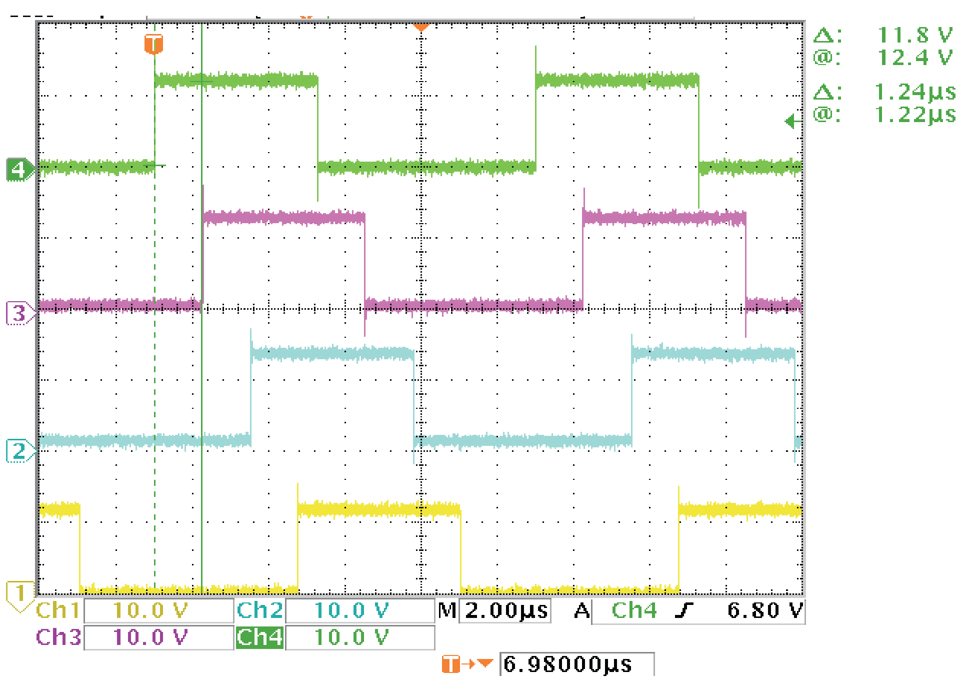
Figure 6. Output Signals From OUTA Pins of Each of the Four UCC28950 Controllers

If the input signals are smaller pulses, a 10% duty cycle for example, (which is a 500-ns on-time for 200 kHz) seen in Figure 7, the outputs of Figure 8 remain the same as seen before in Figure 6 as long as all SYNC input signals meet the minimum specifications set forth in the beginning of this document and their falling edges are aligned and offset by the same time of 1.25 µs.



Ch. 4: SYNC Input Signal Phase 1
Ch. 3: SYNC Input Signal Phase 2
Ch. 2: SYNC Input Signal Phase 3
Ch. 1: SYNC Input Signal Phase 4

Figure 7. Input Signals to SYNC Pins of Four-Phase UCC28950 PSFB Converter (10% D, 200 kHz)



Ch. 4: Output Signal Phase 1 (OUTA1)
Ch. 3: Output Signal Phase 2 (OUTA2)
Ch. 2: Output Signal Phase 3 (OUTA3)
Ch. 1: Output Signal Phase 4 (OUTA4)

Figure 8. Output Signals From OUTA Pins of Each of the Four UCC28950 Controllers

To generate the desired four SYNC input signals with the proper delay demonstrated in Figure 8, a clock signal input and the shift-register circuit seen in Figure 9 is all that is needed.

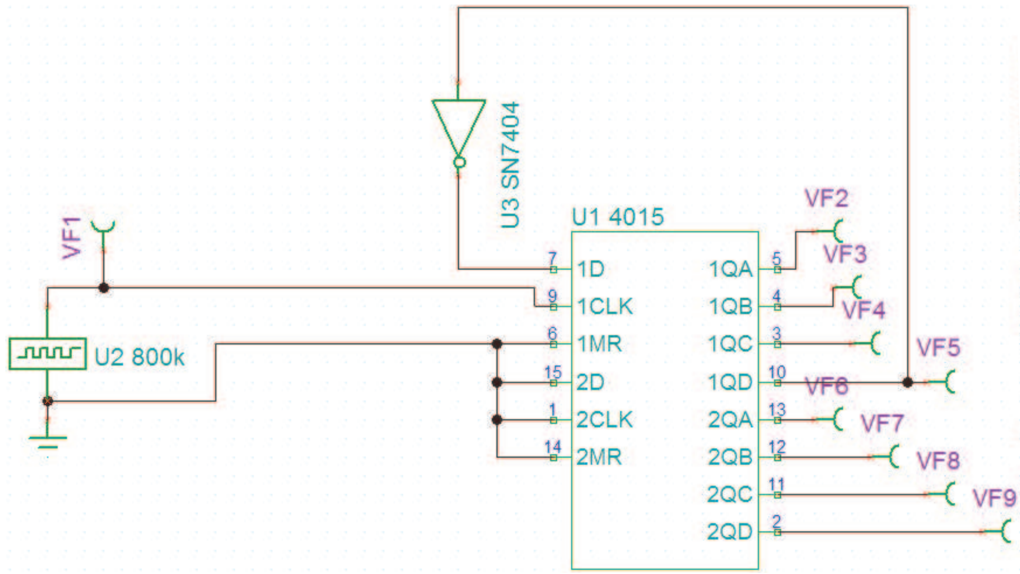


Figure 9. Four-Bit Shift-Register to Generate Four, Phase-shifted SYNC Signals From a Single Clock Source

Comparing the outputs VF2 through VF5 in Figure 10 to Channel 4 through Channel 1 of Figure 5, it can be seen that they are equivalent.

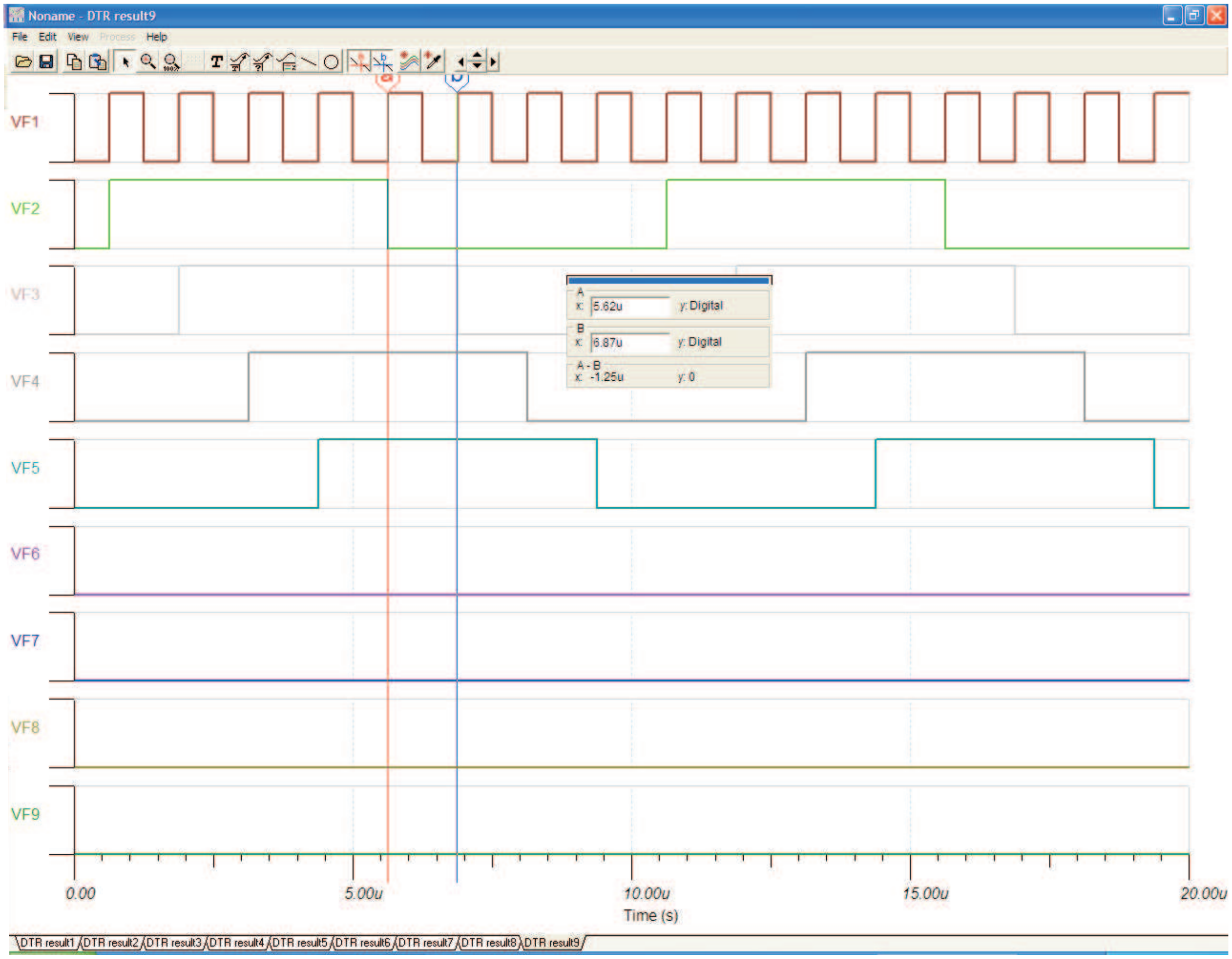
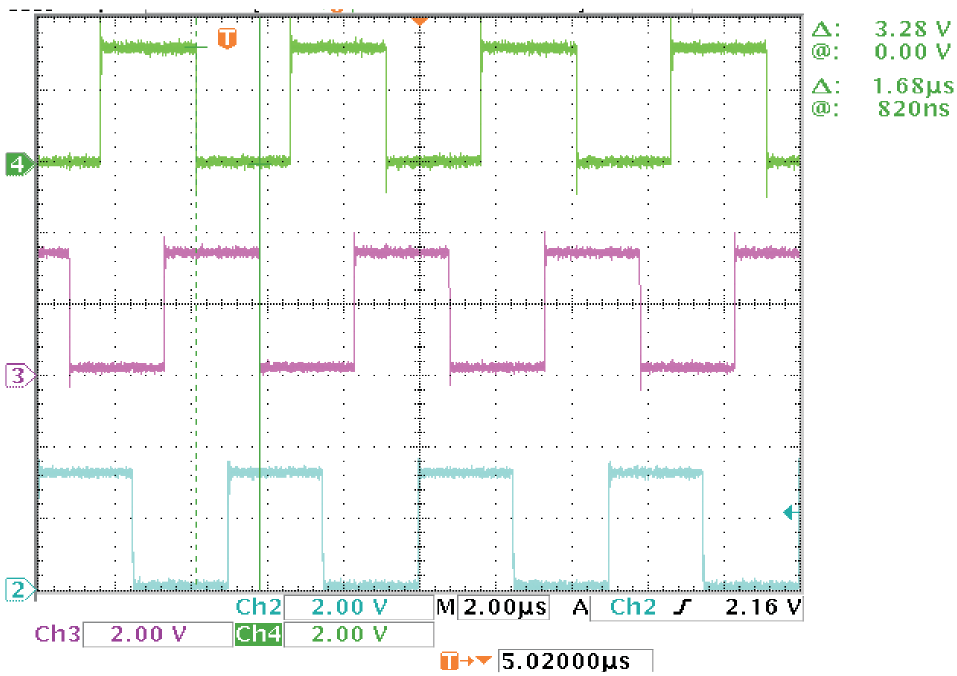


Figure 10. Waveforms of Dual, Four-Bit, Shift-Register Circuit

4 Example of a Three-Phase UCC28950 PSFB

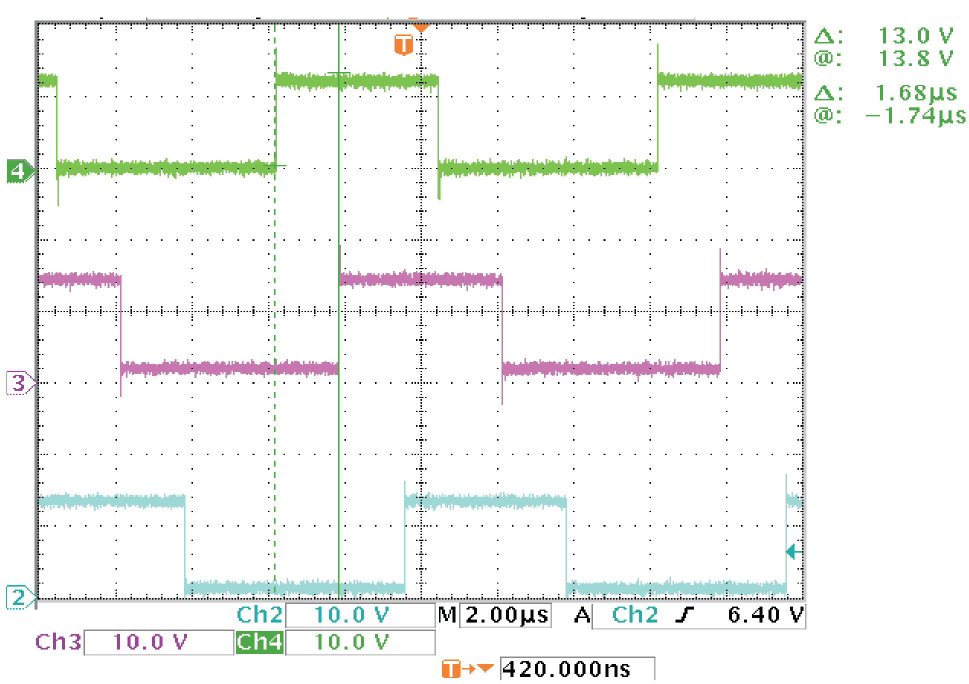
If instead of a four-phase UCC28950 supply, the application required only three-phases, the approach is very similar but the three SYNC input signals have a 1.67-μs falling edge delay for a 200-kHz SYNC frequency as seen in Figure 11.



Ch. 4: SYNC Input Signal Phase 1
Ch. 3: SYNC Input Signal Phase 2
Ch. 2: SYNC Input Signal Phase 3

Figure 11. Input Signals to SYNC Pins of Three-Phase UCC28950 PSFB Converter (50% D, 200 kHz)

With these input signals, the outputs of the respective UCC28950 controllers appear as seen in Figure 12.



Ch. 4: Output Signal Phase 1 (OUTA1)
Ch. 3: Output Signal Phase 2 (OUTA2)
Ch. 2: Output Signal Phase 3 (OUTA3)

Figure 12. Output Signals From OUTA Pins of Each of the Three UCC28950 Controllers

5 Conclusion

This application report explains and characterizes useful parameters when synchronizing three or more UCC28950 power supply controllers. The document also demonstrates two examples of multiphase circuits using four and three UCC28950s, respectively, and the corresponding input and output signaling. Finally, it shows that with a single clock and some simple, inexpensive circuits, these phase-adjusted SYNC signals can be generated to synchronize multiple power supplies.

Appendix A UCC28950 Control Card Schematic and Layout

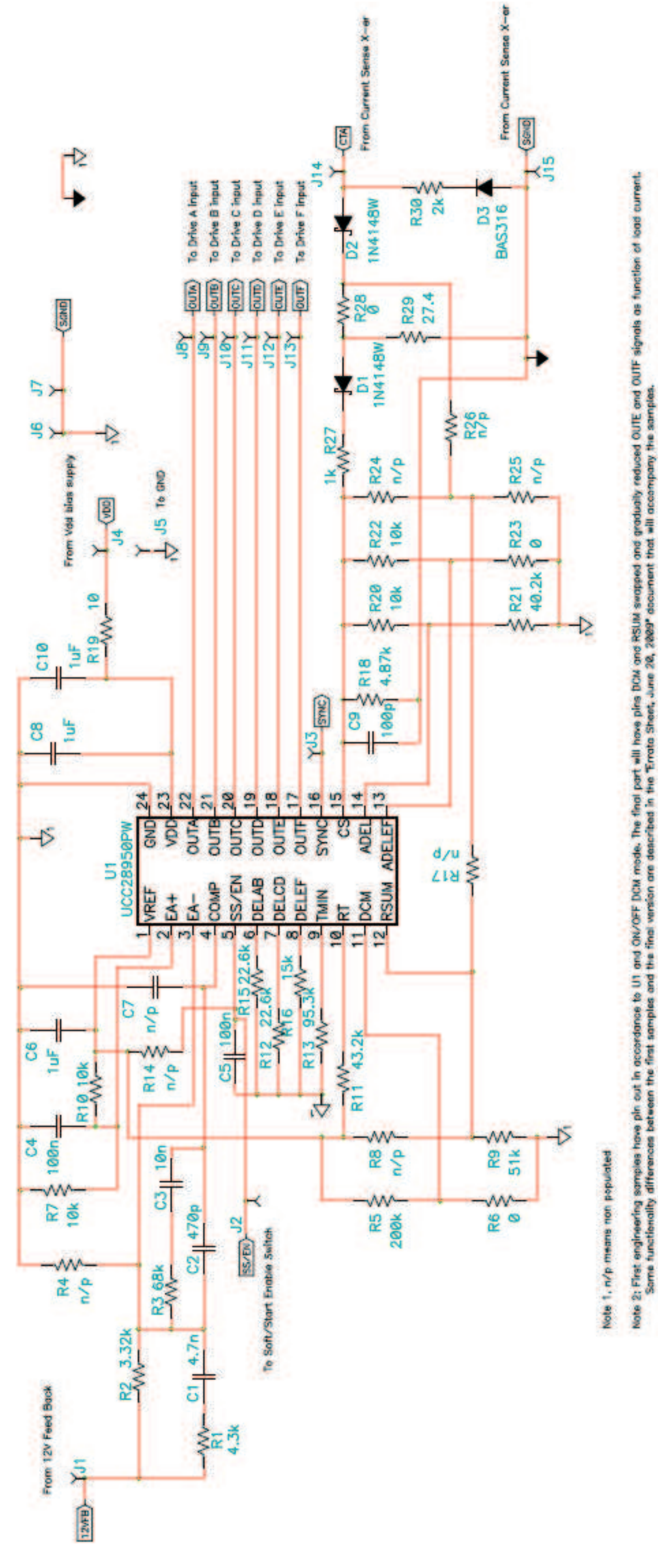


Figure 13. UCC28950 Small Control Card Schematic

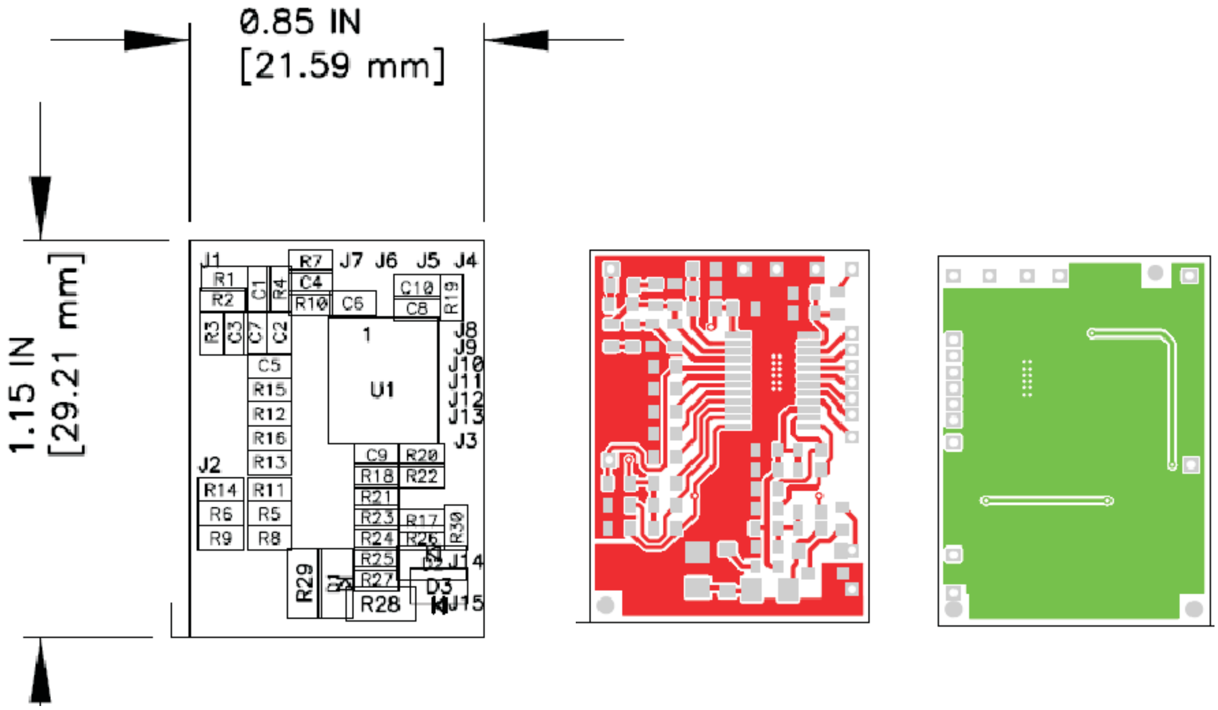


Figure 14. UCC28950 Small Control Card Layout and Assembly

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