Application Report
SLUA660A–November 2012–Revised September 2014

bq40z50 Advanced Gas Gauge Circuit Design

Battery Management Solutions

ABSTRACT

Components in the bq40z50 reference design are explained in this application report. Design analysis and suggested tradeoffs are provided, where appropriate.

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1 Introduction

The bq40z50 advanced gas gauge has approximately 61 components in the reference design for a four-thermistor, five-LED, four-cell application. The device is divided into the following classifications: High-Current Path, Gas Gauge Circuit, Secondary-Current Protection and Cell-Balancing Circuit, and Secondary-Voltage Protection.

This discussion is based on the four-cell reference design for the bq40z50 and bq294700 chipset. Figure 17 shows the bq40z50 reference design schematic.

2 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, and the sense resistor, and then returns to the PACK– terminal (see Section 6). In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

2.1 Protection FETs

The N-channel charge and discharge FETs must be selected for a given application. Most portable battery applications are a good match for the Si7114DN. The Vishay Si7114DN is an 18.3-A, 30-V device with Rds(on) of 7.5 mΩ when the gate drive voltage is 10 V.

If a precharge FET is used, R1 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to (Vcharger – Vbat) / R1 and maximum power dissipation is $(Vcharger – Vbat)^2/R1$.

The gates of all protection FETs are pulled to the source with a high-value resistor between the gate and source to ensure they are turned off if the gate drive is open.

Capacitors C1 and C2 help protect the FETs during an ESD event. The use of two devices ensures normal operation if one of them becomes shorted. In order to have good ESD protection, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both C1 and C2 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

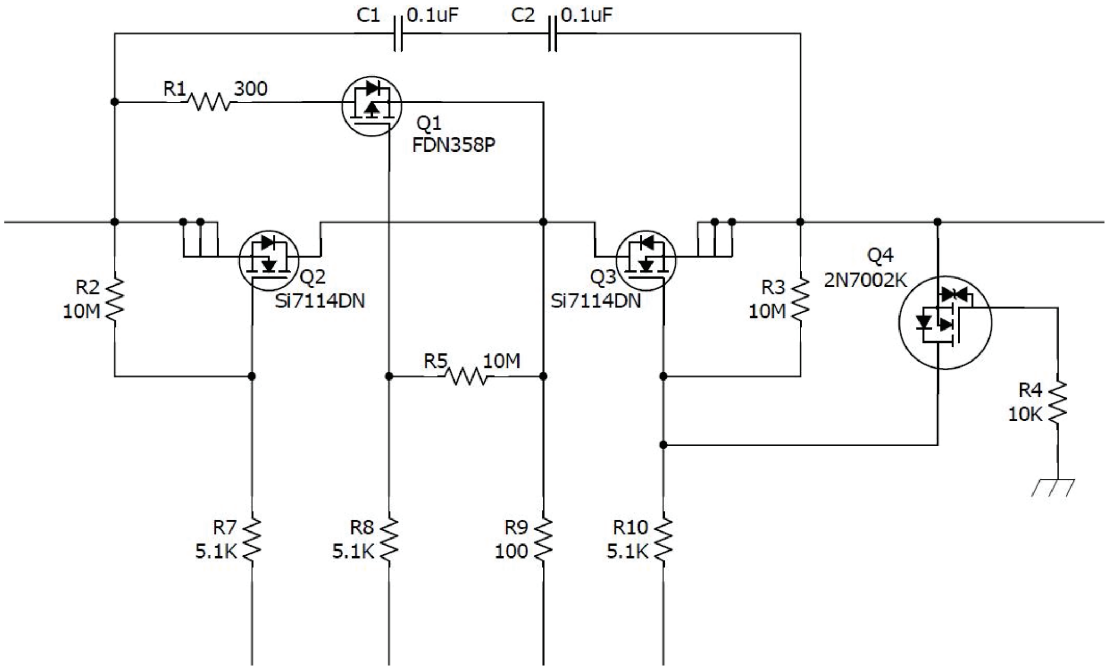

Figure 1. bq40z50 Protection FETs

2.2 Chemical Fuse

The chemical fuse (Dexerials, Uchihashi, and so forth) is ignited under command from either the bq294700 secondary voltage protection IC or from the FUSE pin of the gas gauge. Either of these events applies a positive voltage to the gate of Q5, shown in Figure 2, which then sinks current from the third terminal of the fuse, causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-channel FET. Ensure that the proper voltage, current, and Rds(on) ratings are used for this device. The fuse control circuit is discussed in detail in Section 3.5.

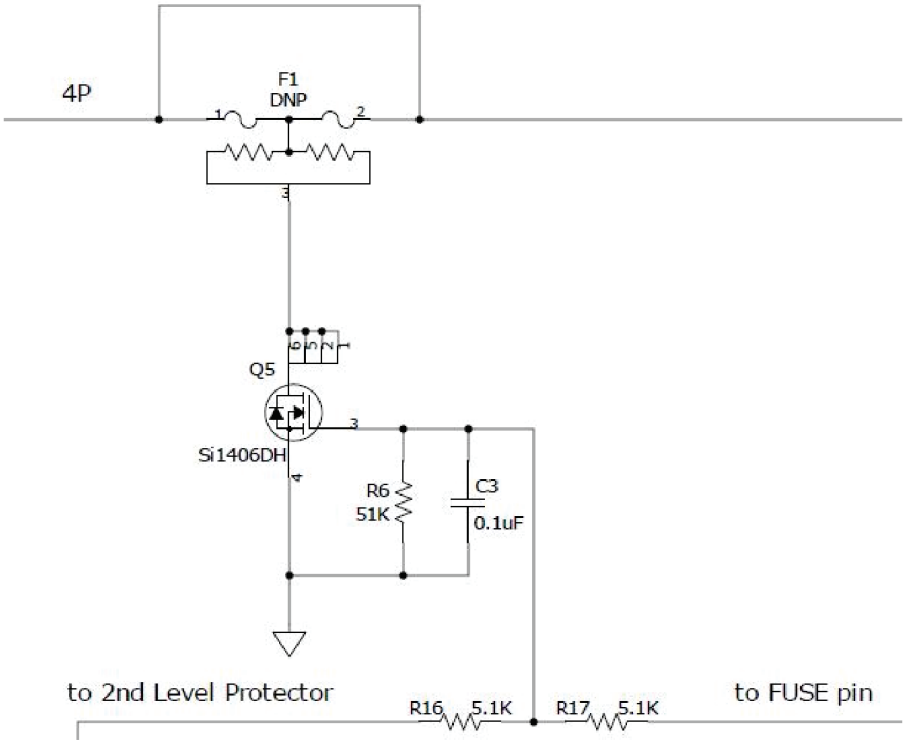

Figure 2. FUSE Circuit

2.3 Lithium-Ion Cell Connections

The important thing to remember about the cell connections is that high current flows through the top and bottom connections; therefore, the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. The location marked 4P in Figure 3 indicates the Kelvin connection of the most positive battery node. The connection marked 1N is equally important. The VC5 pin (a ground reference for cell voltage measurement), which is in the older generation devices, is not in the bq40z50 device. Hence, the single-point connection at 1N to the low-current ground is needed to avoid an undesired voltage drop through long traces while the gas gauge is measuring the bottom cell voltage.

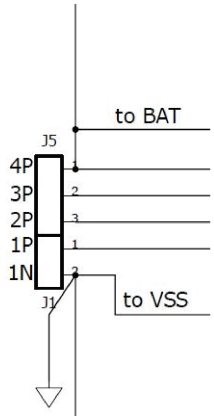

Figure 3. Lithium-Ion Cell Connections

2.4 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the bq40z50. Select the smallest value possible in order to minimize the negative voltage generated on the bq40z50 V_{SS} node(s) during a short circuit. This pin has an absolute minimum of –0.3 V. Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a 1-mΩ to 3-mΩ sense resistor.

The ground scheme of bq40z50 is different from the older generation devices. In previous devices, the device ground (or low current ground) is connected to the SRN side of the Rsense resistor pad. The bq40z50, however, connects the low-current ground on the SRP side of the Rsense resistor pad, close to the battery 1N terminal (see Section 2.3). This is because the bq40z50 has one less VC pin (a ground reference pin VC5) compared to the previous devices. The pin was removed and was internally combined to SRP.

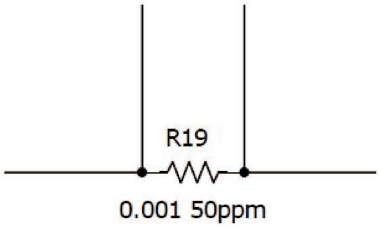

Figure 4. Sense Resistor

2.5 ESD Mitigation

A pair of series 0.1-µF ceramic capacitors is placed across the PACK+ and PACK– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors becomes shorted.

Optionally, a tranzorb such as the SMBJ2A can be placed across the terminals to further improve ESD immunity.

3 Gas Gauge Circuit

The Gas Gauge Circuit includes the bq40z50 and its peripheral components. These components are divided into the following groups: Differential Low-Pass Filter, PBI, System Present, SMBus Communication, FUSE circuit, and LED.

3.1 Coulomb-Counting Interface

The bq40z50 uses an integrating delta-sigma ADC for current measurements. Add a 100-Ω resistor from the sense resistor to the SRP and SRN inputs of the device. Place a 0.1-µF (C18) filter capacitor across the SRP and SRN inputs. Optional 0.1-µF filter capacitors (C19 and C20) can be added for additional noise filtering, if required for your circuit. Place all filter components as close as possible to the device. Route the traces from the sense resistor in parallel to the filter circuit. Adding a ground plane around the filter network can add additional noise immunity.

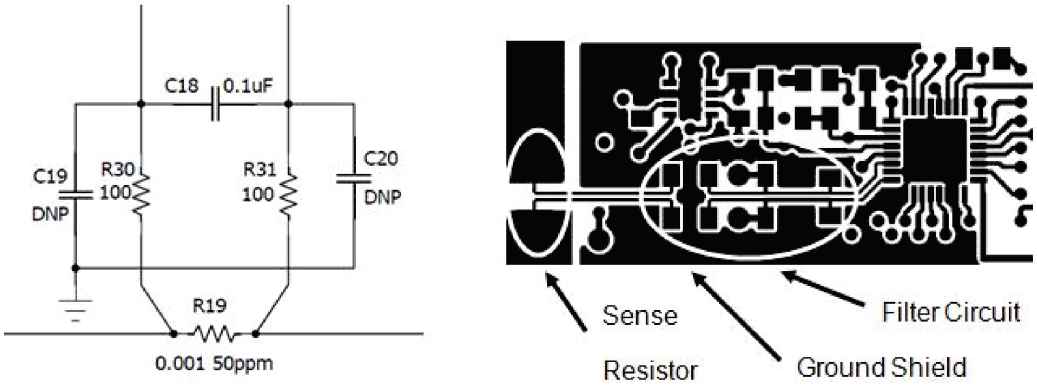

Figure 5. Differential Filter

3.2 Power Supply Decoupling and PBI

The bq40z50 has an internal LDO that is internally compensated and does not require an external decoupling capacitor.

The PBI pin is used as a power supply backup input pin providing power during brief transient power outages. A standard 2.2-µF ceramic capacitor is connected from the PBI pin to ground as shown in Figure 6.

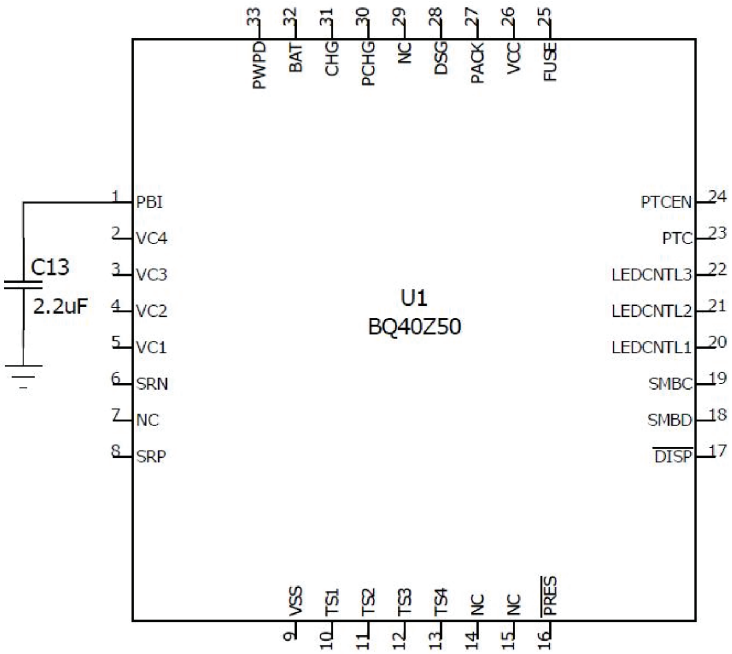

Figure 6. Power Supply Decoupling

3.3 System Present

The System Present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The $\overline{\text{PRES}}$ pin of the bq40z50 is occasionally sampled to test for system present. To save power, an internal pullup is provided by the gas gauge during a brief 4-µs sampling pulse once per second. A resistor can be used to pull the signal low and the resistance must be 20 kΩ or lower to insure that the test pulse is lower than the VIL limit. The pull-up current source is typically 10 µA to 20 µA.

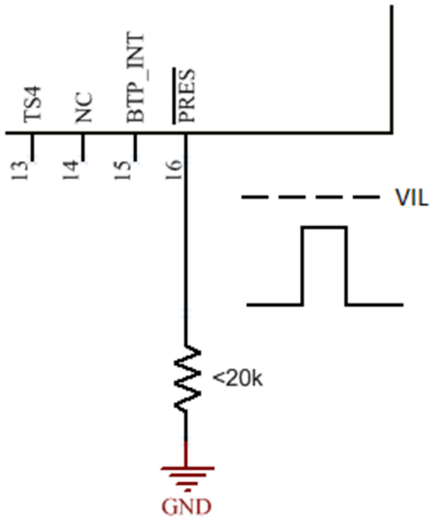

Figure 7. System Present Pull-Down Resistor

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. An integrated ESD protection on the $\overline{\text{PRES}}$ device pin reduces the external protection requirement to just R29 for an 8-kV ESD contact rating. However, if it is possible that the System Present signal may short to PACK+, then R28 and D4 must be included for high-voltage protection.

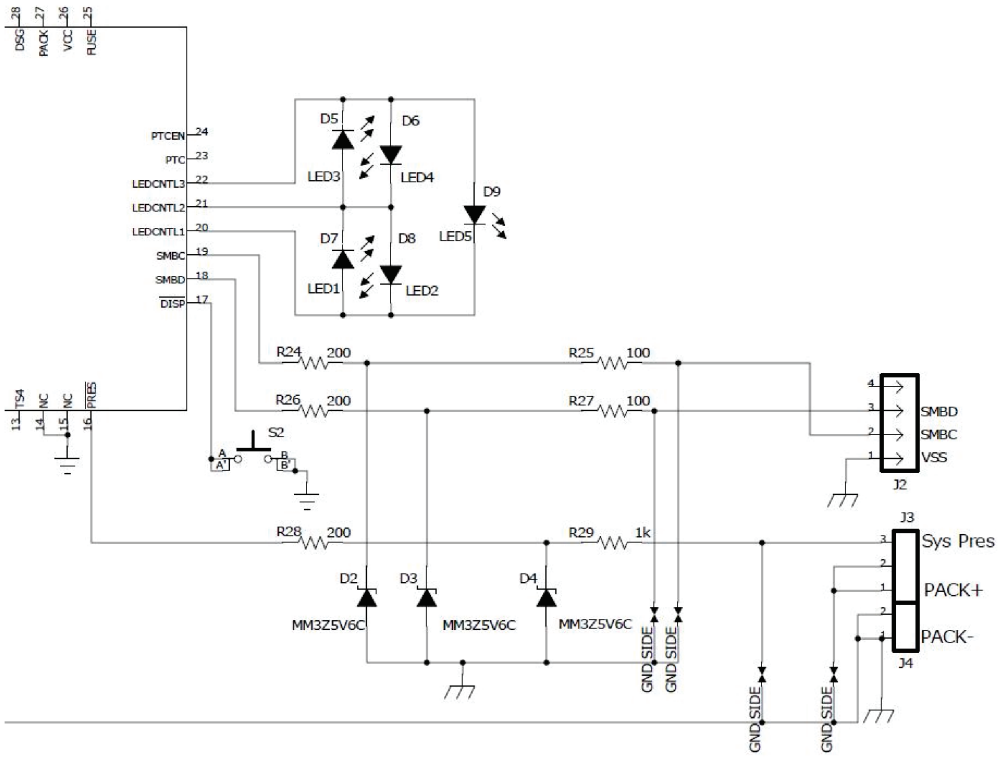

Figure 8. System Present ESD and Short Protection

3.4 SMBus Communication

The SMBus clock and data pins have integrated high-voltage ESD protection circuits, however, adding a Zener diode (D2 and D3) and series resistor (R24 and R26) provides more robust ESD performance.

The SMbus clock and data lines have internal pulldown. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into sleep mode to conserve power.

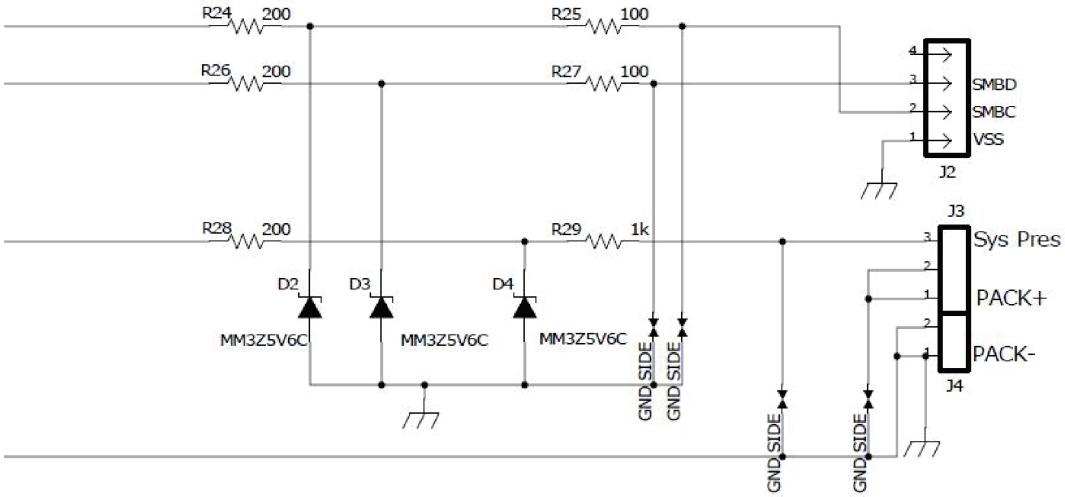

Figure 9. ESD Protection for SMB Communication

3.5 FUSE Circuitry

The FUSE pin of the bq40z50 is designed to ignite the chemical fuse if one of the various safety criteria is violated. The FUSE pin also monitors the state of the secondary-voltage protection IC. Q5 ignites the chemical fuse when its gate is high. The 7-V output of the bq294700 is divided by R16 and R6, which provides adequate gate drive for Q5 while guarding against excessive back current into the bq294700 if the FUSE signal is high.

Using C3 is generally a good practice, especially for RFI immunity. C3 may be removed, if desired, because the chemical fuse is a comparatively slow device and is not affected by any sub-microsecond glitches that come from the FUSE output during the cell connection process.

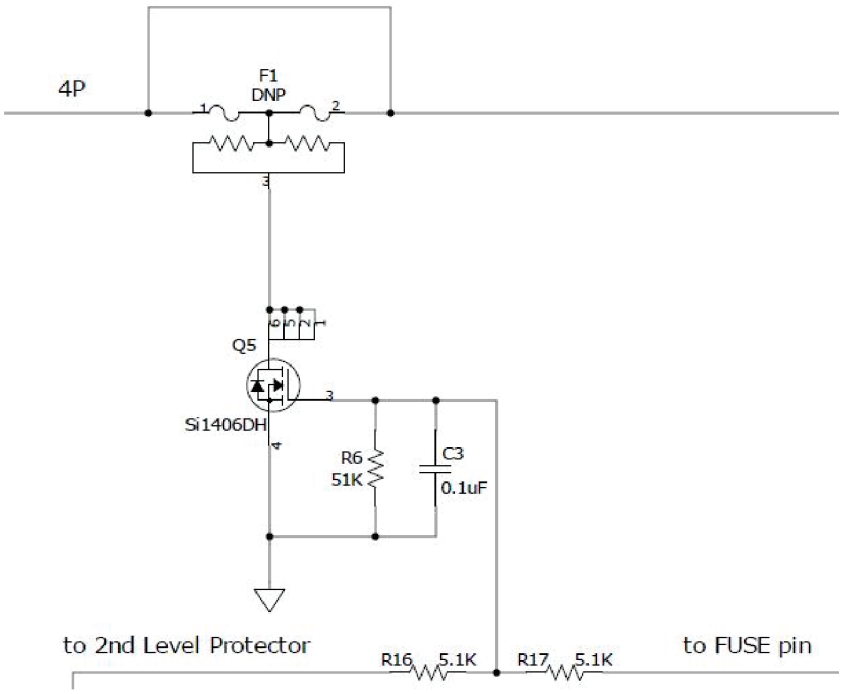

Figure 10. FUSE Circuit

When the bq40z50 is commanded to ignite the chemical fuse, the FUSE pin activates to give a typical 8-V output. The new design makes it possible to use a higher Vgs FET for Q5. This improves the robustness of the system, as well as widens the choices for Q5.

4 Secondary-Current Protection

The bq40z50 provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, and voltage translation. The following discussion examines Cell and Battery Inputs, Pack and FET Control, Temperature Output, and Cell Balancing.

4.1 Cell and Battery Inputs

Each cell input is conditioned with a simple RC filter, which provides ESD protection during cell connect and acts to filter unwanted voltage transients. The resistor value allows some trade-off for cell balancing versus safety protection.

The integrated cell balancing FETs allow the AFE to bypass cell current around a given cell or numerous cells, effectively balancing the entire battery stack. External series resistors placed between the cell connections and the VCx I/O pins set the balancing current magnitude. The intern FETs provide a 200-Ω resistance (2 V < VDS < 4 V). Series input resistors between 100 Ω and 1 kΩ are recommended for effective cell balancing.

The BAT input uses a diode (D1) to isolate and decouple it from the cells in the event of a transient dip in voltage caused by a short-circuit event.

Also, as described previously in Section 2, the top and bottom nodes of the cells must be sensed at the battery connections with a Kelvin connection to prevent voltage sensing errors caused by a drop in the high-current PCB copper.

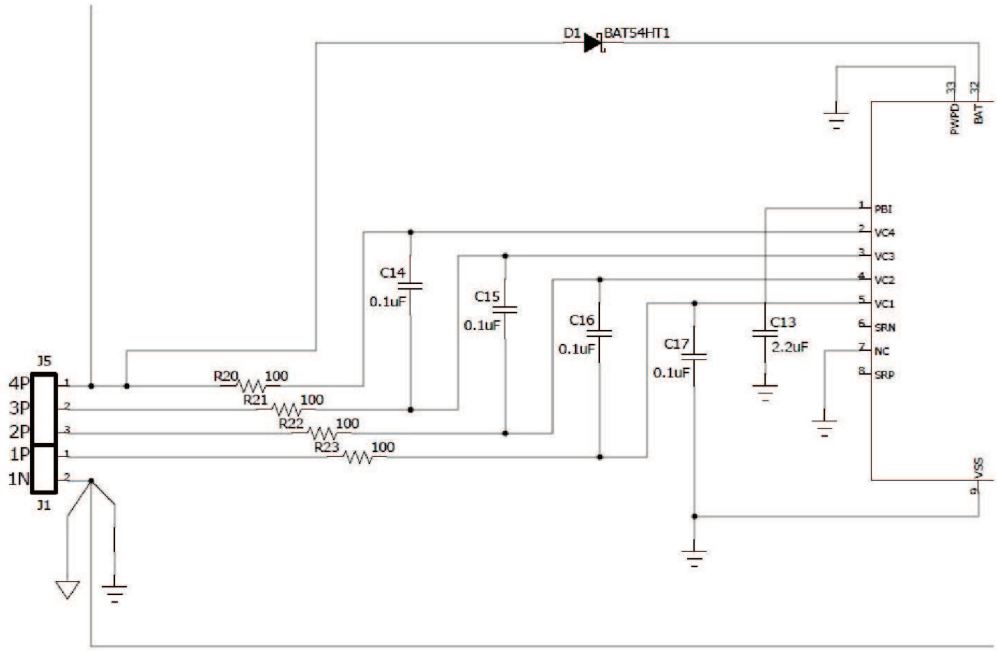

Figure 11. Cell and BAT Inputs

4.2 External Cell Balancing

Internal cell balancing can only support up to 10 mA. External cell balancing provide as another option for faster cell balancing. For details, refer to the application note, *Fast Cell Balancing Using External MOSFET* (SLUA420).

4.3 PACK and FET Control

The PACK and V_{CC} inputs provide power to the bq40z50 from the charger. The PACK input also provides a method to measure and detect the presence of a charger. The PACK input uses a 100-Ω resistor, whereas the V_{CC} input uses a diode to guard against input transients and prevents misoperation of the date driver during short-circuit events.

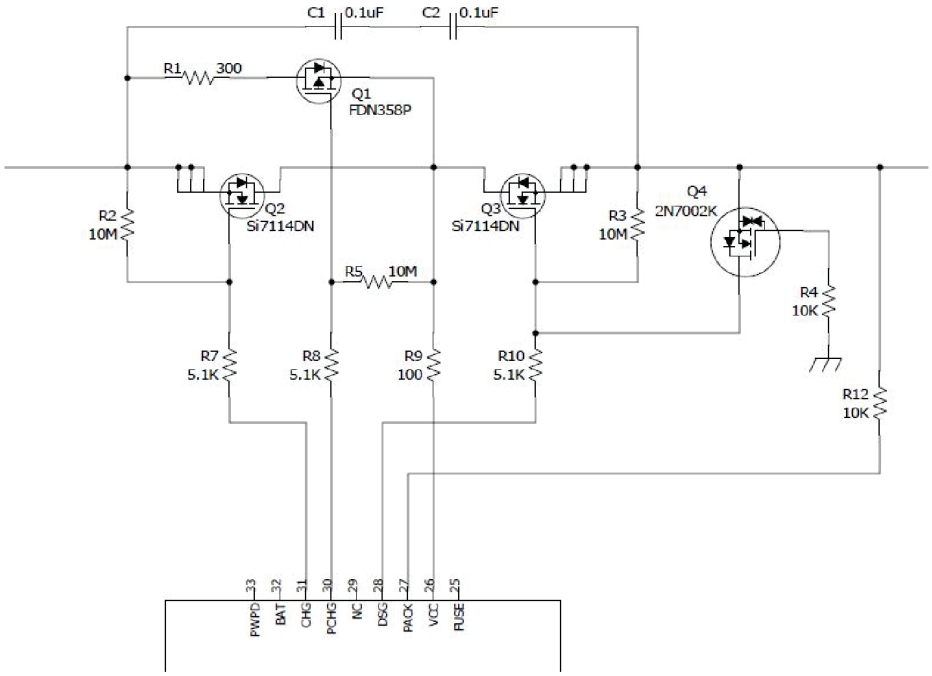

Figure 12. bq40z50 PACK and FET Control

The N-channel charge and discharge FETs are controlled with 5.1-kΩ series gate resistors, which provide a switching time constant of a few microseconds. The 10-MΩ resistors ensure that the FETs are off in the event of an open connection to the FET drivers. Q4 is provided to protect the discharge FET (Q3) in the event of a reverse-connected charger. Without Q4, Q3 can be driven into its linear region and suffer severe damage if the PACK+ input becomes slightly negative.

Q4 turns on in that case to protect Q3 by shorting its gate to source. To use the simple ground gate circuit, the FET must have a low gate turn-on threshold. If it is desired to use a more standard device, such as the 2N7002 as the reference schematic, the gate should be biased up to 3.3 V with a high-value resistor. The bq40z50 device has the capability to provide a current-limited charging path typically used for low battery voltage or low temperature charging. The bq40z50 device uses an external P-channel, pre-charge FET controlled by PCHG.

4.4 Temperature Output

For the bq40z50 device, TS1, TS2, TS3, and TS4 provide thermistor drive-under program control. Each pin can be enabled with an integrated 18-kΩ (typical) linearization pullup resistor to support the use of a 10-kΩ at 25°C (103) NTC external thermistor such as a Mitsubishi BN35-3H103. The reference design includes four 10-kΩ thermistors: RT1, RT2, RT3, and RT4. The bq40z50 device supports up to four external thermistors. Connect unused thermistor pins to V_{SS}.

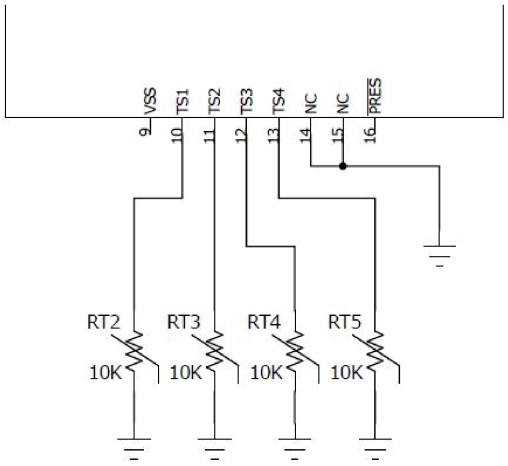

Figure 13. Thermistor Drive

4.5 LEDs

Three LED control outputs provide constant current sinks for the driving external LEDs. These outputs are configured to provide voltage and control for up to 5 LEDs. No external bias voltage is required. Unused LEDCNTL pins can remain open or they can be connected to V_{SS}. The DISP pin should be connected to V_{SS}, if the LED feature is not used.

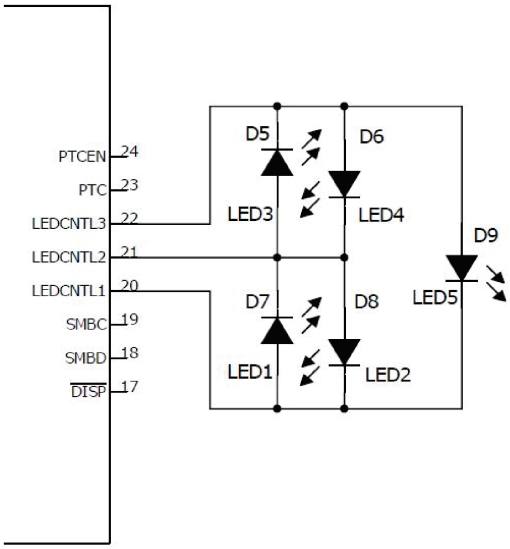

Figure 14. LEDs

4.6 Safety PTC Thermistor

The bq40z50 device provides support for a safety PTC thermistor. The PTC thermistor is connected between the PTC pin and V_{SS}. It can be placed close to the CHG/DSG FETs to monitor the temperature. The PTC pin outputs a very small current, typical ~370 nA , and the PTC fault will be triggered at ~0.7 V typical. A PTC fault is one of the permanent failure modes. It can only be cleared by a POR.

To disable this feature, connect a 10-kΩ resistor between PTC and V_{SS}.

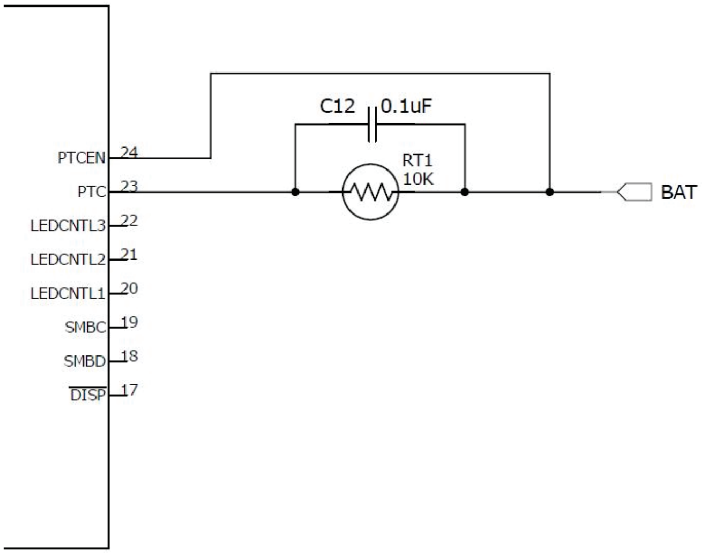

Figure 15. PTC Thermistor

5 Secondary-Overvoltage Protection

The bq294700 provides secondary-overvoltage protection and commands the chemical fuse to ignite if any cell exceeds the internally referenced threshold. The peripheral components are Cell Inputs and Time Delay Capacitor.

5.1 Cell Inputs

An input filter is provided for each cell input. This comprises the resistors R13, R14, R15, and R18 along with capacitors C4, C5, C9, and C11. This input network is completely independent of the filter network used as input to the bq40z50. To ensure independent safety functionality, the two devices must have separate input filters.

Because the filter capacitors are implemented differentially, a low-voltage device can be used in each case.

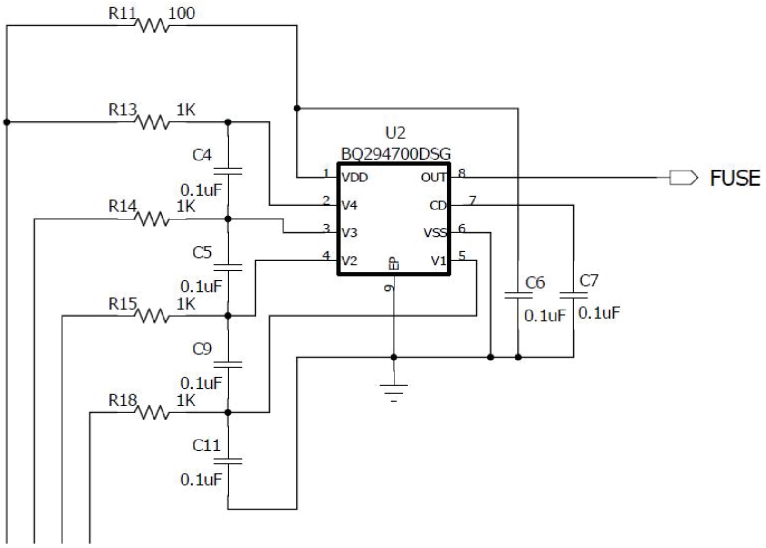

Figure 16. bq294700 Cell Inputs and Time-Delay Capacitor

5.2 Time-Delay Capacitor

C7 sets the time delay for activation of the output after any cell exceeds the threshold voltage. The time delay is calculated as td = 1.2 V × DelayCap (µF)/0.18 µA.

6 Reference Design Schematic

Figure 17 shows the bq40z50 reference design schematic.

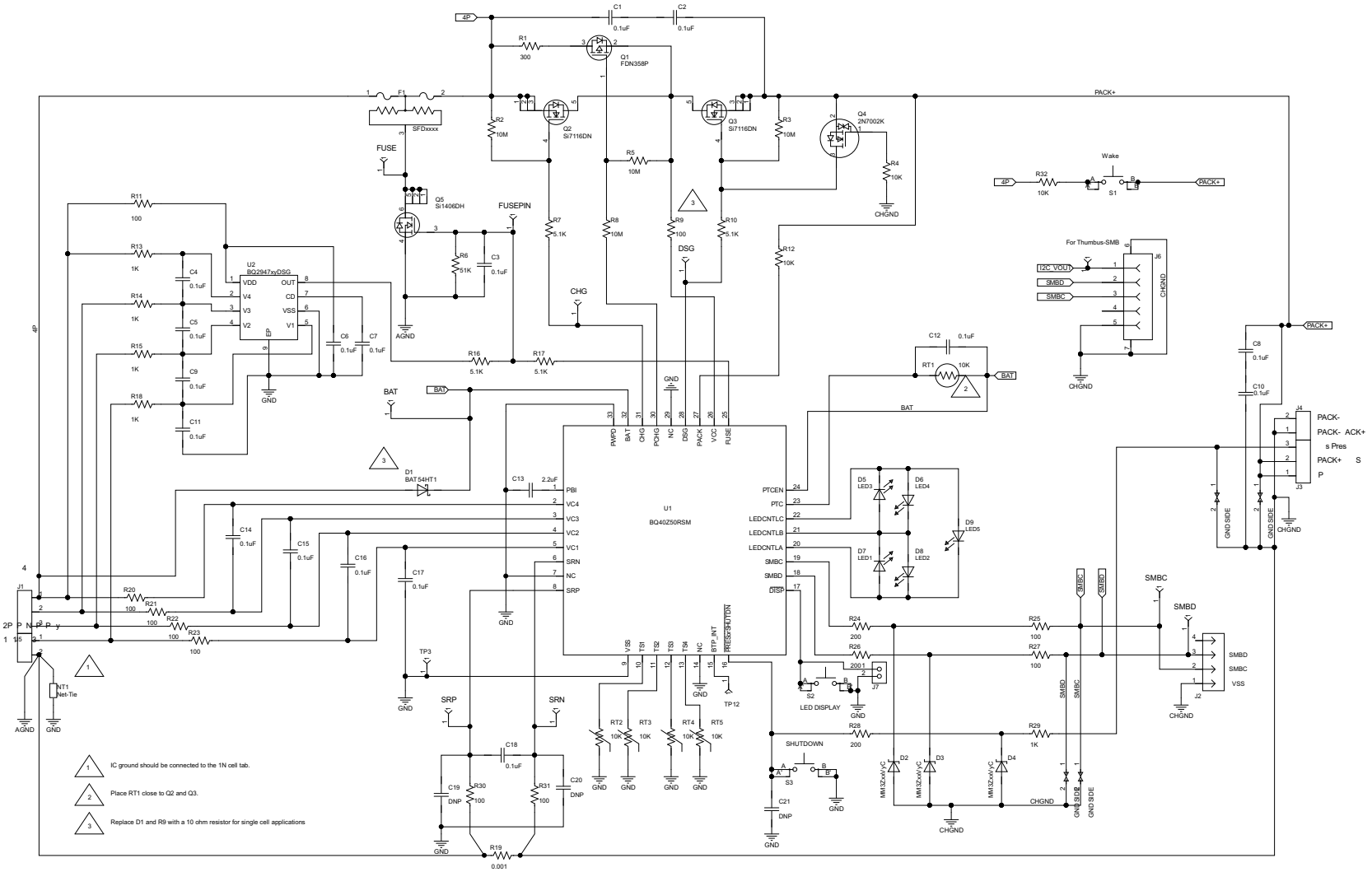

Figure 17. bq40z50 Schematic

Revision History

Changes from Original (November 2012) to A Revision **Page**

- Changed *Sony Chemical* to *Dexerials* in the *Chemical Fuse* section. 3
- Added paragraph and *System Present Pull-Down Resistor* image to the end of the first paragraph in the *System Present* section. 7
- Changed *two thermistors* to *four external thermistors* in the first paragraph of the *Temperature Ouput* section. 12
- Added sentence to the end of the first paragraph in the *Temperature Ouput* section. 12
- Added two sentences to the first paragraph in the *LEDs* section. 12
- Changed bq40z50 schematic. 15

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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