Application Report
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Addressing the Need for the Next-Generation Interleaved Transition Mode PFC

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ABSTRACT

The new changes in standards governing efficiency and losses in a power supply of all major high-volume end equipment including personal electronics have driven up the complexity of power supplies along with need for costly external components. These components include an auxiliary flyback converter, PFC disable circuits, and so forth. The UCC28064A device is introduced as the next-generation interleaved transition PFC controller in this document. When operated with the UCC25630x LLC controller, the total solution meets all the modern standby standards without needing any addition additional external circuits. The rest of document discusses some of the motivation and lists the changes between the UCC28063 and the UCC28064A devices.

For more information, see *Power Factor Correction* at *www.ti.com*.

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Trademarks

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1 Introduction

The two-phase interleaved critical condition mode (CRM) Boost PFC is used widely for medium to high-power systems AC/DC power supplies (300 W to 700 W) that need to be compliant with harmonic standards such as IEC61000-3-2. Figure 1 shows there has been a significant trend in the reduction in the thickness of DTV and All-In-One (AIO) PC. Currently, in a typical 52 in DTV, the maximum height of any electronic component cannot be more than 15 mm.

Figure 1. Progression of DTV Thickness Over the Years and With Various Technologies

These unique geometric constraints at these power levels make a single-phase CRM PFC unviable. This is due to large peak currents that increase conduction losses as well as the large size of these single inductors which become difficult to comply with the dimensional constraints. Continuous Conduction Mode (CCM) PFCs are also a good fit for this power level. The CCM PFC inductor is bigger than both an equivalent single-phase CRM PFC inductor and most certainly the two-phase CRM PFC inductors. Also, in a CCM PFC, the boost diodes suffer from reverse recovery losses that increase common mode emissions. Common mode filters are generally bulky and drive additional system costs of the power PFC, especially considering the tight height restrictions that may be imposed in these end equipment.

The UCC28063 device enables a cost-effective solution with a particular focus on ruggedness, fault management, fault recovery, efficiency, and higher end performance in areas such as acoustic management and fast transient response. The *Natural Interleaving*™ PFC controller in the UCC28063 device allows CRM operation and yet maintains the 1800 difference between the phases by adjusting the ON-time every switching cycle. This innovative approach reduces the input current ripple significantly; helps achieve good efficiency and EMI across the entire range of line and load voltage. The *Natural Interleaving* method also allows for operating with reduced audible noise and EMI which are two key challenges that must be solved in consumer electronics applications.

2 Motivation for the UCC28064A

In recent years there has been industry-wide adoption of standards designed to combat global warming. Recent examples include EU COC EPS Version 5 Tier 2 (5), DOE Level IV, and Energy Star 5.0 (star). These standards set minimum efficiency targets and limit the power that products can draw when in standby mode. Traditional CRM control schemes, such as frequency clamped constant ON-time PFC, do not provide adequate efficiency at light loads to meet these standards. Table 1 shows some of the key efficiency specifications that are increasingly being adopted industry wide.

Table 1. No-Load Power Consumption

RATED OUTPUT POWER	NO-LOAD POWER CONSUMPTION	
	TIER 1	TIER 2
≥ 0.3 W and < 49 W	0.15 W	0.075 W
> 49 W and < 250 W	0.25 W	0.15 W
Mobile handheld battery driven and < 8 W	0.075 W	0.075 W

Table 2. Energy-Efficiency Criteria for Active Mode

RATED OUTPUT POWER P_{NO}	MINIMUM 4 POINT AVERAGE EFFICIENCY IN ACTIVE MODE		MINIMUM EFFICIENCY IN ACTIVE MODE @ 10% OF FULL LOAD OF RATED OUTPUT CURRENT	
	TIER 1	TIER 2	TIER 1	TIER 2
0.3 W ≤ P_{NO} < 1	≥ 0.5 × P_{NO} + 0.146	≥ 0.5 × P_{NO} + 0.146	≥ 0.5 × P_{NO} + 0.46	≥ 0.5 × P_{NO} + 0.06
1 W ≤ P_{NO} < 49	≥ 0.0626 × lnM (P_{NO}) + 0.146	≥ 0.071 × lnM (P_{NO}) – 0.00115 × P_{NO} + 0.67	≥ 0.0626 × lnM (P_{NO}) + 0.546	≥ 0.071 × lnM (P_{NO}) – 0.00115 × P_{NO} + 0.67
49 W ≤ P_{NO} < 250	≥ 0.89 W	≥ 0.89 W	≥ 0.79 W	≥ 0.79 W

Table 3. Energy-Efficiency Criteria for Active Mode for Low-Voltage External Power Supplies

RATED OUTPUT POWER P_{NO}	MINIMUM 4 POINT AVERAGE EFFICIENCY IN ACTIVE MODE		MINIMUM EFFICIENCY IN ACTIVE MODE @ 10% OF FULL LOAD OF RATED OUTPUT CURRENT	
	TIER 1	TIER 2	TIER 1	TIER 2
0.3 W ≤ P_{NO} < 1	≥ 0.5 × P_{NO} + 0.086	≥ 0.5 × P_{NO} + 0.091	≥ 0.5 × P_{NO}	≥ 0.517 × P_{NO}
1 W ≤ P_{NO} < 49	≥ 0.0755 × lnM (P_{NO}) + 0.586	≥ 0.0834 × lnM (P_{NO}) – 0.0011 × P_{NO} + 0.69	≥ 0.072 × lnM (P_{NO}) + 0.500	≥ 0.0835 × lnM (P_{NO}) – 0.00127 × P_{NO} + 0.518
49 W ≤ P_{NO} < 250	≥ 0.88 W	≥ 0.88 W	≥ 0.78 W	≥ 0.78 W

These standby power requirements have created interesting challenges for the power-supply architecture. There are some practical ways of using older generations of PFCs such as the UCC28063 device to attain the previously mentioned performance targets, many of them have been successfully implemented in high-volume production.

Figure 2 shows a simplified block diagram of one such architecture.

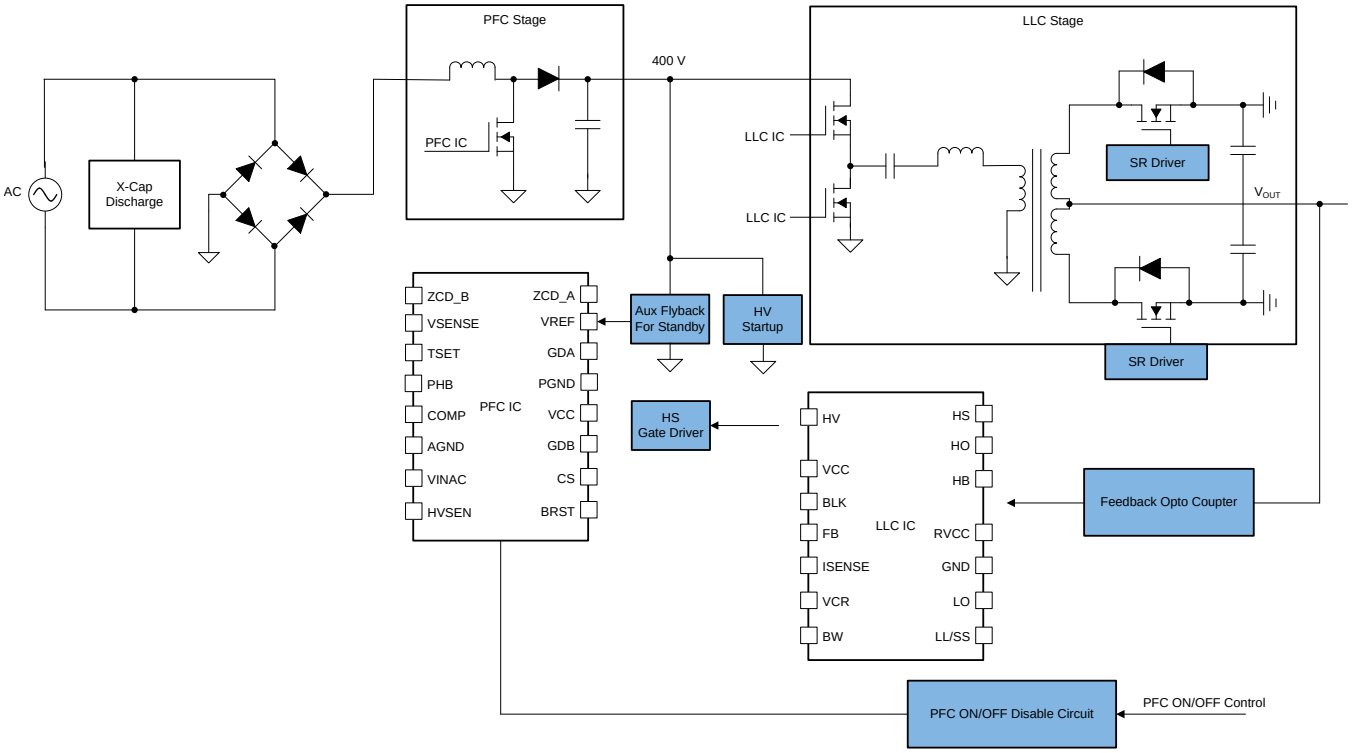

Figure 2. Block Diagram Representation of AC/DC Power Supply for Low Standby Power Applications

From the diagram it is clear that previous generations of DTV achieve low standby power by taking advantage of the following aspects of the system:

1. Turning off the PFC when the converter goes into standby mode.
2. Using an additional low-standby flyback converter to provide regulation to the house-keeping circuits and all the circuits that need to be ON during standby – this can enable the system to completely shut down the main power train of the system. This is also very common in applications such as higher power gaming adapters, power tool chargers, and LED lighting.

One of the key attractions of the UCC28064A device, when combined with the UCC25430x LLC controller is meeting these challenging requirements by providing significant cost savings to the overall system such as completely removing the auxiliary flyback power supply and the PFC disable circuitry.

3 Implications of Standards on PFC Design

It is clear from the previous two methods that reducing standby power has implications for both system cost as well as performance.

3.1 System Cost

One of the key tradeoffs of turning off a PFC is cost. At the very least, there must be hardware circuits to do the following functions:

- Detect the standby mode – this is usually done by hardware close to the load in the secondary
- Isolated disable signal
- Analog interface in the primary to turn OFF the PFC

These circuits add cost to the system. An optocoupler is the most commonly used component for creating an isolated disable signal. The optocoupler is expensive and is not known for reliability across its lifetime, especially in markets such as automotive and industrial. As the consumer electronics markets expand into emerging economies such as India, Africa, and so forth, where the residential AC line voltages are susceptible to frequency surges, dips, and interruptions. Modern power supply manufacturers are considering performing surge testing at elevated test voltage levels (> 6-kV common mode and differential mode) to ensure reliable operation in these places. This further drives up the cost of the optocoupler needed for the application. Figure 3 shows one implementation example:

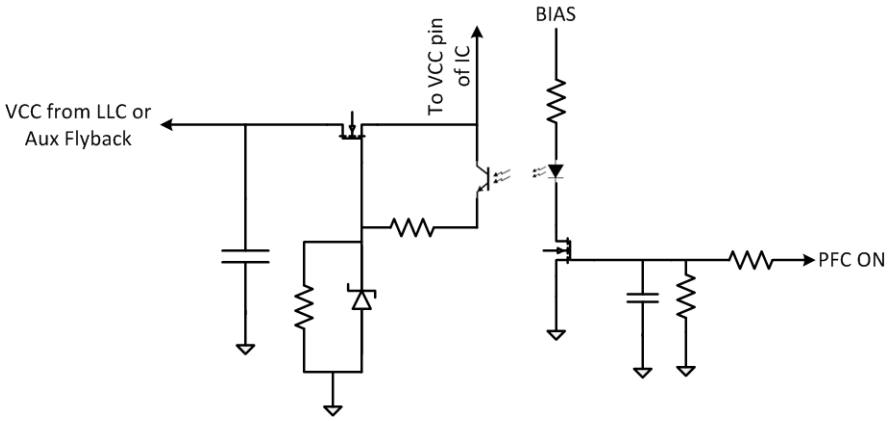

Figure 3. Example Implementation of a PFC Disable Circuit

The MOSFET on the primary is in series between the primary side VCC and the VCC pins of the control IC, thereby disabling the system when the PFC ON signal goes high.

3.2 Transient Response Out of Standby

Figure 4 shows a typical PFC startup at 85 Vac into a full load. What is clear is that the converter takes several line cycles before the PFC output is regulated to its final value. If there is an NTC to prevent inrush current in the circuit (as is usually the case), then startup in cold temperature can potentially take several 100 ms before the PFC output voltage goes to within 15% of its nominal value.

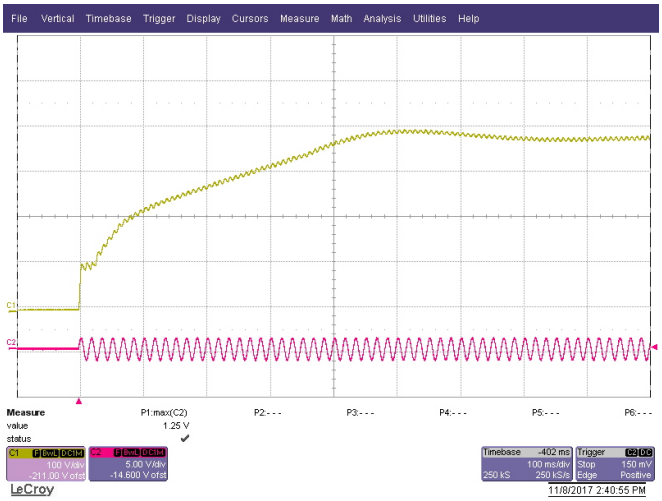

Figure 4. PFC Startup at Low Line (85 Vac)

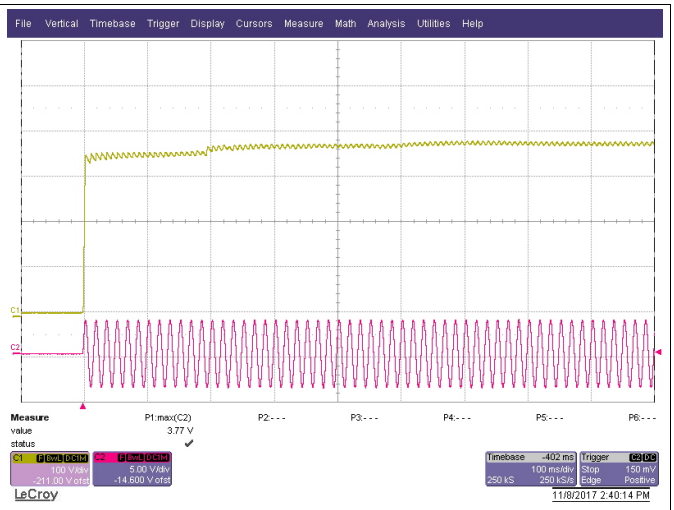

Figure 5. PFC Startup at High Line (265 Vac)

Hence every time the system comes out of standby, for example in a sudden load change from the standby condition, the PFC needs to start. The power-supply designer must make a tough tradeoff – wait for several hundred milliseconds before responding to the load step and risk degraded user experience, or overdesign the 2nd stage DC/DC converter such that it can temporarily provide the peak power necessary until the PFC completes its startup.

In applications such as LED lighting, there are tough standards such as CA-Title 22 which stipulate that the maximum startup time under all conditions has to be < 0.5 s. In other applications such as DTV or *All in One PC* (AIO), waiting several hundred ms for the PFC to turn ON means that there is a noticeable delay between the time the DTV is powered ON to the time when the content is actually visible to the viewer. This can further decrease the user experience. Hence, the ability to have an instant-ON feature or even a robust response out of a standby condition is highly desired. In some sophisticated applications, there are supervisory controllers which also run some firmware code to predict load changes coming out standby and feed the information up-stream to the AC/DC converter for better transient response. Power-supply designers may alternately increase the output capacitance of the AC/DC power supply a little to help reduce the voltage sag that may arise during this condition.

Another way to deal with this problem is to overdesign the 2nd stage DC/DC converter. Theoretically, if the 2nd stage converter were to be able to deliver full power from the peak of minimum line voltage (120 Vpk), then any transient event out of a standby condition would be seamless and good. As discussed previously, at these power levels where the UCC28064A device is used, the de-facto second stage converter used is the LLC. LLC converters are very efficient; however, there are a number to make them deliver full power across a very wide range of input and output voltages. Hence there is considerable overhead in designing a wide input LLC converter which can deliver peak power all the way from 120 V to 450 V.

4 Key Value Proposition of UCC28064A

To help solve some of the new efficiency requirements, TI has introduced the UCC28064A device which is the next generation interleaved CRM boost PFC. The UCC28064A device retains the core algorithm of the UCC28063 device and adds some key features to help improve light load efficiency and standby power. Some of these changes have made significant improvement to efficiency and standby power. Table 4 shows the standby power of a total system including the UCC28064A device and UCC25630 LLC controller running where both the PFC and LLC outputs are regulated to its final value.

Table 4. Standby Power Performance of UCC28064A PFC + UCC25630x LLC Converter

INPUT VOLTAGE (Vrms)	OUTPUT LOAD (mW)	INPUT POWER (mW)
115	0	100
230	0	120

4.1 Pinout

To improve the standby power performance, the PWMCTRL pin is replaced with the BRST pin. A constant voltage on this pin defines the power level at which the PFC enters and exits the burst mode.

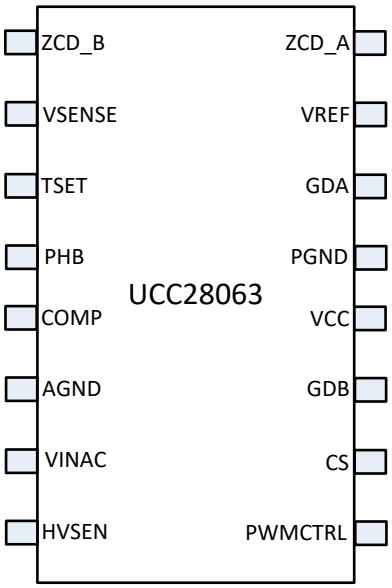

Figure 6. UCC28063 Pinout

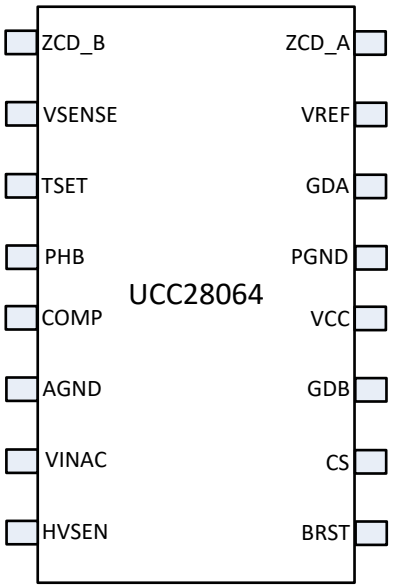

Figure 7. UCC28064A Pinout

4.2 Phase Management

Shutting down a phase improves light load efficiency of the PFC because in a CRM controller, the frequency of operation increases as the load reduces. When one phase of the PFC is shutdown, the frequency reduces by half on the remaining phase as the load on it is doubled. In the UCC28063 device, the 2-phase CRM PFC can be made to work in single phase by forcing the PHB pin low with an external signal. While this is quite useful, there are additional external circuits required to realize this function. In the UCC28064A device, there is no need for an external signal to enable phase shedding. The user can set the phase B turning off threshold and the hysteresis on this pin with an external resistor on the pin. The UCC28064A device has some intelligent circuits to determine the instant at which one phase needs to be turned OFF autonomously and shuts it down. This helps in improved efficiency. Figure 8 shows the block diagram for how the phase management has been implemented.

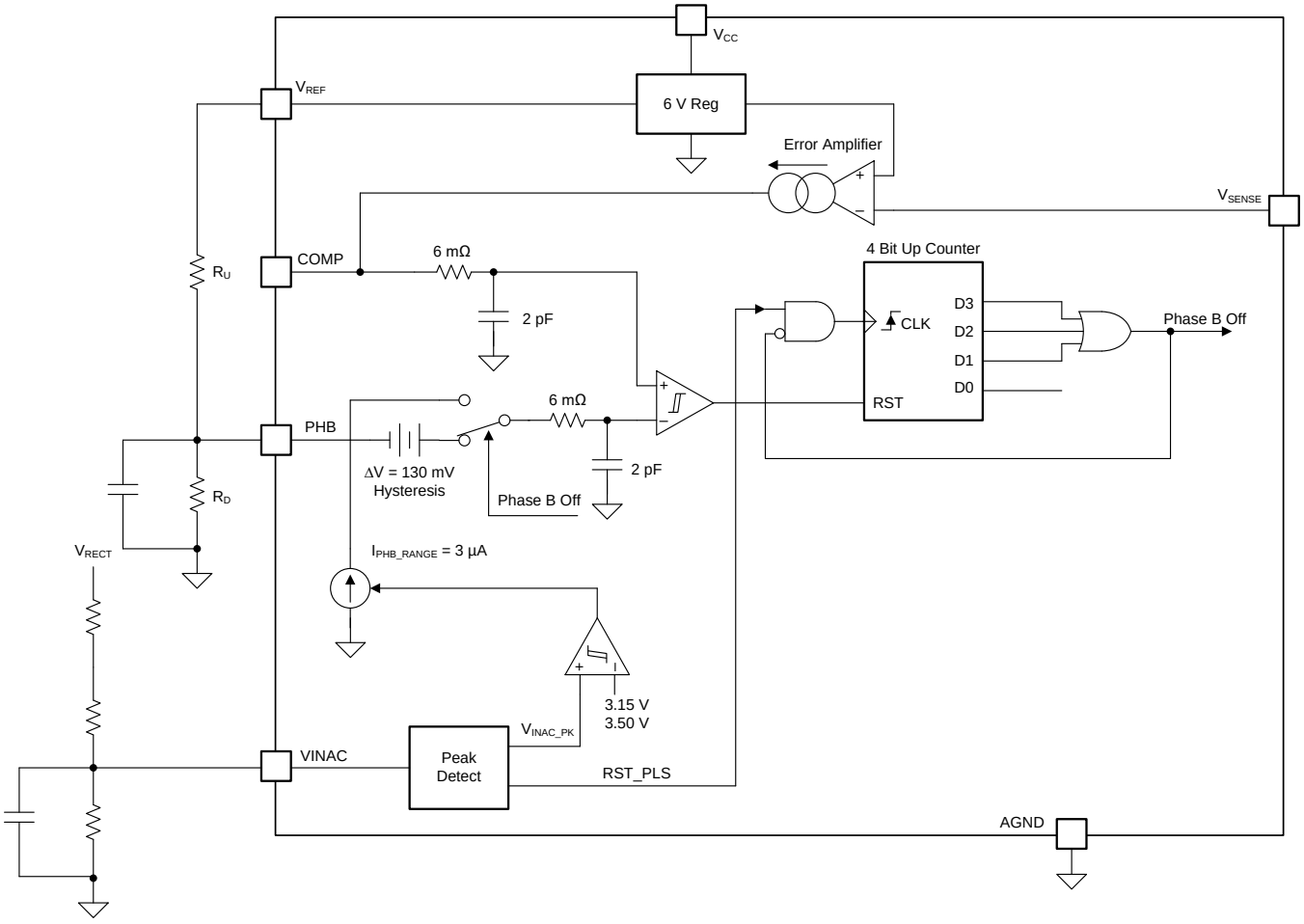

Figure 8. Block Diagram of Phase Shedding Block

The COMP voltage has to go below the PHB threshold for 3 half-line cycles before turning off phase B. This is to avoid any line frequency ripple on COMP to cause the PHB pin to chatter. Once the PHB is turned OFF, the controller automatically doubles the T_{ON} from the previous cycle to maintain the same power delivered to the load.

4.3 Input Voltage Feed-Forward

It is desirable to make both the burst mode threshold and the phase shedding threshold as a function of power. But the IC does not explicitly calculate the input or output power. However, if the loop has built-in input voltage feed-forward, then the COMP pin voltage becomes a true representation of power. To enable this, the UCC28064A device has implemented a feed-forward circuit that is accurate not just at low line and high line but is accurate across the range of load and line values. Figure 9 shows the block diagram representation.

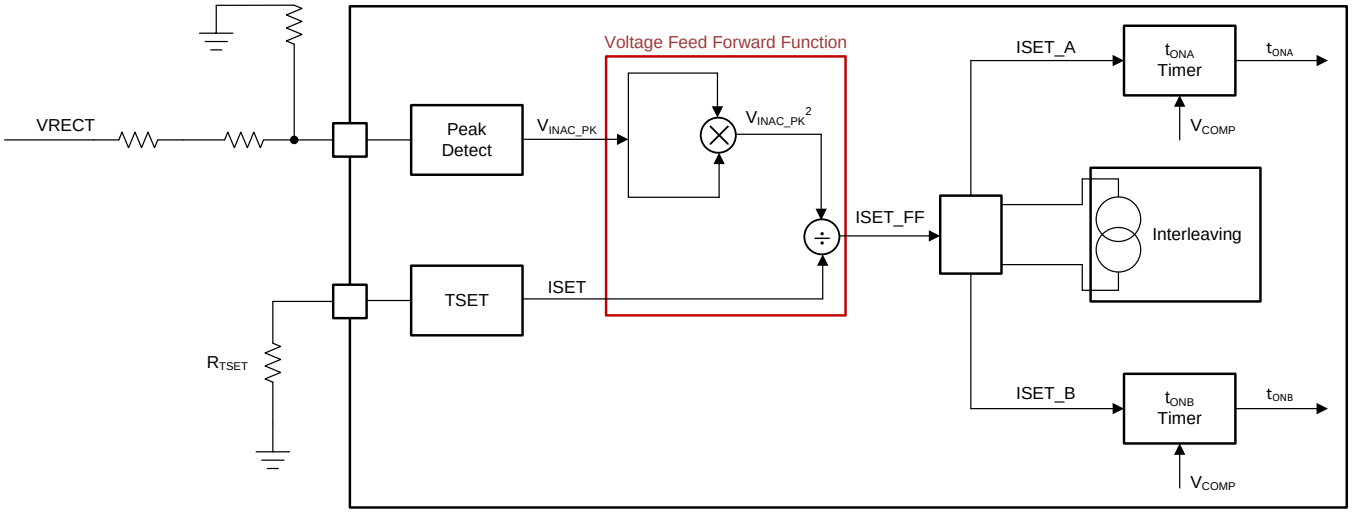

Figure 9. Block Diagram Representation of Input Voltage Feed-Forward

In addition to providing near ideal line feed-forward, the UCC28064A device has an asymmetric peak detect. This helps in providing near ideal line transient response especially when there is a low line to high line transient. Under this condition, the peak detect circuit adjusts the feed-forward function in real time. This means that the T_{ON} is also scaled correctly and real time and large inductor currents in the circuit are avoided and the robustness of the system is improved. Figure 10 shows the line response comparison between the UCC28063 and UCC28064A devices.

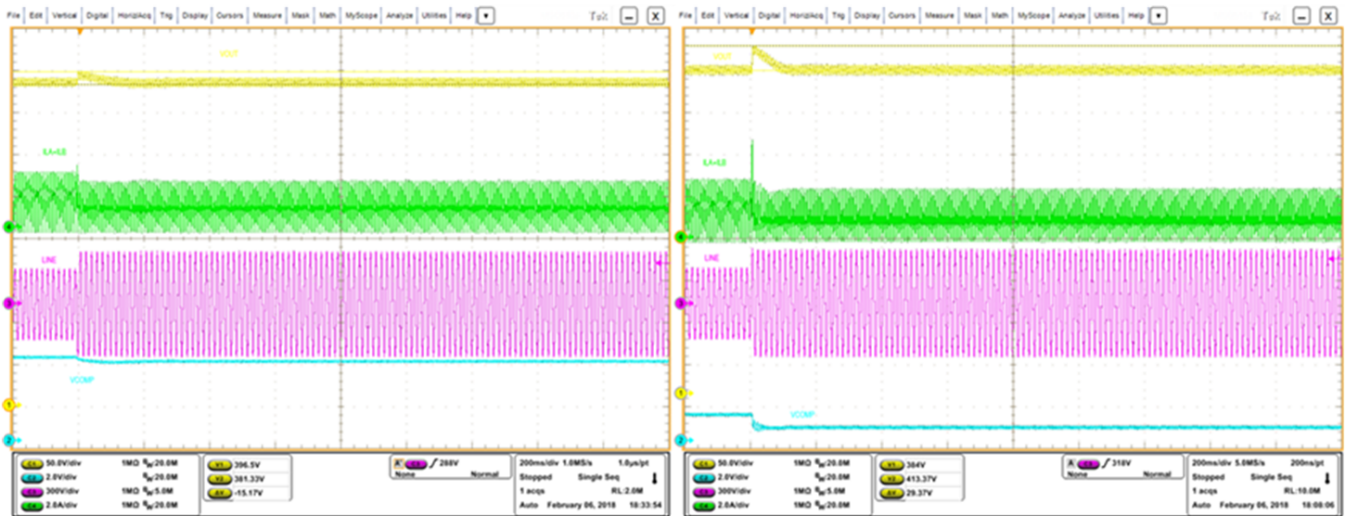

Figure 10. Line Transient Comparison Between UCC28063 and UCC28064A

4.4 IC Current Consumption

During the burst mode when the PFC is not switching, the current consumption of the ICC has been greatly reduced to help achieve the low standby requirements. Table 5 shows the current consumption during normal operation and during burst mode.

Table 5. UCC28064A IC Current Consumption

CONDITION	ICC (mA)
Normal operation	5
Burst mode	0.5

Some of the key observations regarding the efficiency of the PFC from the architecture of the UCC28064A when compared to the UCC28063 device, we can make the following inferences:

- The efficiency curve of the PFC is flat and does not degrade with load as is the case with the UCC28063 device or any other CRM controller
- Phase shedding improves efficiency of the system at 100 W, 230 Vrms by about > 0.8%
- Burst mode helps improve efficiency of PFC @ < 10% load by > 8%
- ICC of < 0.65 mA helps in reducing total system standby power to less than 0.1 W

Figure 11 shows the BOM savings of migrating from the UCC28063 device to the UCC28064A device. The overhead that is eliminated is from the BOM corresponding to circuits that are used to turn off the PFC at standby.

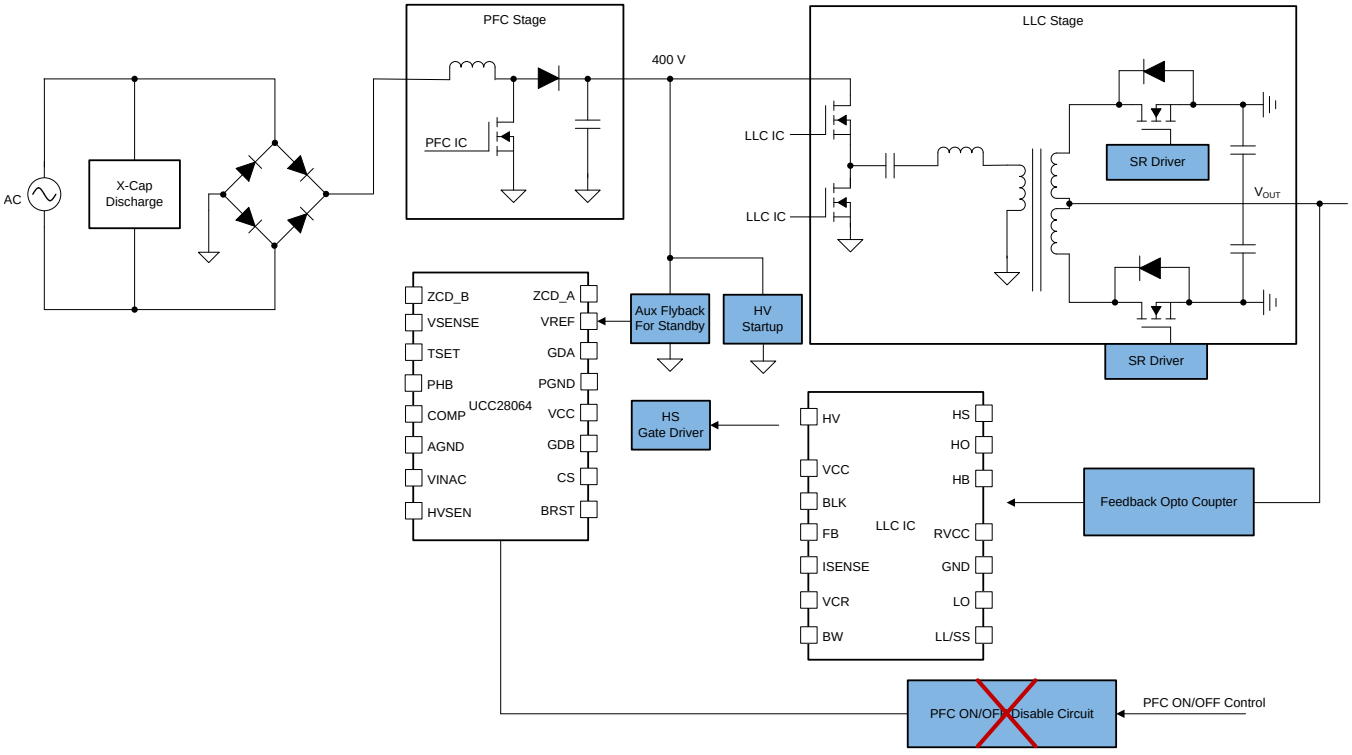

Figure 11. BOM Savings for Migrating From UCC28063 to UCC28064A

5 PFC Design Differences Between the UCC28063 and UCC28064A

Figure 12 with the highlighted colors shows the pins which have different design equations. This section explains some of the qualitative differences. For a detailed explanation of the design process, see *UCC28064A Natural Interleaving™ Transition-Mode PFC Controller With Improved Light-Load Efficiency* .

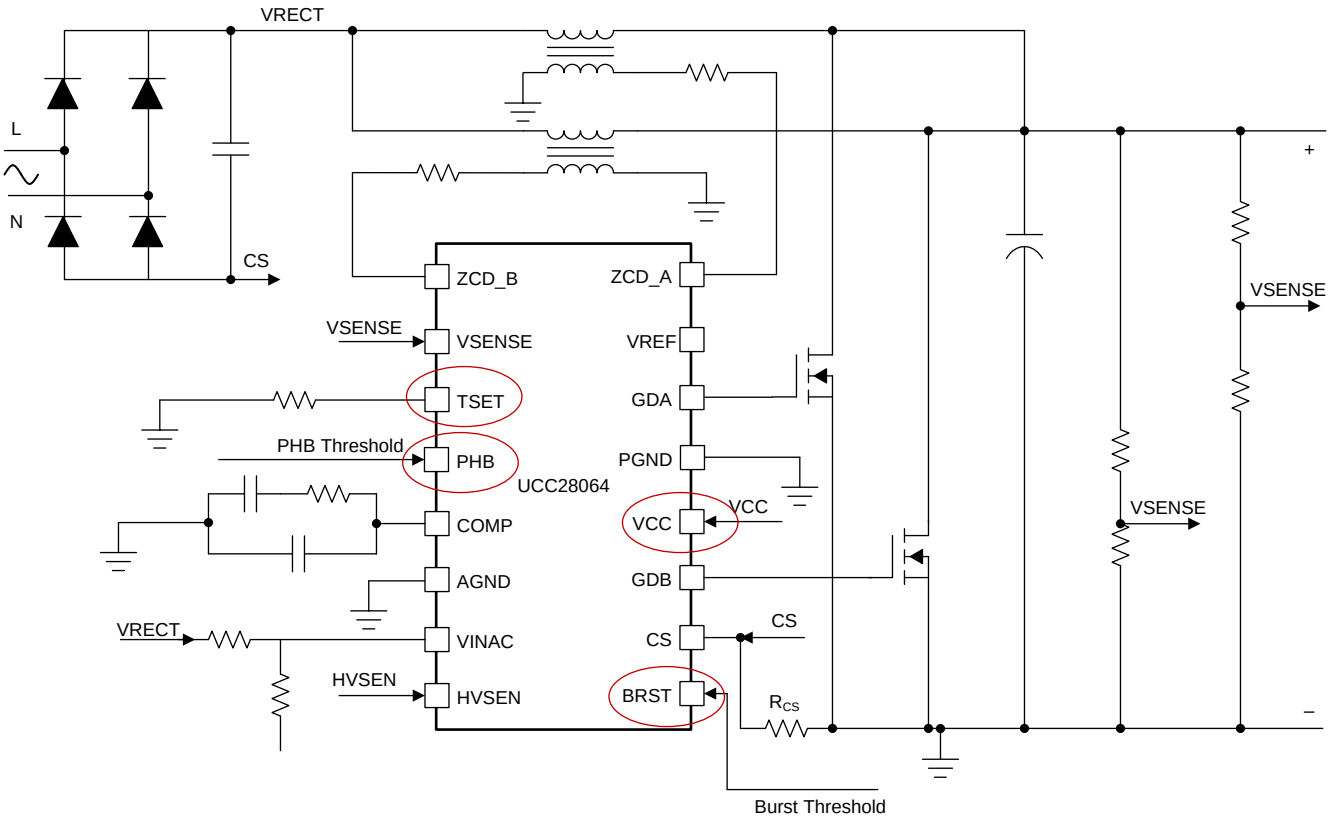

Figure 12. UCC28064A Application Schematic Highlighting Changes From the UCC28063

5.1 R_{TSET} Resistor Calculation

Since the UCC28064A device has implemented a new input voltage feed-forward scheme, the calculation of the R_{TSET} resistor is different from the UCC28063 device. Equation 1 shows the R_{TSET} resistor calculation.

$$T_{ON} = (V_{COMP} - 0.125\ V)\frac{C_t}{I_{SET\_X}} = (V_{COMP} - 0.125\ V)\frac{C_t}{V^2_{INAC_{PK}}} \times \alpha \times I_{SET}$$

$$T_{ON} = (V_{COMP} - 0.125\ V)\frac{C_t}{V^2_{INAC_{PK}}} \times \alpha \times \frac{V_{SET}}{R_{TSET}} = (V_{COMP} - 0.125\ V) \times K_T(V^2_{INAC_{PK}}) \quad (1)$$

Obtain K_T from *UCC28064A Natural Interleaving™ Transition-Mode PFC Controller With Improved Light-Load Efficiency Data Sheet*.

5.2 Setting the BRST Pin and PHB Pin Threshold

In the UCC28063 device, the PHB pin was just a digital input signal. The BRST pin is new for the UCC28064A device and had a different function than the UCC28063 device. Figure 13 shows how it is supposed to be connected.

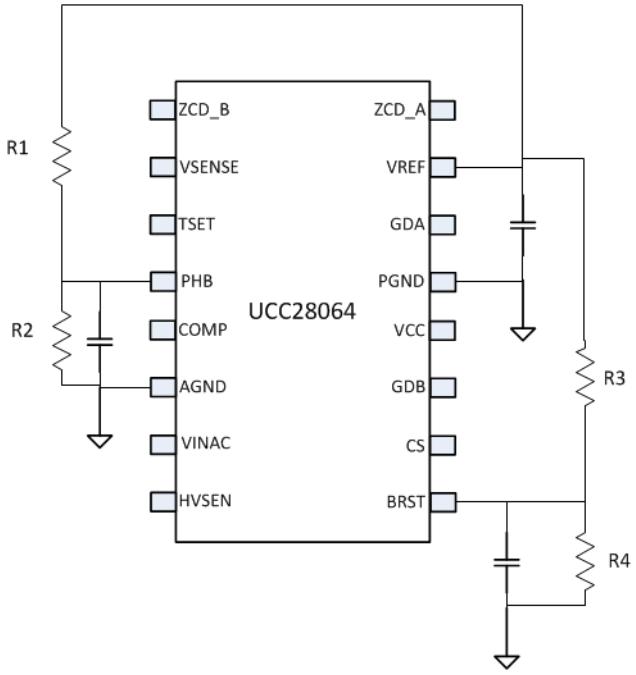

Figure 13. Burst Pin and PHB Pin Connections

As in the UCC28063, V_{REF} is a regulated 6 V voltage. C_{vref} is a local decoupling capacitor that is placed at the pin to stabilize the V_{REF} regulator. The burst threshold is obtaining by solving the voltage divider on R3 and R4. The Phase shedding threshold voltage can be solved by solving the divider on R1 and R2 resistors.

5.3 VCC_{ON} and VCC_{OFF} Thresholds

The VCC_{ON} and the VCC_{OFF} thresholds for the UCC28064A are lower than the UCC28063, see Table 6.

Table 6. VCC_{OFF} Thresholds

PARAMETER	UCC28063	UCC28064A
VCC_{ON}	12.6	10.35
VCC_{OFF}	10.35	9.6

The change allows the IC to be powered off of the RVCC pin of UCC25630x directly without needing any additional circuits.

6 Conclusion

The UCC28064A is a highly-differentiated controller that can meet the lowest standby power and efficiency standards of the industry. It has significant advantages over the UCC28063 device in both system cost as well as performance. Using the UCC28064A device, an UCC25630x as a chipset can reduce total standby power consumption while leaving both the PFC and the LLC regulating. In many applications, the UCC28064A device can eliminate the need for an additional flyback converter if it is used exclusively for standby purposes.

7 References

- *UCC28064A Natural Interleaving™ Transition-Mode PFC Controller With Improved Light-Load Efficiency Data Sheet*
- *Optimizing Efficiency and Standby Power With the UCC28056 in Offline Applications Application Report*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2018) to A Revision	Page
• Changed UCC28064 to UCC28064A throughout.	1

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