Improving ZVS and Efficiency in LLC Converters

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1 Introduction

In medium (150 W) to high power (600 W +) high input voltage (V_{IN}) DC to DC step down converter applications the resonant LLC topology has become a popular choice, due to its ability to achieve zero voltage switching (ZVS) on the converter's primary switch node (V_{sw}) over a wide load range (R_{LOAD}). When design correctly the design will achieve zero current switching (ZCS) on the power converter's secondary rectifiers removing secondary side rectifier switching losses. The LLC with ZVS on the primary and ZCS on the secondary removes switching losses power converter and reduces power converter heating allowing the converter to be designed for high switching frequencies and greater power densities. To improve the efficiency of the LLC converter even further output rectifiers can be replaced with synchronous rectifiers (SR) using TI's new dual SR driver the UCC24624 (Fig. 1) to drive these FETs. This application brief will give advice, tips and guidance on how to design an LLC that uses SRs to achieve ZVS on the primary and ZCS on the secondary. Please note that this application brief is supplemental to other Texas Instruments application notes, seminar papers and tech notes referenced at the end of this application brief [1..6].

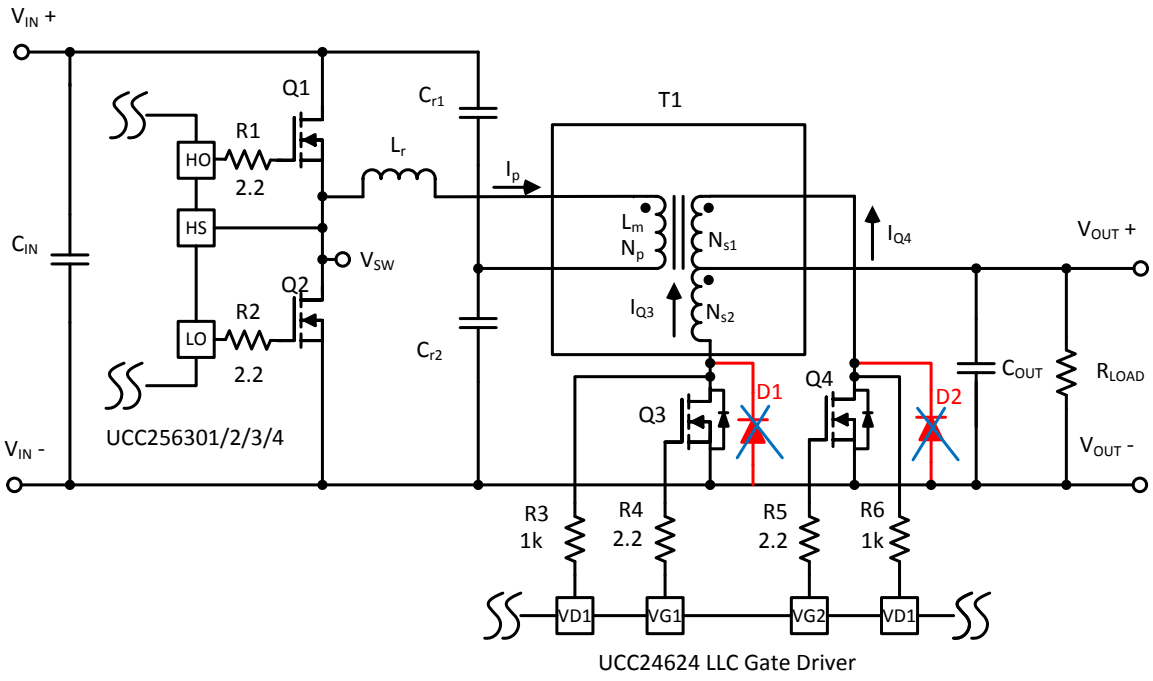

Figure 1. LLC Step Down Converter with Synchronous Rectifiers (SR)

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2 Quick Review of LLC and System Benefits

The LLC converter (Figure 1) consists of an input filter capacitor (C_{IN}) a half bridge power stage drive formed by Q1 and Q2 and driven/controlled by an LLC controller (UCC256301/2/3/4). This converter for galvanic isolation uses transformer (T1) to step down/or up the DC input voltage. This design also requires output rectifiers that consist of two diodes (D1, D2) or two synchronous rectifiers (Q3, Q4) and an output filter capacitor (C_{OUT}). To control the output voltage (V_{OUT}) Q1 and Q2 are operated at 50% duty cycle and are 180 degrees out of phase with a voltage controlled oscillator. This will put a square wave across an LLC reactance divider network consisting of a resonant inductor (L_r), the transformers primary magnetizing inductance (L_m) and a resonant capacitor/s ($C_r = C_{r1}+C_{r2}$). When the converter is operating at frequency (f_r)where L_r and C_r are in resonance. The reactance of L_r and C_r at f_r will be 180 degrees out of phase in resonance and the reactance will cancel each other out in the total reactance of the reactance divider. In this configuration half the input voltage (V_{IN}) will be seen across the primary of the transformer and transferred to the secondary across the transformer turns ratio ($N_{s1/2}$) to the output (V_{OUT}).

$$V_{OUT} \approx \frac{V_{IN}}{2} \times \frac{N_s}{N_p} \tag{1}$$

When designed correctly and delaying (td) the turn on of FET Q1 and Q2 this allows time for the energy stored in the magnetizing inductance (L_m) to swing the switch node (V_{SW}) from rail (V_{IN}+) to rail (V_{IN}-) and achieve zero voltage switching (ZVS). This reduces switching losses, heating and increases overall system efficiency and power density. Please refer to figure 2 for the LLC's switch node, FETs Q1 and Q2's gates (Q1g, Q2g) and primary transformer (T1) current (I_p) operating at the converters resonant frequency and achieving ZVS.

Figure 2. LLC ZVS Oscilloscope Waveforms

Another benefit of using an LLC converter is when the converter is operating at the resonant frequency (f_r) or below f_r the secondary rectifiers achieve ZCS to improve system efficiency. Figure 3 shows the gate drives of the synchronous rectifiers (Q3g and Q4g); as well as, the output rectifiers' drain currents (I_{Q3} and I_{Q4}). From this waveform it can be observed that the SRs are ZCS.

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Figure 3. LLC ZVS Oscilloscope Waveforms

The SRs power dissipation (P_{Q3} and P_{Q4}) can be estimated with the following equation at the resonant frequency (f_r). Where Q_{Q3g} and Q_{Q4g} are the SR's gate charge, V_{Q3g} is the voltage the gate of the SRs is driven too, $R_{DS(on)Q3}$ is the on resistance of the SRs and I_{OUT} is the output current of the power converter.

$$P_{Q3} = P_{Q4} = Q_{Q3g} \times V_{Q3g} \times f_r + R_{DS(on)Q3} \times \left(\frac{\pi}{4} \times I_{OUT}\right)^2 \quad (2)$$

3 Tip 1, Select the FETs for the design before designing your transformer (T1):

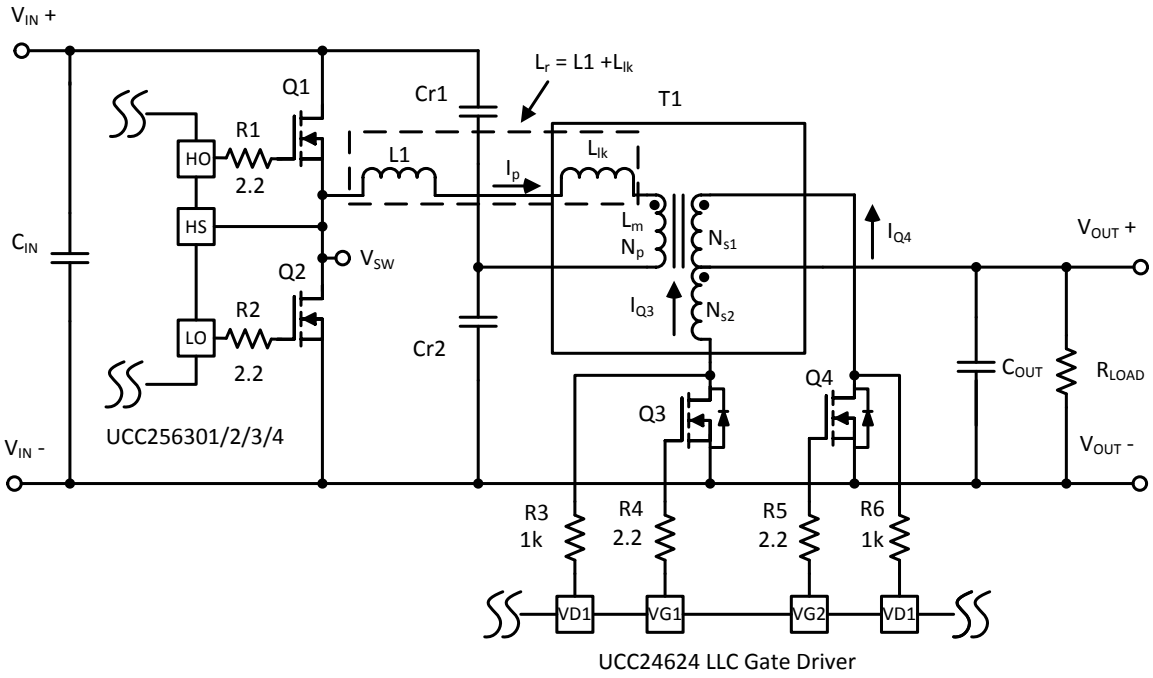

Figure 4. LLC with SRs

To design the transformer it is recommended that the FETs are selected for the design first, to avoid redesigning the transformer later. It is necessary to know Q1 and Q2's approximate switch node capacitance related to time ($C_{O(tr)}$); as well as, these FETs' on resistances $R_{DS(on)}$. It will also be necessary to know the output rectifiers' (Q3 and Q4) on resistance to design the transformer as well.

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This application brief will review how to calculate the transformer's primary magnetizing inductance (L_m) and the transformer primary to secondary turns ratio (N_{ps}) based on the input and output requirements and the FETs' $C_{O(tr)}$ and $R_{DS(on)}$. It will also go through a 120 W design example. Table 1, shows the input and output power requirements of a 120 W LLC power converter, as well as, the FET critical parameters that will be required for calculating N_{ps} and L_m. It is recommended to keep the input voltage range within +/- 15% of the typical value (V_{IN}) for the best LLC performance.

Table 1. 120W LLC Critical Design Parameter's for T1 Calculations

	MINIMUM	TYPICAL	MAXIMUM	UNITS	DESCRIPTION
Input Voltage	340 ($V_{IN(min)}$)	390 (V_{IN})	410 ($V_{IN(max)}$)	V	LLC Input Voltage
V_{OUT}		12		V	LLC Output Voltage
I_{OUT}		10		A	LLC Output Current
$C_{O(tr)Q1}$		160		pF	Effective FET Output Capacitance Time Related
$C_{O(tr)Q2}$		160		pF	Effective FET Output Capacitance Time Related
$R_{DS(on)Q1}$		220		mΩ	FET on Resistance
$R_{DS(on)Q2}$		220		mΩ	FET on Resistance
$R_{DS(on)Q3}$		2.5		mΩ	FET on Resistance
$R_{DS(on)Q4}$		2.5		mΩ	FET on Resistance
f_r		100		kHz	Resonant Frequency

4 Tip 2, Design the Transformer (T1) for ZVS

To select the transformer N_{ps} requires estimating the transformer primary peak current (I_{ppk}) and the output rectifier peak currents (I_{Q3pk} and I_{Q4pk}).

$$I_{ppk} \approx \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \times \frac{\pi}{2} = \frac{10A \times 12V}{390V} \times \frac{\pi}{2} = 483mA \tag{3}$$

$$I_{Q3pk} = I_{Q4pk} \approx I_{OUT} \times \frac{\pi}{2} = 10A \times \frac{\pi}{2} = 15.7A \tag{4}$$

Once the FET peak currents are calculated N_{ps} can be calculated. For this example based on the design requirements of table 1 this design would require a turn's ratio of 16.2

$$Nps = \frac{N_p}{N_{s1}} = \frac{N_p}{N_{s2}} = \frac{V_{IN} - I_{ppk} \times R_{DS(on)Q1}}{2 \times (V_{OUT} + I_{Q3pk\times} \times R_{DS(on)Q3})} = \frac{390V - 483mA \times 220m\Omega}{2 \times (12V + 15.7A \times 2.5m\Omega)} = 16.2 \tag{5}$$

Please note that it is understood that fractional turns may be difficult to achieve in a transformer design, just select a turns ratio that is close to the calculated value. For this design we selected and N_{ps} of 16.

$$Nps = 16 \tag{6}$$

Once the transformer turn's ratio is selected, the transformer's primary magnetizing inductance (L_m) should be chosen to insure the design can achieve ZVS over the entire input voltage range of $V_{IN(min)}$ to $V_{IN(max)}$. Start by selecting the delay time (t_d) to achieve ZVS to be 1% of the resonant frequency period.

$$t_d = \frac{0.01}{f_r} = \frac{0.01}{100kHz} = 100ns \tag{7}$$

Next calculate d_v/d_t based on $V_{IN(max)}$ and t_d. Please note that some controllers such as the UCC256301/2/3/4 devices have adaptive delays to help achieve ZVS. **However, the UCC256301/2/3/4 devices have a minimum d_v/d_t requirement of 1 V/ns. To avoid circuit misbehavior it is recommended that the d_v/d_t that is used to calculate I_m is at least 4 times this minimum requirement, to exceed this minimum requirement with margin, (Equation 10).**

$$\frac{1V \times 4}{1ns} \geq \frac{d_v}{d_t} = \frac{V_{IN(\max)}}{t_d} = \frac{410V}{100ns} = \frac{4.1V}{ns} \tag{8}$$

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Once the switch node d_v/d_t is determined the transformer's magnetizing current (I_m) and maximum primary magnetizing inductance (L_m) can be calculated.

$$I_m = \frac{d_v}{d_t} \times 2 \times C_{O(tr)Q1} = \frac{4.1V}{1ns} \times 2 \times 160pF \approx 1.3A \quad (9)$$

$$L_m \leq \frac{V_{IN(\min)} \times 0.5}{I_m \times 2 \times f_r} = \frac{340V \times 0.5}{1.232A \times 2 \times 100kHz} = 654\mu H \quad (10)$$

For this design example we used a transformer that had a turn's ratio of 16 and a L_m of 550µH and had a leakage inductance of 27.5 µH. Please note that L_{lk} is part of the resonant inductance and needs to be considered when sizing L1.

$$L_m = 550\mu H \quad (11)$$

$$L_{lk} = 27.5\mu H \quad (12)$$

5 Tip 3, Select Resonant Capacitors ($C_r = C_{r1} + C_{r2}$):

To calculate the resonant capacitor (C_r) requires calculating the effective reflected impedance (R_e) seen by the primary of the transformer.

$$R_e = \frac{8 \times {N_{ps}}^2 \times V_{OUT}}{\pi^2 \times I_{OUT}} = \frac{8 \times 16^2 \times 12V}{\pi^2 \times 10A} \approx 249\Omega \quad (13)$$

C_r is the sum of C_{r1} and C_{r2} and can be calculated based on R_e, f_r and a target Q_e. For this example we chose a Q_e of 0.15 to keep the control to output transfer function peaking two a minimum.

$$C_r = \frac{1}{2 \times \pi \times Q_e \times R_e \times f_r} = \frac{1}{2 \times \pi \times 0.15 \times 249\Omega \times 100kHz} \approx 42.6nF \quad (14)$$

For this design example we used two standard 22 nF capacitors for C_{r1} and C_{r2}, which resulted in a C_r of 44 nF.

$$C_r = C_{r1} + C_{r2} = 22nF + 22nF = 44nF \quad (15)$$

Tip 4, Set L_r by properly selecting L1, but don't forget to include T1's L_{lk} in the calculation:

The resonant inductance (L_r) needs to be calculated based on C_r, Q_e and R_e.

$$L_r = C_r \times {Q_e}^2 \times {R_e}^2 = 44nF \times (249\Omega)^2 \times (0.145)^2 \approx 57.4\mu H \quad (16)$$

With L_r and L_{lk} inductor L1 can be calculated.

$$L1 = Lr - Llk = 57.4\mu H - 27.5\mu H = 29.9\mu H \quad (17)$$

In this example we used a high current, high voltage, 33 µH inductor for L1.

$$L1 = 33\ \mu H \quad (18)$$

6 Tip 5, Double check to make sure the transformer with L_r, C_r and N_{ps} meets the design requirements

Calculate the designs minimum gain required Mg_min:

$$M_{g\_min} = \frac{N_{ps} \times (V_{OUT} + I_{Q3pk} \times R_{DS(on)Q3})}{\frac{(V_{IN(\max)} - I_{Q1pk} \times R_{DS(on)Q1})}{2}} = \frac{16 \times (12V + 15.7A \times 2.5m\Omega)}{\frac{(410V - 483mA \times 220m\Omega)}{2}} \approx 0.94 \quad (19)$$

Calculate the designs maximum gain required Mg_max:

$$M_{g\_max} = \frac{N_{ps} \times (V_{OUT} + I_{Q3pk} \times R_{DS(on)Q3})}{\frac{(V_{IN(\min)} - I_{Q1pk} \times R_{DS(on)Q1})}{2}} = \frac{16 \times (12V + 15.7A \times 2.5m\Omega)}{\frac{(340V - 483mA \times 220m\Omega)}{2}} \approx 1.133 \quad (20)$$

Plot Gain vs Frequency (Mg(f)):

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$$L_n = \frac{L_m}{L_1 + L_{lk}} = \frac{550\mu H}{33\mu H + 27.5\mu H} \approx 9.09 \tag{21}$$

$$M_{g(f)} = \left| \frac{L_n \times \left(\frac{f}{f_r}\right)^2}{\left[(L_n + 1) \times \left(\frac{f}{f_r}\right)^2 - 1\right] + j \times \left[\left(\left(\frac{f}{f_r}\right)^2 - 1\right) \times \left(\frac{f}{f_r}\right) \times Q_e \times L_n\right]} \right| \tag{22}$$

From the $M_{g(f)}$ curve in figure 6 it can be observed that the transformer's turns ratio and resonant components will meet the systems gain requirements of M_{g_min} to M_{g_max}. Please note when using a PFC pre-regulator the converter will be operating at f_r nominally and will only vary the switching frequency (f) during large signal transients.

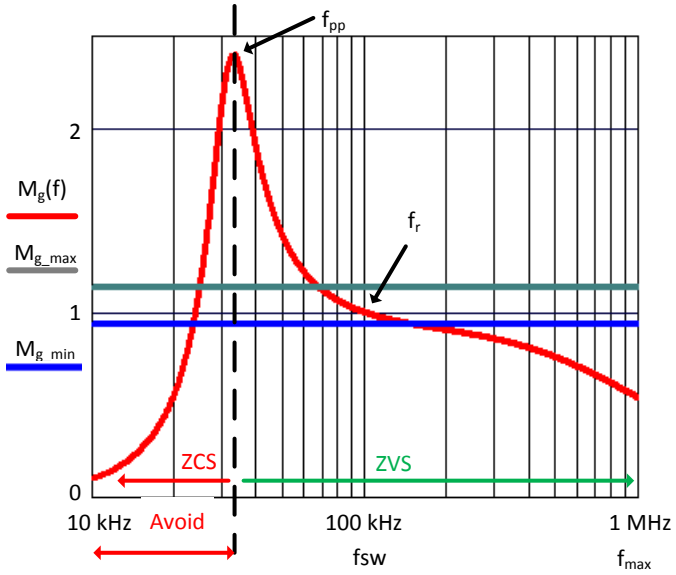

Figure 5. Plot of $M_{g(f)}$ vs frequency (f_{sw})

7 Tip 6, Avoid ZCS on primary switch node (V_{sw})

Please note that ZCS on the output rectifiers will not cause issues with circuit performance. However, when using an LLC, ZCS on the primary switch node (V_{sw}) can lead to feedback control misbehavior or latch up if older LLC controllers are used; such as, the UCC25600 that do not have primary ZCS detection/correction.

If an older LLC controller, such as the UCC25600, to avoid operating in the ZCS frequency range just requires setting the minimum frequency (f_{min}) to greater than the f_{pp} frequency (fig 6).

$$f_{min} > f_{pp} = \frac{f_r}{\sqrt{L_n + 1}} = \frac{100kHz}{\sqrt{9.00 + 1}} \approx 31.5kHz \tag{23}$$

In this example, I would suggest setting f_{min} to 40 kHz. This is generally done by selecting a resistor to program this frequency. Refer to the UCC25600 data sheet for details on how to set f_{min}.

$$f_{min} = 40kHz \tag{24}$$

If the design is using newer LLC controllers, UCC256301/2/3/4, there is no need to worry about programing f_{min} or operating in the ZCS frequency range. These devices have internal circuitry that has primary ZCS detection and frequency correction to avoid feedback control latch up and does not require an external resistor for programing f_{min}. If ZCS is detected these LLC controller will automatically increase the switching frequency (f_{sw}) so the converter will operate above f_{pp} and operate in the ZVS frequency range.

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8 Evaluating Design Performance

A 120W LLC prototype was constructed based on the design example, table 1. The design used a UCC256302 LLC controller; as well as, the UCC24624 LCC SR driver.

The N_{ps}, L_m, L_r and C_r that were selected for an f_r of 100 kHz that would occur at a V_{IN} of 385 V. In the prototype circuit an f_r of roughly 100.9 kHz was achieved at V_{IN} of 380 V. These values were very close to the design target and achieved ZVS quite easily. Please refer to figure 7 for circuit performance at VIN of 385 V.

Figure 6. V_{IN} = 380 V, I_{OUT} = 10 A, ZVS at f_r

Please note that using this design technique ZVS was maintained at minimum and maximum input voltages as well to handle large signal transients. Please refer to Figure 7 and Figure 8 for ZVS circuit performance.

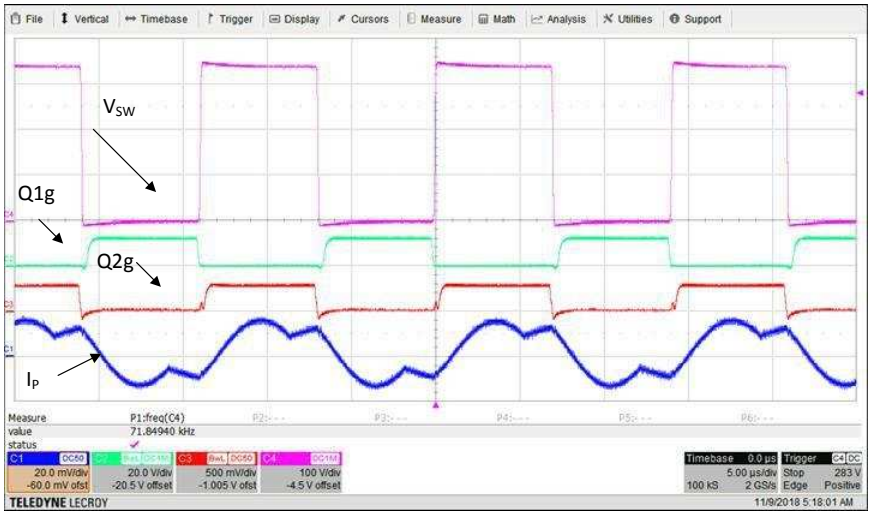

Figure 7. ZVS @ V_{IN} = 340 V, I_{OUT} = 10 A

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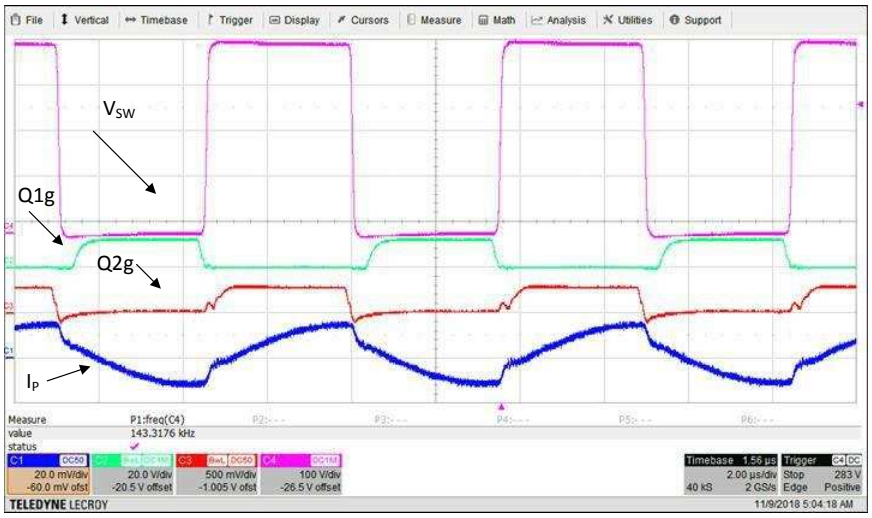

Figure 8. ZVS @ V_{IN} = 400 V, I_{OUT} = 10 A

9 Summary

As this application brief discussed when designing an LLC converter (UCC256301/2/3/4) for off line applications using SRs (UCC24624) to get the highest efficiency and best performance possible, we recommend the following.

1. Select FETs for the primary and SRs before designing the transformer.
2. Transformer design considerations to ensure ZVS.
   - Select N_{ps} at the nominal LLC input voltage and include the effect of the voltage drops across the FETs used in the design.
   - Select L_m to achieve ZVS based on input and output power requirements, Q1 and Q2's $C_{o(tr)}$, and d_v/d_t requirements. **Please note that when using the UCC256301/2/3/4 devices the d_v/d_t needs to be set greater than 4 V/ns to avoid control misbehavior.**
3. After the preliminary transformer calculations are done C_r can calculated/selected based on Q_e, R_e and f_r.
4. When selecting L_r and L1 don't forget to include the effects of the transformer's L_{lk}.
5. Avoid operating the LLC when the primary switch node is operating in ZCS to avoid feedback control latch up.
   - In older controllers this just requires setting f_{min} to greater than f_{pp} (UCC25600).
   - Newer LLC controllers (UCC285601/2/3/4) have ZCS detection and frequency adjustment to avoid latch up. So there is no need to worry about switch node ZCS feedback latch up issues in these devices.

10 References

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