Application Report
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Parallel Paths with the BQ76952 Battery Monitor Family

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ABSTRACT

While the typical schematics for the BQ76952 family of battery monitors show series FETs, the family supports parallel charge and discharge paths. This document shows an example of a parallel path implementation using the BQ76942 and provides an example for designers implementing parallel path circuits with this or other devices in the family.

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1 Typical Series FET Circuit

A typical battery has one set of terminals for both charge and discharge. Current passes through charge and discharge FETs arranged in series. Since the current flows through both FETs, the size and quantity used for charge and discharge are the same. The BQ76952 family of battery monitors consisting of the BQ76942 and BQ76952 support series FETs. References to the BQ76952 in this document will generally apply to all family members unless specifically indicated. A typical schematic with the BQ76942 and series FETs is shown in Figure 1. The schematic is for a 7-cell implementation and includes pre-charge and pre-discharge FETs. The pre-charge path is used to limit current into the battery from a fixed voltage charger when the battery is deeply discharged. The pre-discharge path is used to charge high capacitive loads without a high current spike. With the series FETs, there is the possibility of charging through a disabled discharge FET or discharging through a disabled charge FET. The current through the body diode of the disabled FET can produce significant heat, so the BQ76952 devices use a body diode protection feature to enable the FET when current is flowing in the non-protected direction.

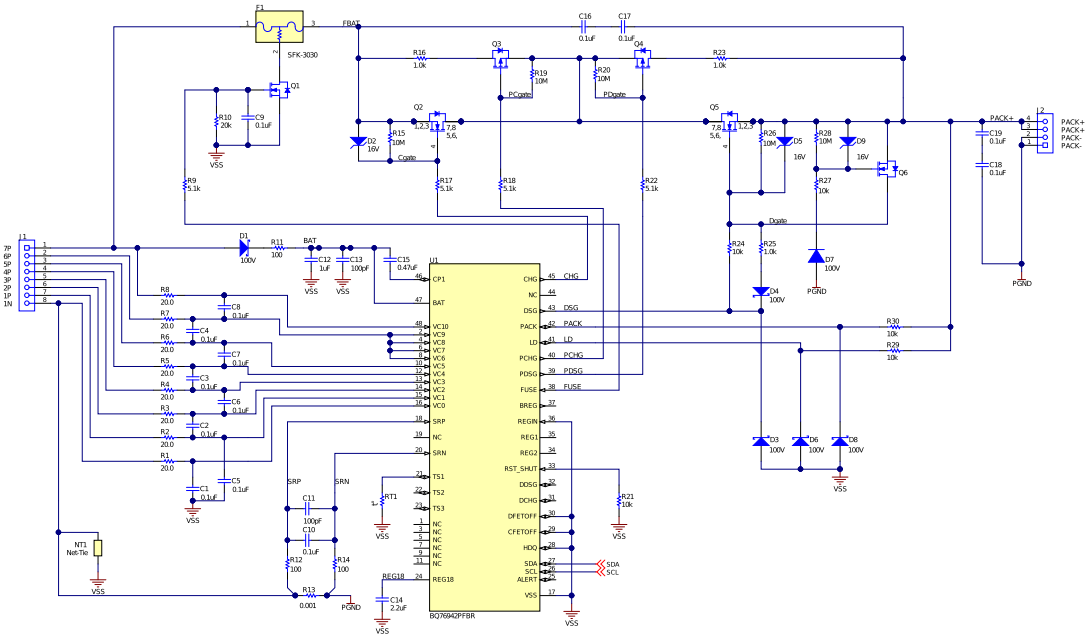

Figure 1. Typical 7S Series FET Schematic

2 Parallel FET Circuit

With a parallel FET configuration, there are different connections for the charge and discharge current paths. The protection FETs can be sized appropriately for the current of the protected direction. The BQ76952 family of devices can support parallel FET operation. An example of a parallel FET schematic with the BQ76942 is shown in Figure 2. When using a parallel FET circuit, the body diode protection feature must be turned off in the BQ76952 configuration by setting the ***Settings:FET Control SFET*** bit to 0.

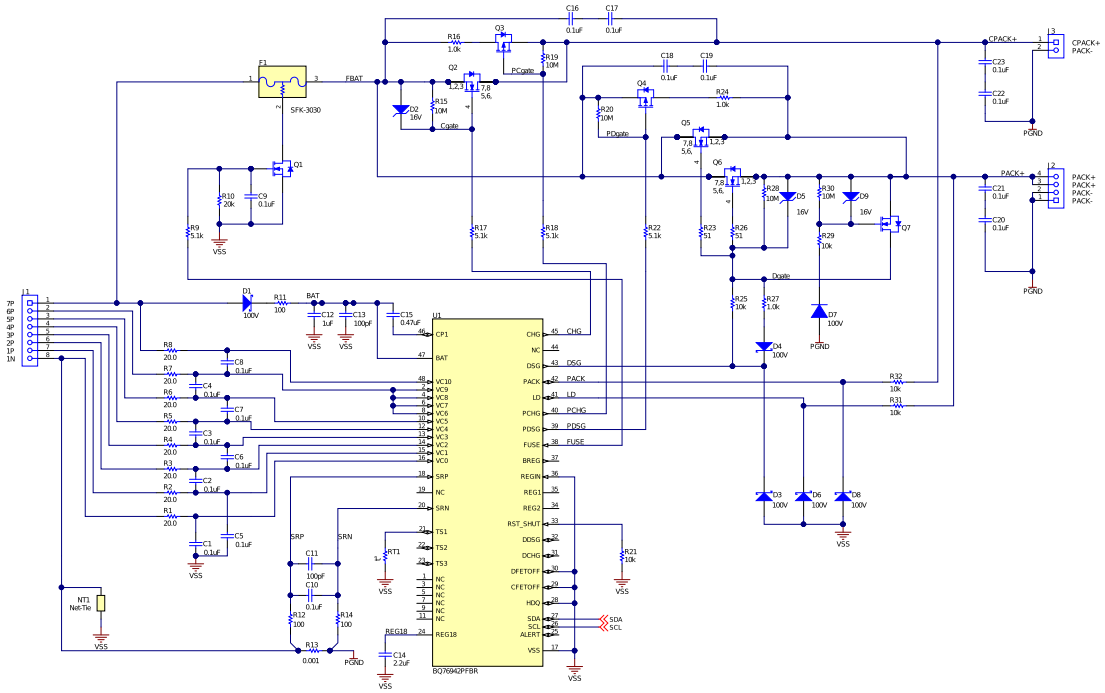

Figure 2. Typical 7S Parallel FET Schematic

3 Test results

A variation of the circuits in Figure 1 and Figure 2 were built and tested. Diodes D3, D6, and D8 were not installed. The primary difference in the configuration of the devices is the ***Settings:FET Control SFET*** bit to 0 with the parallel circuit test. Other configuration settings were adjusted as needed to facilitate testing. A similar circuit structure is available on the EVMs for the family. Reference designators on schematics in this document do not match those in the EVM schematics.

When the charge FET is off in the series FET board due to overvoltage of a cell, the FET turns on again when discharge current exceeds a threshold as shown in Figure 3. With the parallel FET board and configuration, the charge FET is not turned on during the discharge current (see Figure 4). Similarly, with a cell in undervoltage, the series FET board turns on DSG with charge current while the parallel FET configuration does not (see Figure 5 and Figure 6).

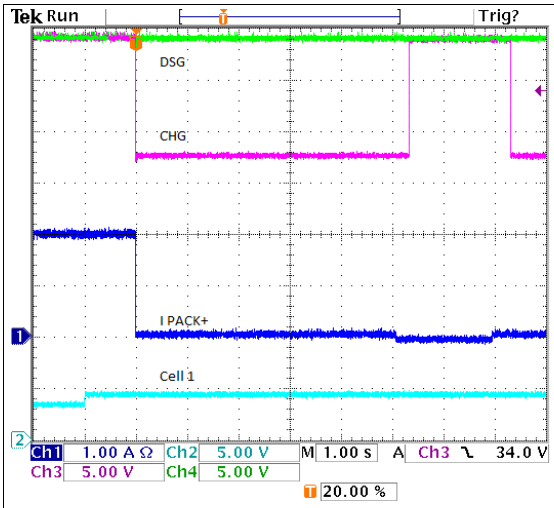

Figure 3. Series FETs, Discharge While OV

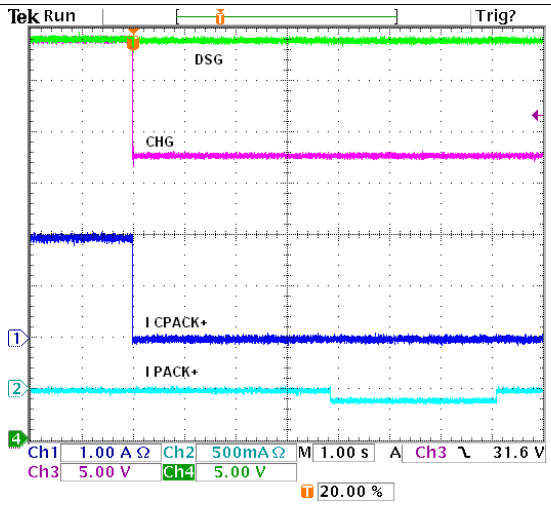

Figure 4. Parallel FETs, Discharge While OV

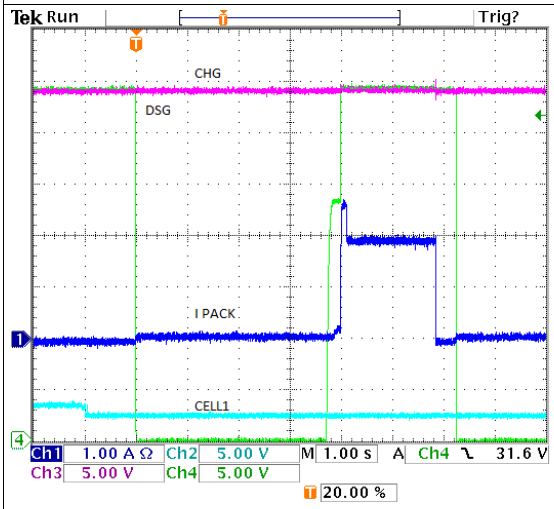

Figure 5. Series FETs, Charge While UV

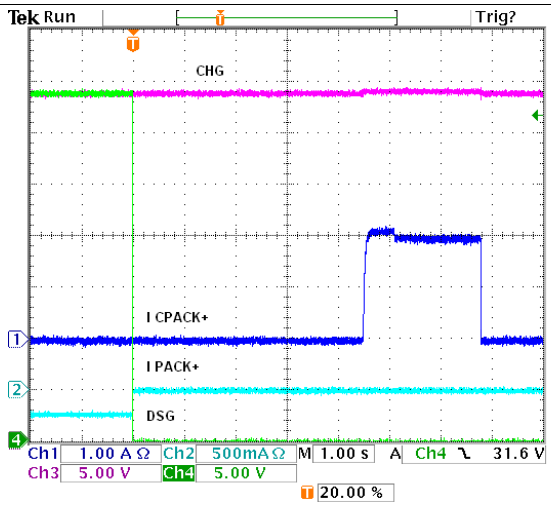

Figure 6. Parallel FETs, Charge While UV

The parallel FET circuit in Figure 2 uses two discharge FETs with the same value of gate resistor as the series schematic. Notice in Figure 7 and Figure 8 that the switching time slows with the capacitance of the second gate of the FET. The gate resistor, R27, can be adjusted for faster switching. The individual gate resistors R23 and R26 avoid oscillation in the parallel FETs. Adjust this value as needed for your FETs. In some cases, ferrite beads are used for impedance at high frequency to avoid oscillation, but provide low DC resistance.

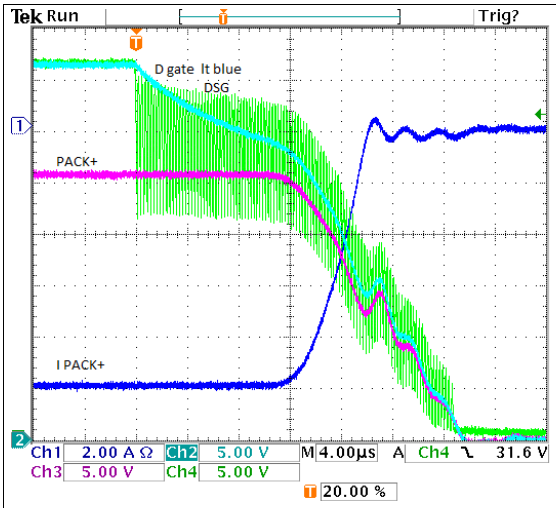

Figure 7. Series FETs, OCD

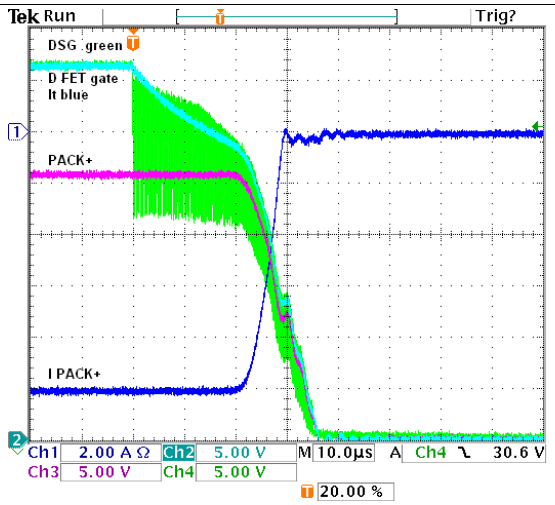

Figure 8. Parallel FETs, OCD

4 Blocking Leakage Currents in Parallel Paths

When considering blocking leakage current in parallel paths, the designer can conclude that a series FET solution provides a more cost effective battery solution due to the complexity of the circuit. However, system architectures vary, but the designer can determine that the configuration options of the BQ76952 and the added complexity of the external circuits are suitable for their application. The part does not have duplicate CHG and DSG pins for the separate paths. This section shows example circuits and limitations that can be encountered using the single high-side controls for the separate current paths. Circuits that can be controlled with the DDSG and DCHG signals are not considered here.

4.1 Blocking Discharge through the Charge Path

The charge FET provides a path for discharge through its body diode when it is off. In some cases, the designer can be concerned about the leakage of the battery into a disabled charger. While leakage into a charger can be small, continued loss can leave the battery permanently disabled since the battery is not able to switch off the load. A Schottky diode D3 as shown in Figure 9 is one solution. The diode avoids leakage current and can immediately respond to loads. The Schottky diode has a lower forward voltage than a standard diode, but does provide loss during charging.

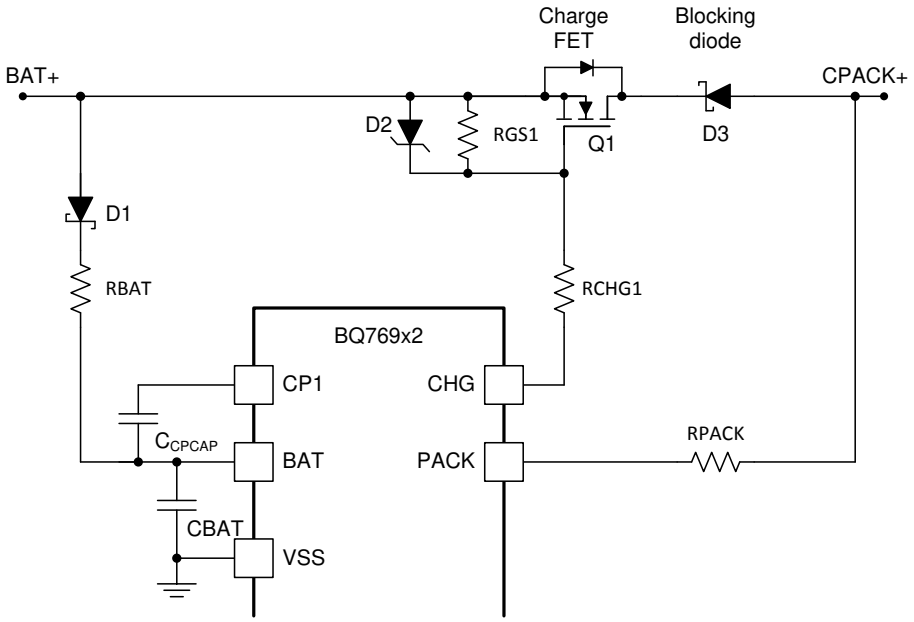

Figure 9. Blocking Discharge in Charge Path with Schottky

A FET might be considered a diode, which can be enhanced. Since the CHG pin of the BQ76952 is driven only to the BAT level when it is low, a common drain connection of the blocking FET allows the charge FET to be controlled by the CHG pin. Figure 10 shows an example schematic. In this circuit, an N-channel blocking FET Q2 is also driven high by the CHG pin. The gate of the blocking FET Q2 must also be allowed to fall with CPACK+ to keep the blocking FET from operating as a source follower. This is accomplished by the P-channel signal FET Q3. The added RGS2 for the blocking FET adds to the load on the charge pump and increases the BQ76952 supply current when CHG is high. This may not be a concern in a system where CHG and DSG are enabled one at a time. When CHG is on Q1 is on, Q3 is also on, so Q2 is on. When CHG is off, CHG pulls down to BAT, and Q1 and Q3 are off. D3 is used to prevent a high voltage on CPACK+ and the voltage divider of RGS2, RCHG2, and RCHG1 from biasing Q1 to act as a source follower and allow charging with CHG off. When the signal FET Q3 turns off, capacitance across D3 can help turn off Q2, but mostly, the RGS2 must accomplish the turn off of the blocking FET Q2. RGS2 must be large to minimize load on the charge pump, so response to a load on the CPACK+ terminal is slow. The circuit requires no additional control lines but has performance limits.

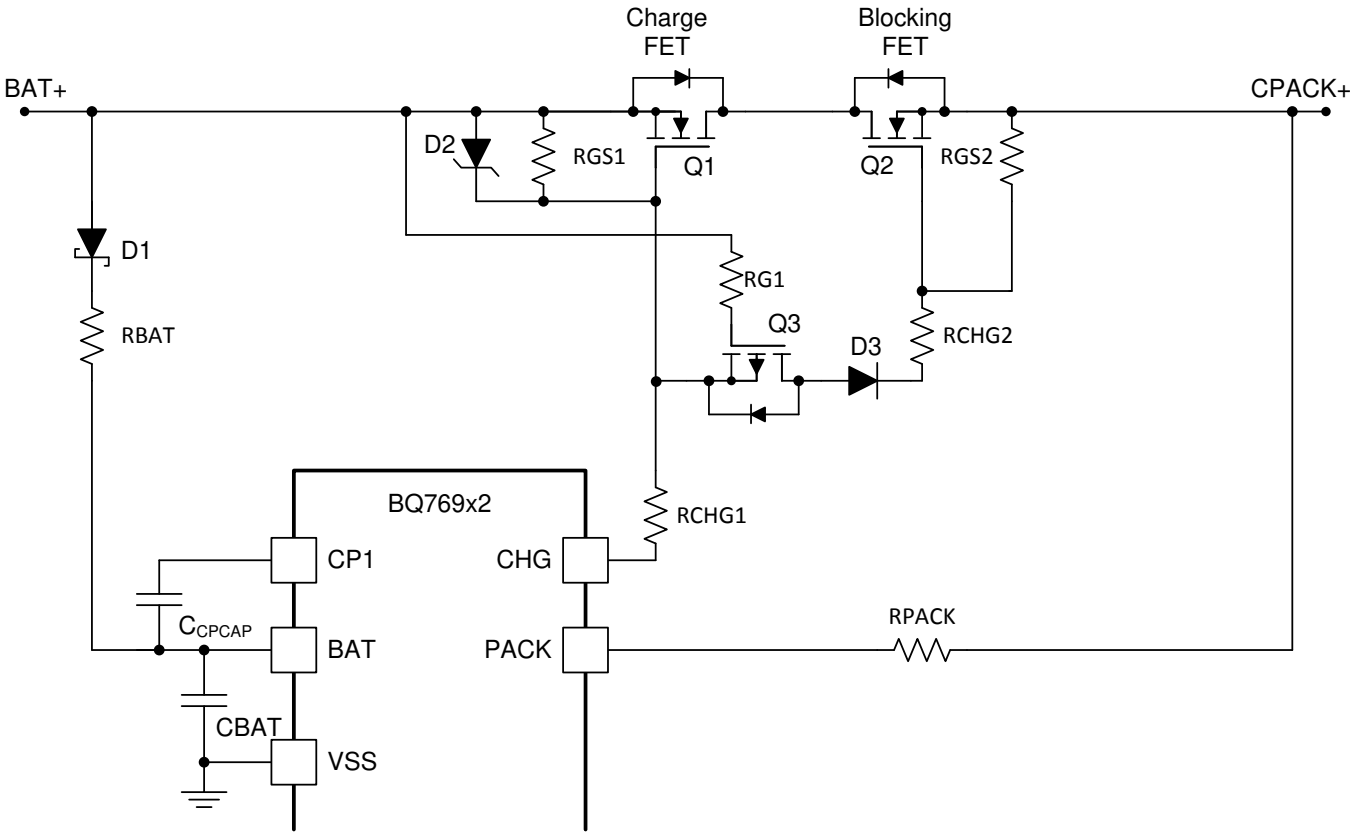

Figure 10. Charge Path Blocking FET

With a charger present, the circuit switches current into the battery pack as CHG is turned off and on, as shown in Figure 11 and Figure 12. When a load is present on CPACK+ and CHG is turned off, the load current continues for a significant time as expected (see Figure 13). The Q2 FET must sustain the power of the discharge while its gate voltage is discharged by RGS2. This can be useful for designs where the concern is low discharge currents. Another limitation of this schematic is turnon of the CHG with a load present on the CPACK+ terminal. With CPACK+ loaded, the CHG pin drives current through the following:

- RCHG1
- Q3
- D3
- RCHG 2
- RGS2

Depending on the load, component values, and system voltage, the charge pump voltage on CP1 can be drawn down and the CHG is unable to turn on the FETs. See Figure 14 for an example. The low charge pump voltage would also affect the DSG if it were turned on in this condition. The BQ76952 does not have an undervoltage lockout on the charge pump voltage. The system control would need to recognize this situation and turn off the CHG output.

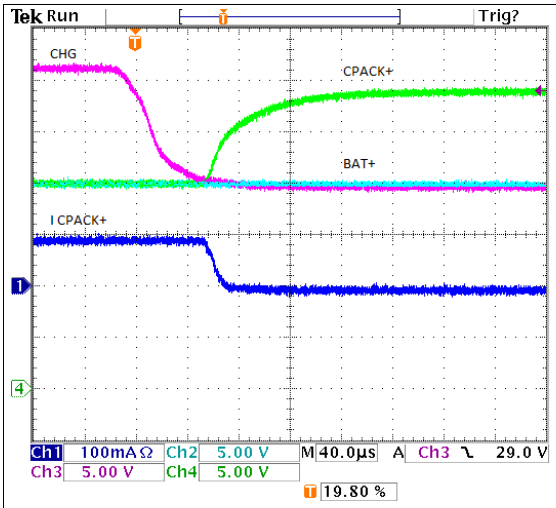

Figure 11. CHG Off with Charge Path Blocking and Charger

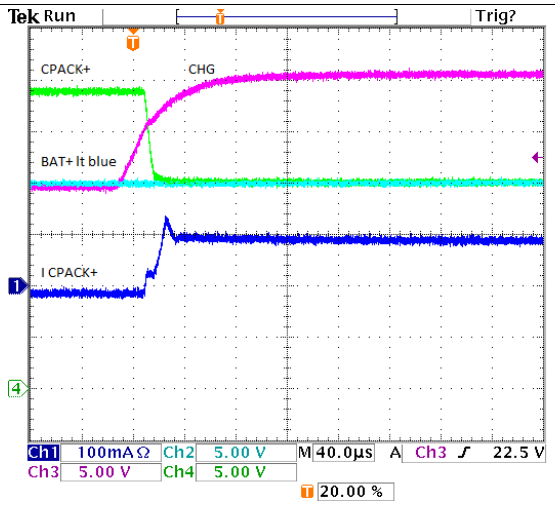

Figure 12. CHG On with Charge Path Blocking and Charger

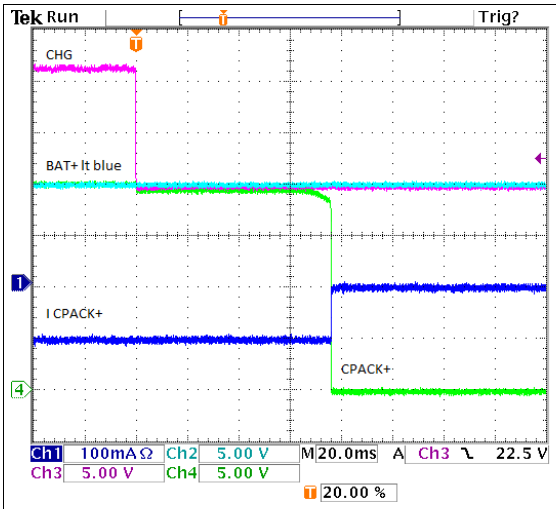

Figure 13. Slow Turn Off of Charge Blocking with Load

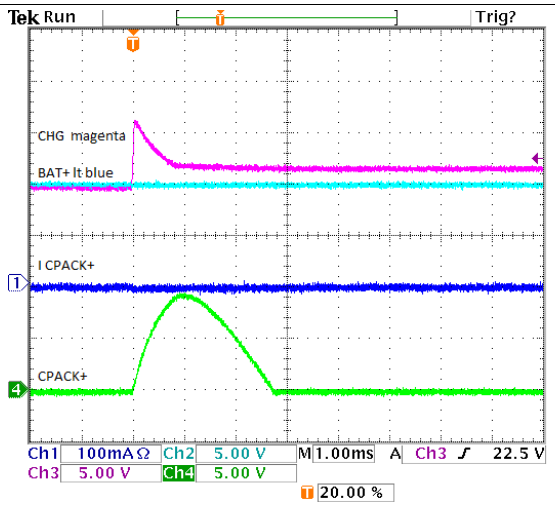

Figure 14. Charge Pump Depletion when CHG is On with Load on CPACK+

When the concern on the charge path is for the short circuit of the charge path rather than slow leakage, the gate can be clamped to the BAT voltage as shown in Figure 15. This circuit holds up the CPACK+ terminal again and allows some leakage through D4, RG2, and RGS3. The designer can control the speed of the circuit and maximum leakage current with component selection. An example of a short circuit of the charger is shown in Figure 16. The BAT signal is from a similar capture saved for comparison. The circuit works by the voltage difference between the BAT pin and CPACK+ during the short circuit event, turning on Q4 to clamp the blocking FET off. It is the components external to the BQ76952 that turn off the path rather than the CHG output, which remain on during and after the event and pulls down the charge pump voltage. The battery system must detect the condition and turn off CHG. If the battery is able to sustain the load current, the circuit does not operate. Again, the battery system must detect the condition and turn off CHG.

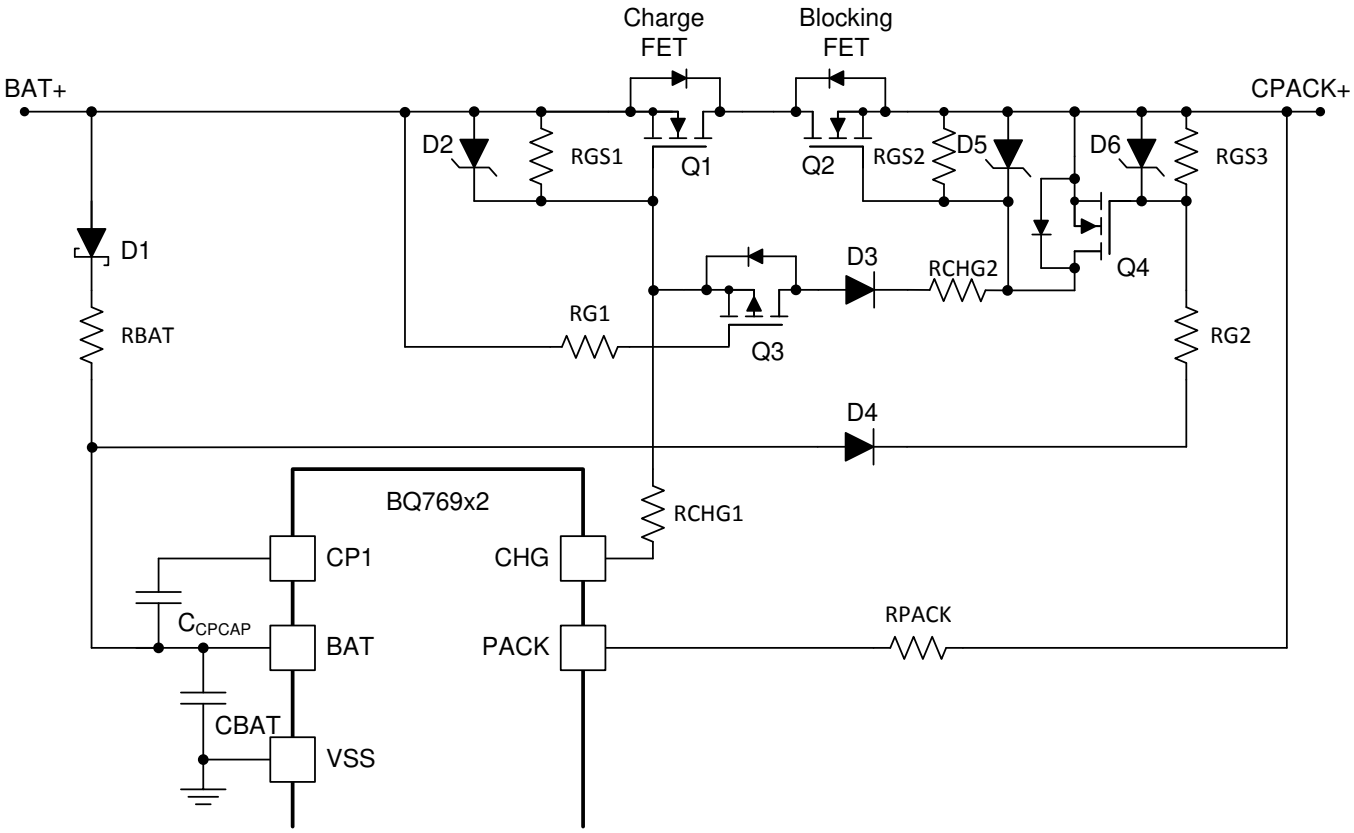

Figure 15. Charge Path with Blocking and Clamp FETs

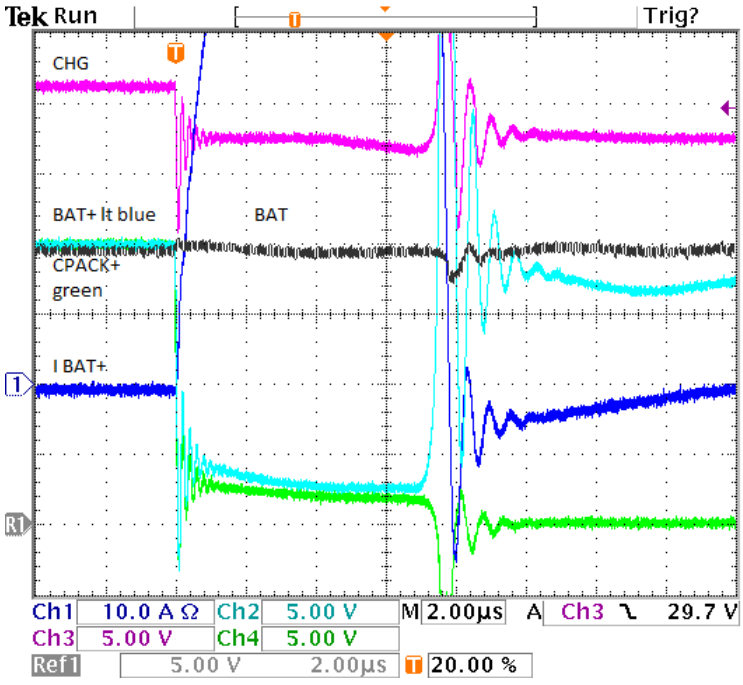

Figure 16. Short Circuit of Charger Terminals with Blocking FET and Clamp

Other circuits are possible, depending on the system and requirements. Using a P-channel clamp circuit on the gate of Q2 to speed its turnoff, or a P-channel FET for Q2 with control from DCHG or other GPO can be options. Development of specific circuits is left to the application designer.

4.2 Blocking Charge through the Discharge Path

The BQ76952 DSG pin can swing to VSS. During turnoff, it is driven to a voltage below LD and after a time out, turns off, leaving the RGS to hold the gate low. A common drain blocking FET circuit would need to leave the gate of the blocking FET at or near the battery+ potential and prevent pullup of the DSG pin. A common source connection allows control of both FETs by the DSG pin and is shown in Figure 17.

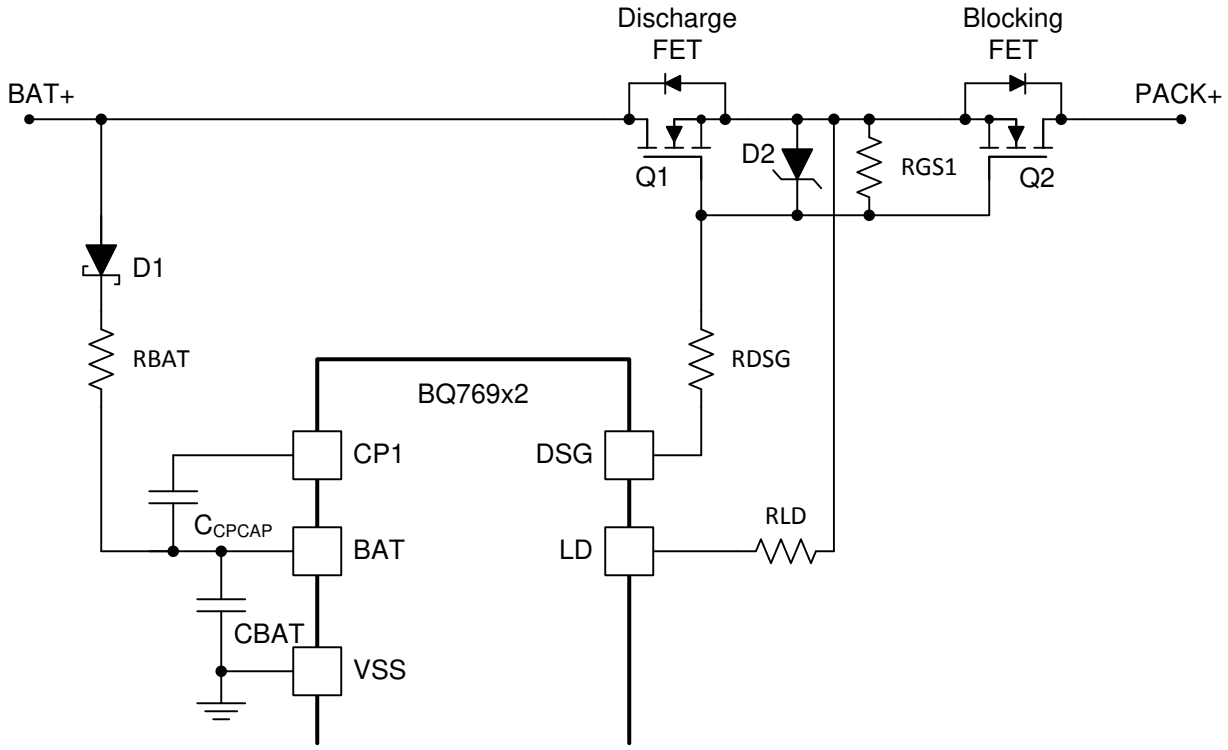

Figure 17. Blocking Charge Current in the Discharge Path

With DSG on, the current can flow in either direction as shown in Figure 18. With DSG off, current is blocked and PACK+ can swing above BAT+ as shown in Figure 19. With a load present, examples of DSG turnon and DSG turnoff are shown in Figure 20 and Figure 21. With a source present on the load path, examples of DSG turnon and DSG turnoff are shown in Figure 22 and Figure 23.

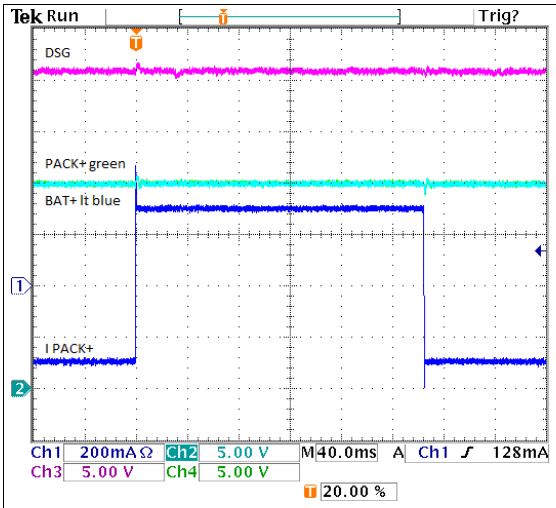

Figure 18. Current Flow with DSG On

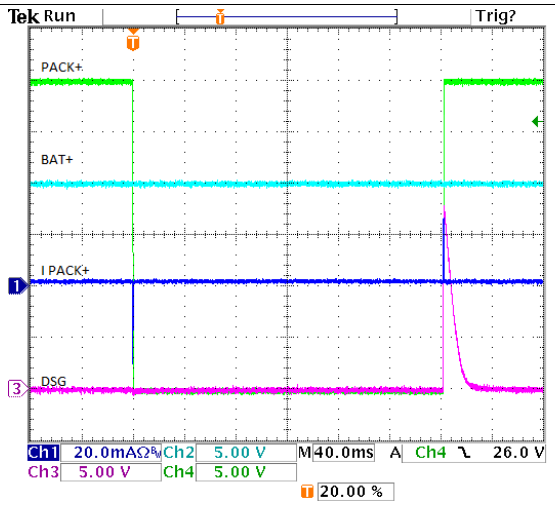

Figure 19. Current Blocking with DSG Off

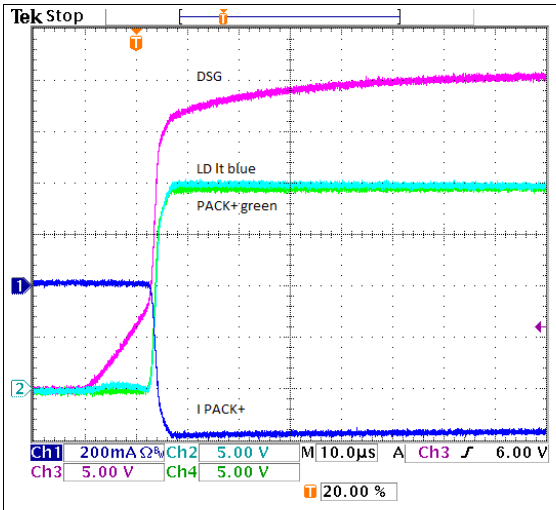

Figure 20. DSG Turnon with Load

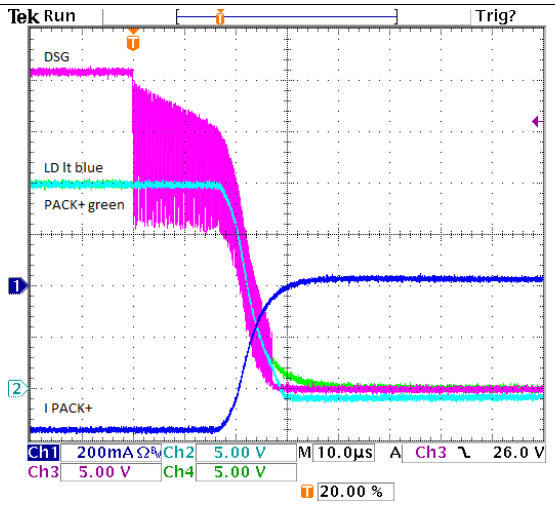

Figure 21. DSG Turnoff with Load

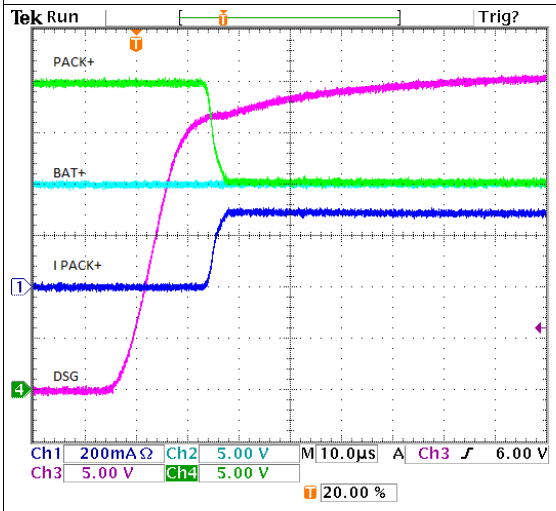

Figure 22. DSG Turnon with Source

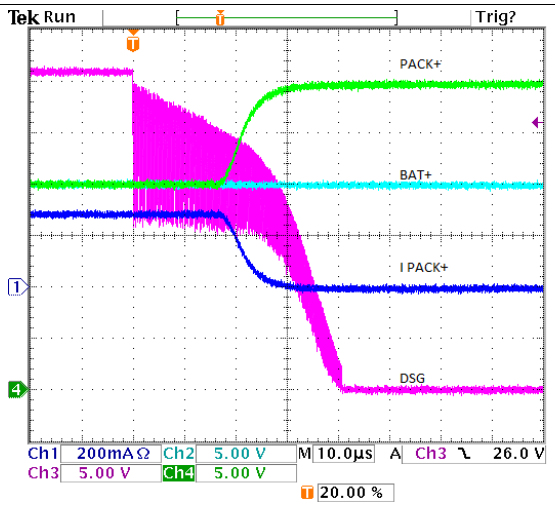

Figure 23. DSG Turnoff with Source

5 Wakeup Circuit Options

Wakeup options for the BQ76952 are pullup of the LD pin or pulldown of the TS2 pin. With a parallel path implementation, LD is connected to the discharge path and pullup is not normally expected. The parallel schematic in Figure 2 does not include a wakeup provision. The EVMs for the family use a switch on TS2 to wake the part. This can be desired for some applications. Other designers can chose to use a signal from the charger or system to wake the BQ76952.

With a Schottky diode blocking discharge into CPACK+, a simple wakeup circuit is shown in Figure 24. Since the Schottky allows CPACK+ to drop to 0 V, the circuit can wake from application of a charger voltage as shown in Figure 25, and the input can share any ESD protection on the CPACK+ terminal. When the CPACK+ is not blocked or has a residual DC voltage with a circuit such as Figure 15, a separate terminal is needed. A separate terminal can be used by both charger and system.

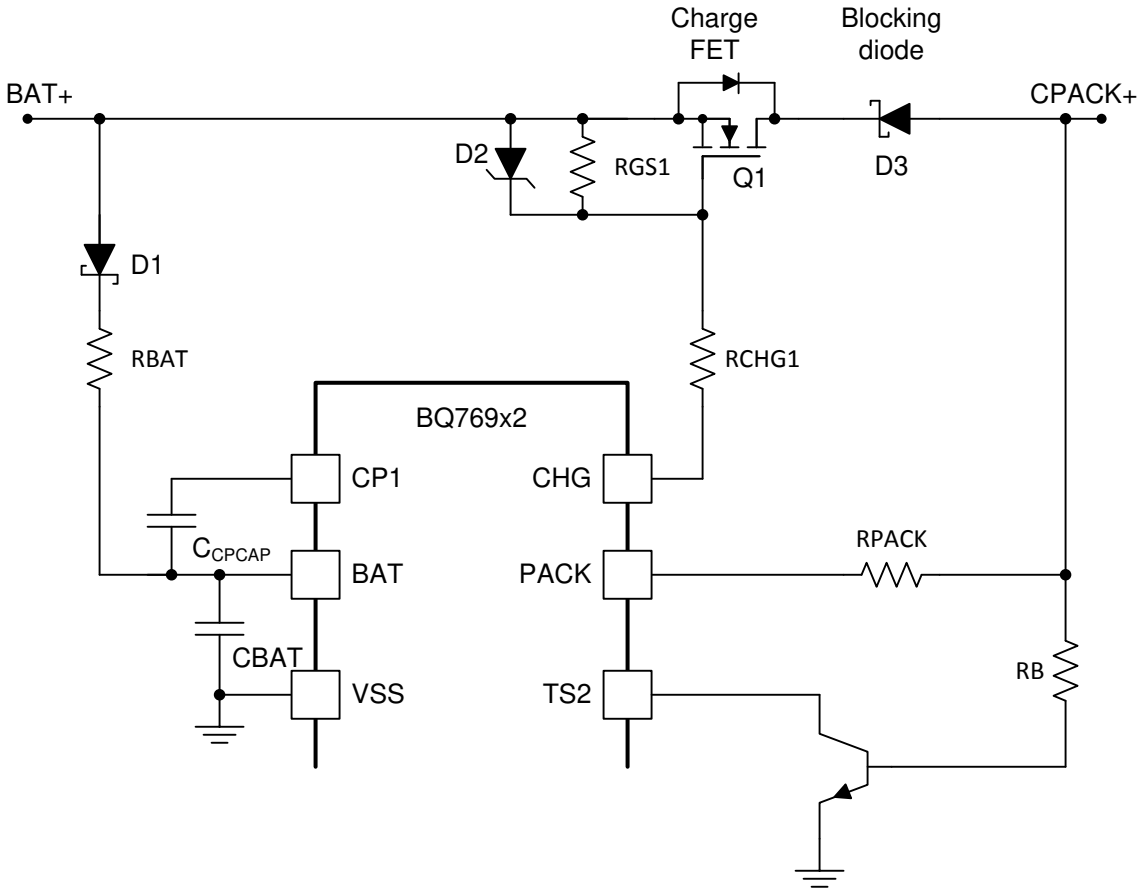

Figure 24. Wakeup Circuit with Blocking Schottky

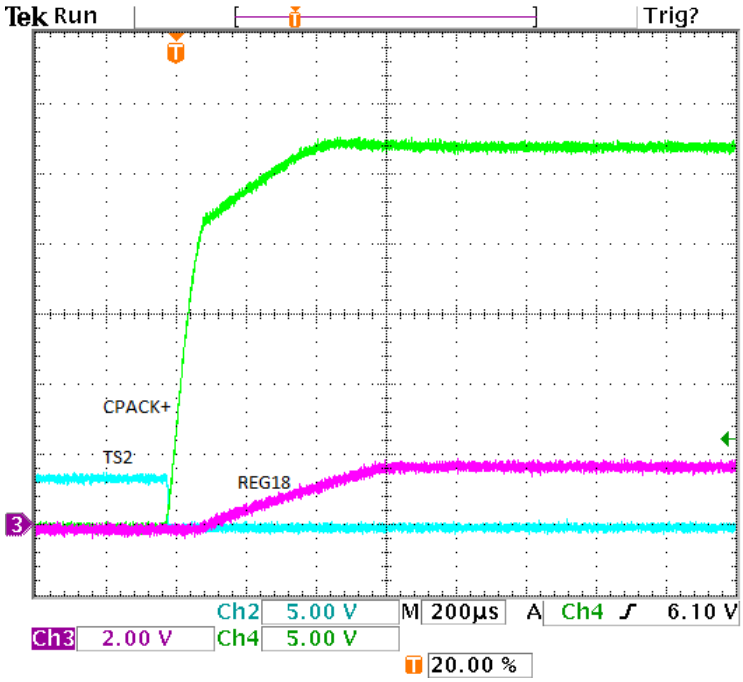

Figure 25. Wakeup from Charger Voltage

The wakeup feature on the LD pin is not disabled by the parallel design or the ***SFET*** bit setting. The designer must be aware of two common observations. The BQ76952 can wake up from connection of the battery since the common ESD capacitors across both the FET and pack terminals (C18–C21 in Figure 2) create a divider which initially provides half the battery voltage to PACK+ and a pulse to the LD terminal as shown in Figure 26. If the load can generate voltage on PACK+, it pulls up the LD pin and wakes the circuit without a charge blocking FET. Even with the charge blocking FET such as Q2 of Figure 17, with a sufficient rise time, a transient on PACK+ can couple through the blocking FET capacitance and overcome the pulldown on LD to wake the BQ76952 as shown in Figure 27.

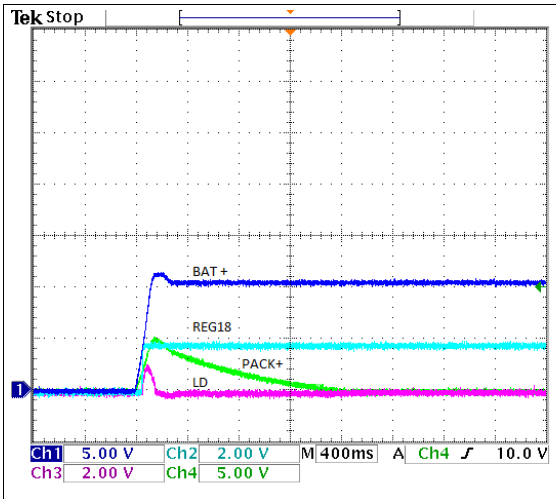

Figure 26. Wakeup from Battery Connection

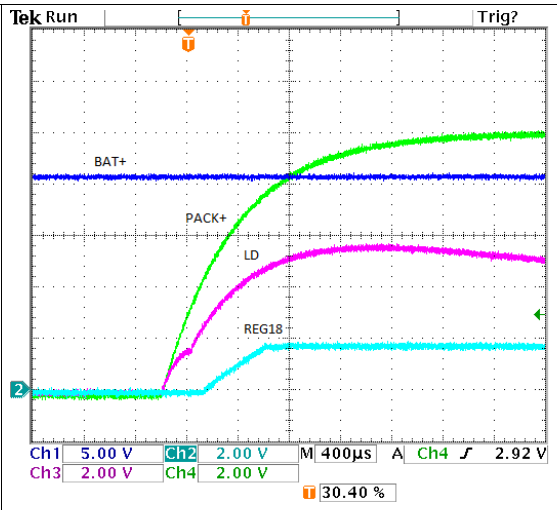

Figure 27. Wakeup from PACK+ Transient with Blocking FET

6 Conclusion

The BQ76952 family devices allow series or parallel FET configurations through the pin connections and the ***SFET*** configuration bit to control body diode protection operation. Accessory circuits in a parallel path configuration can have design tradeoffs and must be designed to meet the system requirements. The circuits and test results presented in this document will help the designer recognize conditions for consideration in their design. Refer to the data sheets for device and configuration information.

7 References

- Texas Instruments, *BQ76942 3S-10S Battery Monitor and Protector Data Sheet*
- Texas Instruments, *BQ76952 3S-16S Battery Monitor and Protector Data Sheet*
- Texas Instruments, *BQ76942EVM User's Guide*
- Texas Instruments, *BQ76952EVM User's Guide*

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