Application Report
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Methods to Eliminate Damage Caused by Reverse Current in Synchronous Buck Converters

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ABSTRACT

Reverse current is a common phenomenon that occurs in synchronous buck converters. If the reverse current is large enough, the low-side field-effect transistor (FET) is very likely to be damaged. Since this issue is relatively common in synchronous buck converters, it is worth investigating the mechanisms that lead to reverse current and the subsequent damage that it causes. At the same time, it is important to understand potential solutions to eliminate this condition altogether. In this application note, four such solutions are presented and evaluated.

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Trademarks

1 Introduction

In synchronous buck converters, a large reverse current is an imposing threat. If the reverse current is too large, damage to the integrated low-side MOSFET is likely to occur, especially when the buck converter meets the following conditions:

- The output voltage is high.
- The output capacitance is large.
- The input falling slew rate of the input source is fast.

The following sections detail the failure mechanism and damage associated with reverse current, along with proposed solutions to help avoid it.

2 Reverse Current Forming Mechanism

In synchronous buck converters, reverse current can be observed under the following two common conditions: (1) the falling slew rate of the input source is fast, and (2) the input rail of the buck converter is short.

This research uses one specific synchronous buck converter as the subject of the experiment. Through proper configuration of the inductance and capacitance of this synchronous buck converter, the input voltage is set to 19 V and the output voltage to 12 V. With a falling slew rate around 10 V/µs at the input source, as Figure 1 and Figure 2 show, a big spike can be clearly observed when the next cycle starts up.

Currently, the current that flows into the low-side MOSFET includes two parts: the reverse current that flows through the inductor and the reverse current in the body diode of the high-side MOSFET. Therefore, the current value that flows into the low-side MOSFET is quite large, around three or four times the amount of current that flows through the inductor. By observing the function of the low-side MOSFET, you can determine that the low-side MOSFET is damaged.

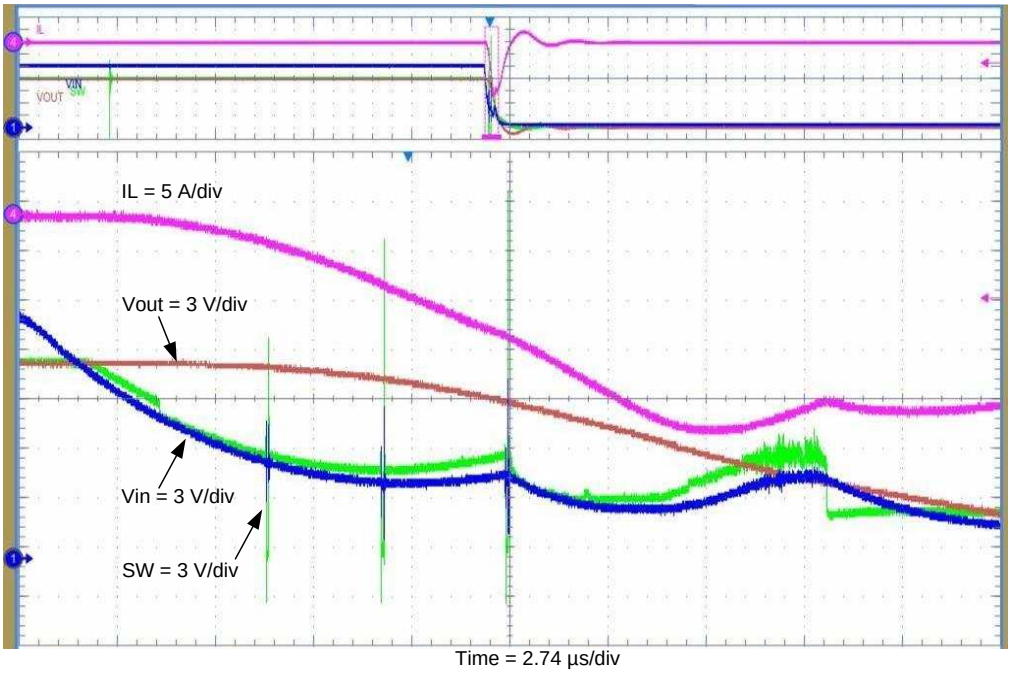

Figure 1. Waveforms at V_{IN} = 19 V, V_{OUT}= 12 V, and Vin SR = 10 V/µs

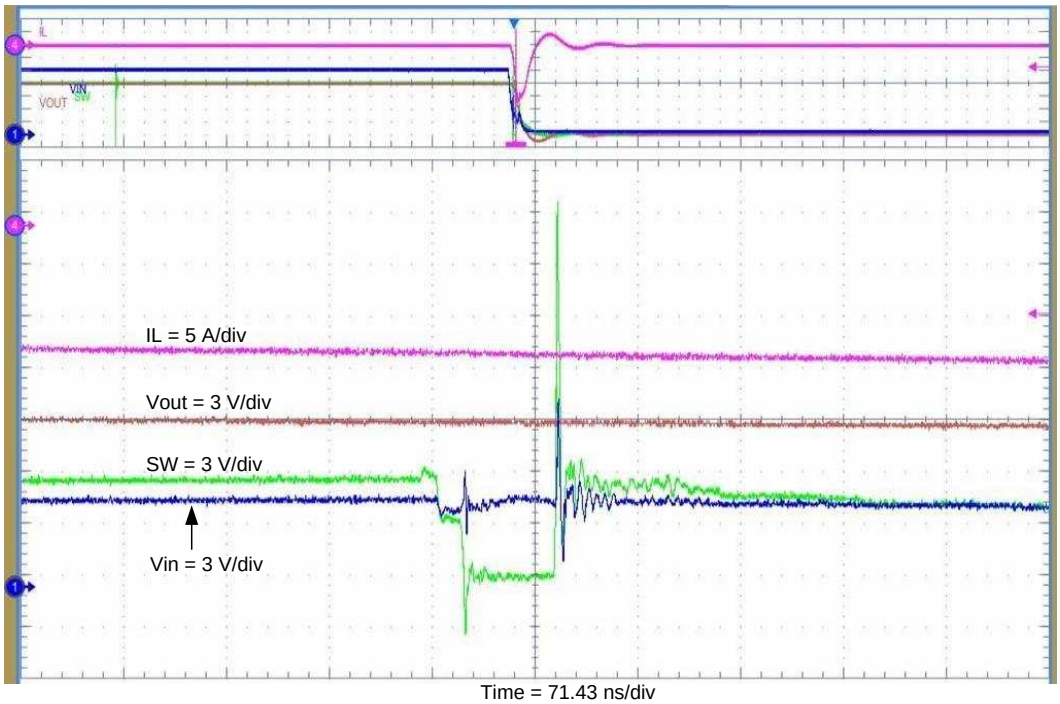

Figure 2. Waveforms at V_{IN} = 19 V, V_{OUT} = 12 V, and Vin SR = 10 V/µs (Zoom-In)

As for the mechanism that leads to reverse current, a schematic diagram is shown in Figure 3.

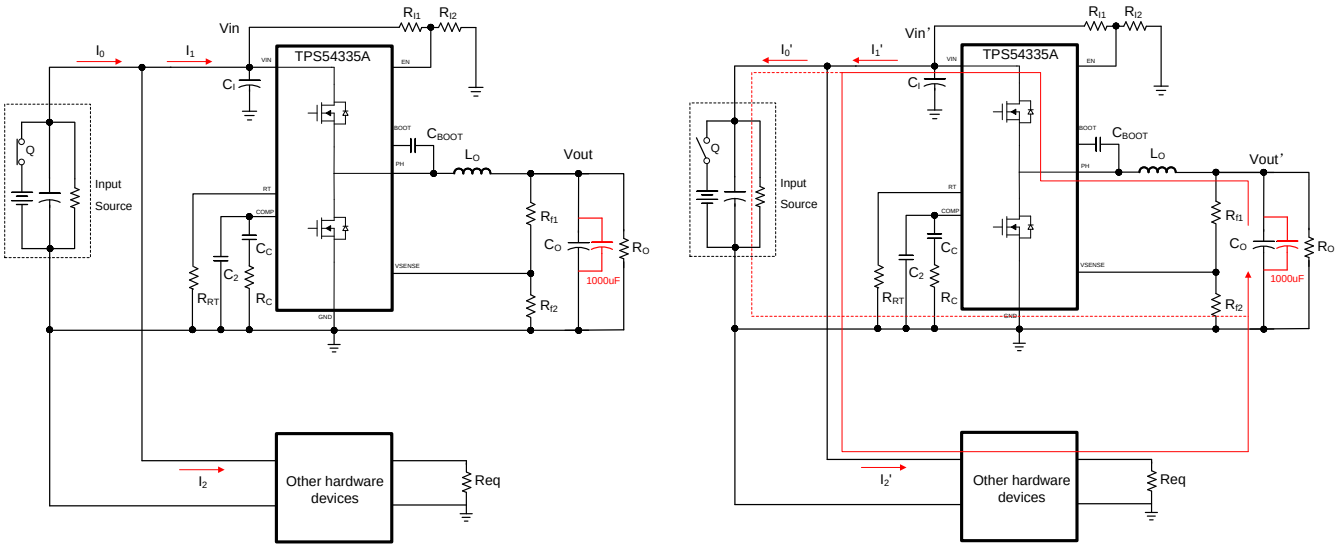

Figure 3. The Forming Mechanism of the Reverse Current

1. At power-on, the synchronous buck converter is supplied by the input source, and the output voltage of the synchronous buck converter comes to the target voltage quickly.
2. When power is off, the input voltage drops quickly since the other hardware devices are still consuming power and some equivalent loading exists in the input source.
3. Assuming a very small voltage drop on V_{OUT} due to large output capacitance with a light load, and a Vin' that is lower than V_{OUT}', a reverse current can form. It can be observed that the higher power consumption of other hardware devices, the higher the reverse current. The faster the falling slew rate of the input source, the higher the reverse current.

3 Low-side MOSFET Failure Mechanism

Section 2 showed you how a reverse current can form. Once that reverse current is formed, the input voltage is already lower than the output voltage. The buck converter is now working in LDO mode as the output voltage is higher than the input voltage. If the buck converter runs for a long time in LDO mode, the boot cap voltage would have a chance to reach 2.1 V. In this case, the low-side MOSFET would be forced to turn on to charge the boot cap. By the time the charging is finished, the low-side MOSFET would turn off with reverse current, resulting in a big spike on the SW pin due to the high slew rate of the low-side MOSFET and the existing parasitic inductance of the bonding wire.

By analyzing the moment of damage on Figure 2, it can be seen that there is already one high spike on the SW pin at the first and the second pulse. The reason why the low-side MOSFET is damaged at the third pulse is that the input voltage is constantly falling, making the reverse current larger and larger until the spike on the SW pin damages the low-side MOSFET.

You can conclude that the larger the reverse current, the higher the spike on the SW pin, and the more likely the low-side MOSFET is damaged. Put in another way, the higher the output voltage, the higher the spike on the SW pin and the more likely the low-side MOSFET is damaged.

4 Solutions

Based on the above analysis of the formation of reverse current and damage to the low-side MOSFET, four solutions are proposed below:

Solution (1): Slow down the falling slew rate of the input source.

Solution (2): Power off EN earlier than VIN.

Solution (3): Configure the input UVLO via EN resistor divider so that it exceeds V_{OUT}.

Solution (4): Increase the inductance to decrease the inductor current.

Using the same synchronous buck converter as an example, the following section will mainly discuss the principles of the proposed methods. Through some experiments, you will see how well these approaches solve the reverse current-caused damage issue.

4.1 Solution 1

The most direct way to solve this damage issue is by slowing down the ramp speed of the input source. Applied with the proposed solution, experiment results are shown in Figure 4 and Figure 5. As Figure 4 and Figure 5 show, after slowing down the falling slew rate of the input source, reverse current can still be observed but the peak forward inductor current is decreased a lot, resulting in only a very small spike on the SW pin. The low-side MOSFET is well-protected.

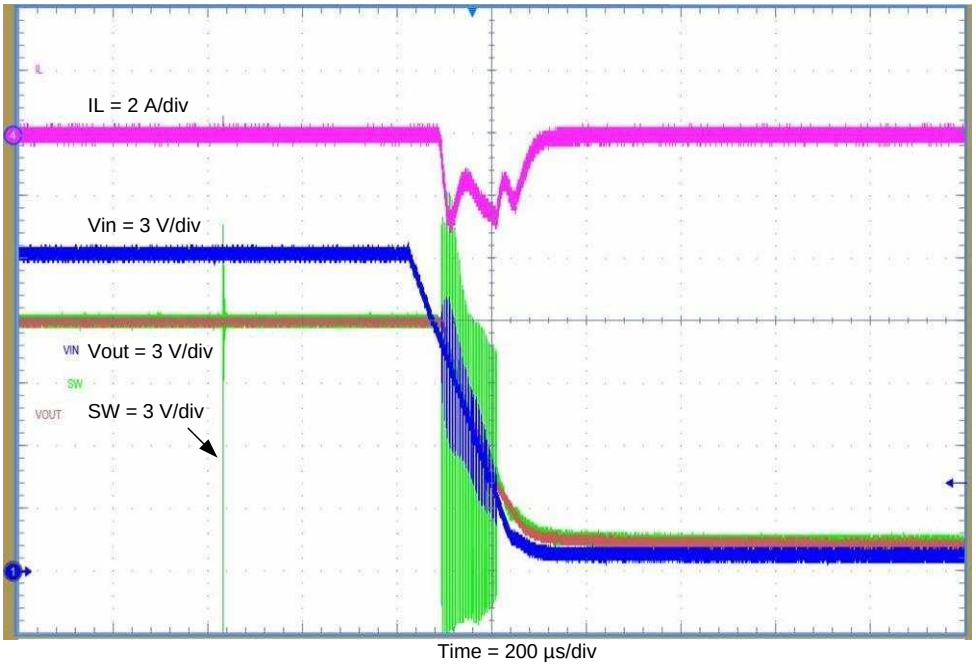

Figure 4. Waveforms at V_{IN} = 19 V, V_{OUT} = 12 V, and Vin SR = 1 V/µs

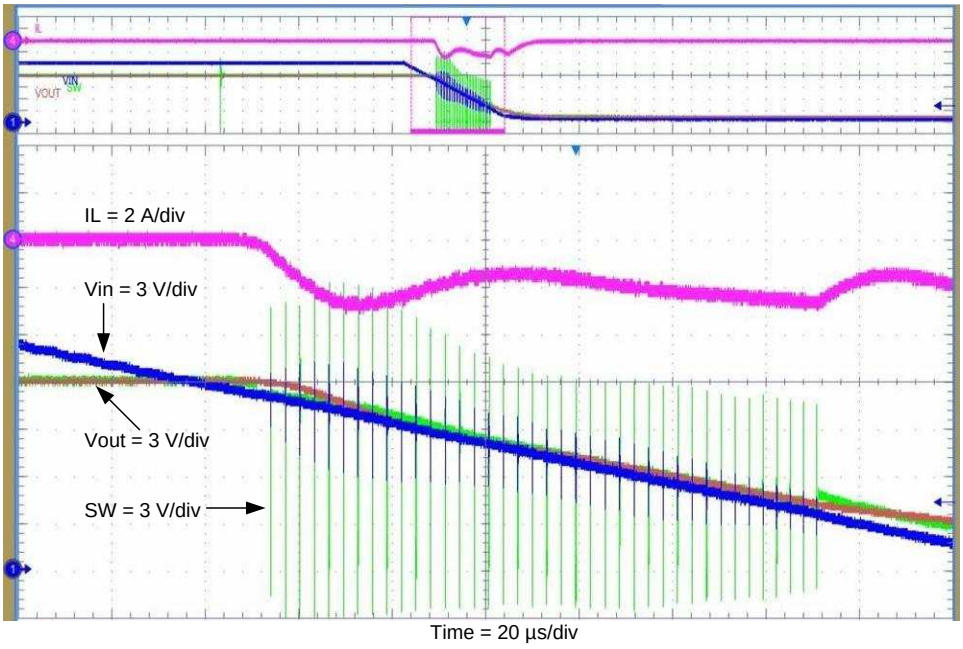

Figure 5. Waveforms at V_{IN} = 19 V, V_{OUT}= 12 V, and Vin SR = 1 V/µs (Zoom-In)

4.2 Solution 2

This solution includes powering off EN earlier than Vin. In this case, the input voltage is already lower than the output voltage. Since EN is powered off earlier, the low-side MOSFET is not damaged because it is already turned off.

4.3 Solution 3

TI recommends solution 3 to the customer. It exceeds VOUT through the configuration of input UVLO via the EN resistor divider. Figure 6 shows the schematic diagram.

As Figure 6 shows, by configuring the EN startup voltage with a resistor divider from the input source, the UVLO of the input source is higher than the output voltage.

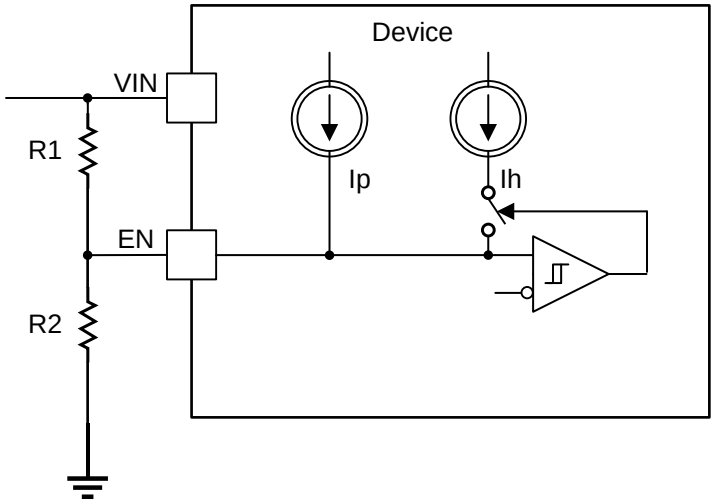

Figure 6. Configure EN Startup Voltage by Resister

4.4 Solution 4

Aside from the previous three solutions, increasing the value of the inductor to decrease the inductor current value can also solve this reversed current-caused damage issue.

As Figure 7 shows, after increasing the standard inductance value, the spike on the SW pin is quite small. The low-side MOSFET can be protected even though the falling slew rate of the input source is fast.

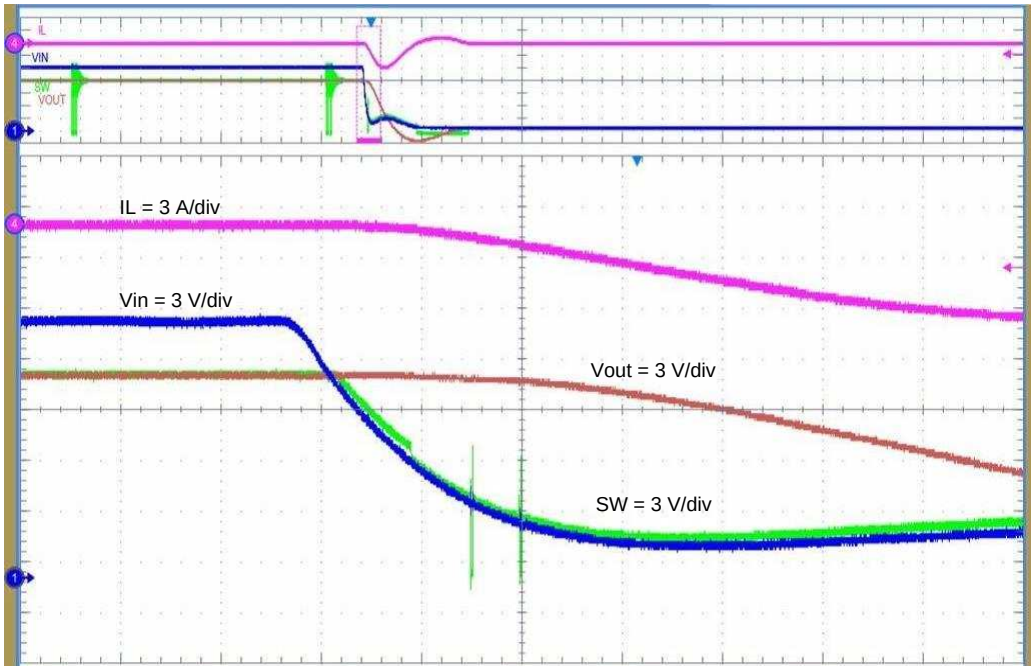

Figure 7. Waveforms at V_{IN} = 19 V, V_{OUT} = 12 V, and Vin SR = 10 V/µs

5 Conclusion

Reverse current-caused damage happens primarily in synchronous buck converters. This application note discusses how reverse current is formed and how it can lead to damage to the low-side MOSFET. After a full theoretical analysis and experimental research, four solutions have been proposed. The results of these experiments prove the validity of these solutions.

The study shows that a larger reverse current produces a higher spike on the SW pin and that this large spike directly damages the low-side MOSFET. Based on the above research, four solutions are proposed and verified to eliminate reverse current-caused damage in synchronous buck converters.

6 References

- Texas Instruments, *TPS54335-2A 4.5-V to 28-V Input, 3-A Output, Synchronous Step-Down DC-DC Converter Data Sheet* (SLUSCK3)

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