Application Report
SLUAA55–May 2020

Programming the TPS53819A 3-V to 28-V Input, 40-A, Eco-mode™, D-CAP2™ Synchronous Buck Controller With PMBus®

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ABSTRACT

The TPS53819A controller allows the user to adjust some configuration options and settings through a 2-wire digital interface port in accordance with the System Management Interface Forum (SMIF) specified PMBus® interface. For more information about SMIF, SMBus™ and PMBus, see:

- SMBus Website – http://www.smbus.org/
- PMBus Website – http://www.pmbus.org/

Specification Compatibility

The TPS53819A is compatible with SMBus revision 2.0 and PMBus Part I, revision 1.1 and PMBus Part II, revision 1.1.

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Trademarks

1 VDD Voltage Supply Compatibility

The VDD of the TPS53819A device must be powered to 4.5 V to 28 V with a minimum supply current of 10 mA for the TPS53819A to be programmed.

2 Digital Signal Supply Compatibility

The TPS53819A uses open-drain drivers and input buffers for ALERT, SCL and SDA pins that are compatible with passive termination to a 2.9-V – 5.5-V rail with external pullup resistors sourcing not more than 4 mA of current.

3 Onboard Termination

SCL and SDA pjns use open-drain output drivers and require external termination. If the programmer does not provide for passive termination, onboard termination may be required. Passive termination should be configured for no more than 4-mA pullup current when SCL or SDA are pulled down to 0 V. For termination to a nominal 3.3-V rail, termination resistance of greater than 900 Ω should be used. For termination to a nominal 5-V rail, termination resistance of greater than 1.4 kΩ should be used. If programmed with push-pull drivers, the driver must have a pullup current limit of no more than 4 mA to prevent damage to the SDA pin driver during bus contention.

4 Clock Speed

The TPS53819A device supports SMBus Clock Speeds from 10 kHz to 400 kHz in accordance with the timing specifications for the high-power SMBus revision 2.0 specification.

5 Clock Stretching

The TPS53819A does not pull the SCL pin low to stretch the clock or slow-down the bus.

6 Programming Configuration and Recommended Schematic

Figure 1 shows the recommended programming schematic for the TPS53819A. To allow programming, the following conditions in Table 1 should be met.

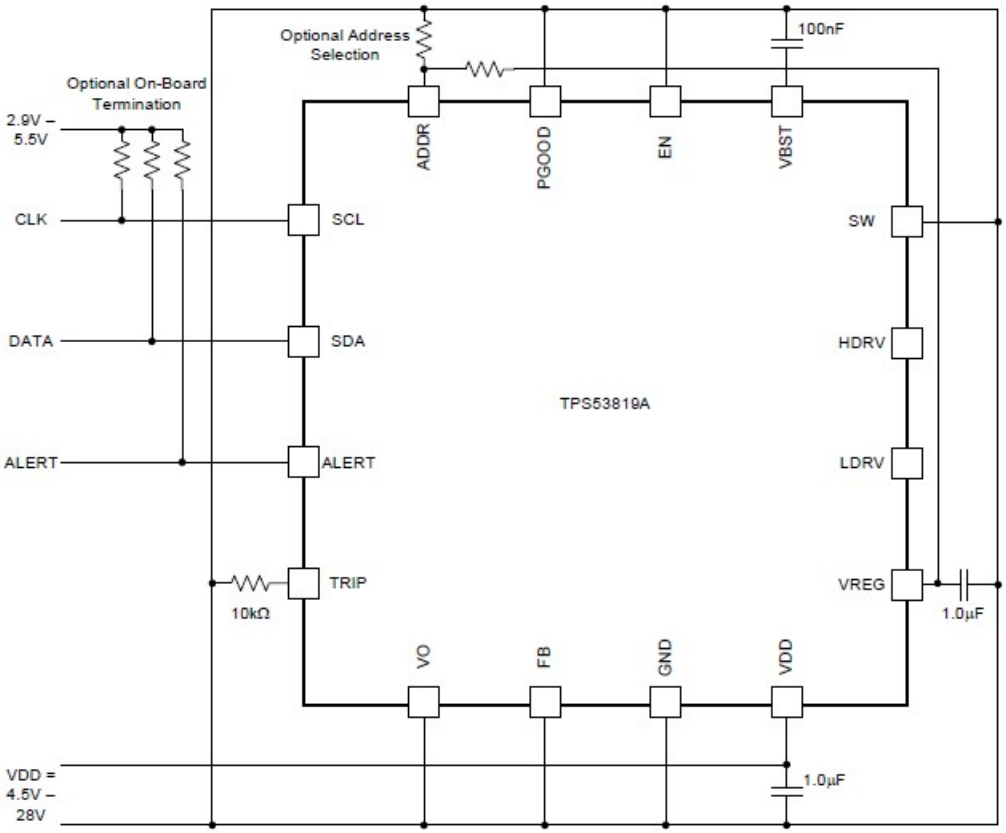

Figure 1. TPS53819A Programming Board Recommended Schematic

Table 1. TPS53819A Programming Recommended Pin Connections

Pin Name	Pin #	Function	Connection
SCL	1	Clock Input for Digital Communication	Input with external passive termination to 2.9-V – 5.5-V supply
SDA	2	Data Input for Digital Communication	Input with external passive termination to 2.9-V – 5.5-V supply
ALERT	3	Active Low Out-of-Band Alert. Pulled low to indicate programming Alert (Optional)	Output with external passive termination to 2.9-V – 5.5-V supply
TRIP	4	10-µA current source for programming current limit	Connect to GND with a 10-kΩ resistor
VO	5	Output Voltage Sense	Short to GND
FB	6	Feedback Regulation	Short to GND
GND	7	Ground	External Ground
VDD	8	Supply	External 4.5-V – 28-V supply. Bypass to GND with a 1.0-µF X5R or better ceramic capacitor with a minimum voltage rating equal to 1.5 × the voltage applied
VREG	9	Regulator Bypass	Bypass to GND with 1.0-µF X5R or better ceramic capacitor with a minimum 10-V rating
DRVL	10	Low-side FET Driver	Leave Floating
DRVH	11	High-side FET Driver	Leave Floating

Table 1. TPS53819A Programming Recommended Pin Connections (continued)

Pin Name	Pin #	Function	Connection
SW	12	Switch Node Sense Pin	Short to GND
VBST	13	High-side Driver Boot-strap	Bypass to SW with 100 nF X5R or better ceramic capacitor with a minimum voltage rating of 10 V
EN	14	Enable pin to Enable Output Conversion	Short to GND
PGOOD	15	Open Drain Power Good Indicator Pin	Short to GND
ADDR	16	Address Programming Pin	Short to GND or connector midpoint of VREG to GND resistor divider

7 Memory Structure

The TPS53819A provides both volatile and non-volatile memory (NVM). Writing to the PMBus command codes set values in volatile memory. Read from PMBus command code return values in volatile memory. The PMBus Command STORE_DEFAULT_ALL (Send Byte to Command Code 11h) copies the current values in volatile memory to their respective bits in non-volatile memory. The PMBus Command RESTORE_DEFAULT_ALL (Send Byte to Command Code 12h) copies current values in volatile memory to their respective bits in non-volatile memory. Not every bit of volatile memory has a corresponding bit of NVM. Volatile memory bits without corresponding bits of NVM will return to their default value if VDD is lowered below its UVLO level and then raised above its UVLO level.

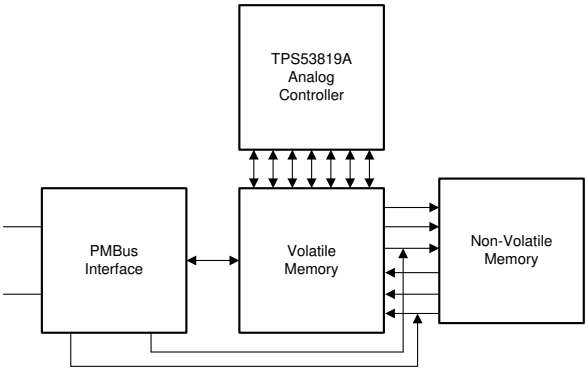

Figure 2. TPS53819A Conceptual Memory Architecture

8 Direct NVM Programming

The TPS53819A does not support Direct or Block NVM programming. To program the NVM memory, the corresponding bits of volatile memory must be set through the PMBus interface followed by the STORE_USER_ALL command.

9 NVM Write Time

The TPS53819A may require up to 20 ms to complete a write of the NVM. VDD power must be maintained during the entire NVM write time or the NVM memory store may become invalid. During the NVM write time, the TPS53819A may not respond to its address. A minimum 25-ms wait is recommended after sending the STORE_USER_ALL command.

10 Supported PMBus® Commands

The TPS53819A supports 14 PMBus commands. 8 Commands contain at least 1 bit with NVM support. The commands are covered in Table 2.

Table 2. TPS53819A PMBus® Command Support

Command	Code	Format	NVM
OPERATION	0x01	R/W Byte	None
ON_OFF_CONFIG	0x02	R/W Byte	[3:2] only
CLEAR_FAULTS	0x03	Send Byte	N/A
WRITE_PROTECT	0x10	R/W Byte	None
STORE_DEFAULT_ALL	0x11	Send Byte	N/A
RESTORE_DEFAULT_ALL	0x12	Send Byte	N/A
STATUS_WORD	0x79	R/W Word	None
CUSTOM_REG	0xD0	R/W Byte	[5:0] Only
DELAY_CONTROL	0xD1	R/W Byte	[5:0] Only
MODE_SOFT_START_CONFIG	0xD2	R/W Byte	[3:0] Only
FREQUENCY_CONFIG	0xD3	R/W Byte	[2:0] Only
VOUT_ADJUSTMENT	0xD4	R/W Byte	[4:0] Only
VOUT_MARGIN	0xD5	R/W Byte	[7:0]
UVLO_THRESHOLD	0xD6	R/W Byte	[2:0] Only

11 Command Ordering

The TPS53819A has no restrictions on command ordering.

12 Readback Verification

To ensure valid programming of NVM, TI recommends using the following procedure:

1. Raise VDD voltage to 4.5 V to 28 V
2. Raise SCL and SDA termination voltage to 2.9 V to 5.5 V
3. Write values to desired PMBus Commands
4. Store PMBus Command values to NVM using STORE_DEFAULT_ALL (Code 11h)
5. Wait a minimum of 25 ms
6. Read Word STATUS_WORD (code 79h)
   - If STATUS_WORD reports a CML fault (Low Byte Bit 1 = 1) recommend repeating steps 3, 4, and 5.
7. Decrease VDD voltage below 2.0 V
8. Wait a minimum 10 ms
9. Raise VDD voltage to 4.5 V to 28 V
10. Read PMBus Command Values to confirm programming
    - Since some PMBus Command values to not have NVM support for all bits, it may be necessary to mask read-back values by bit-wise AND with 0b for bits without NVM support to avoid readback verification errors.

13 Resources

- Texas Instruments, *TPS53819A Product Folder*

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