Application Note

UCC28951-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for UCC28951-Q1 (TSSOP (24) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

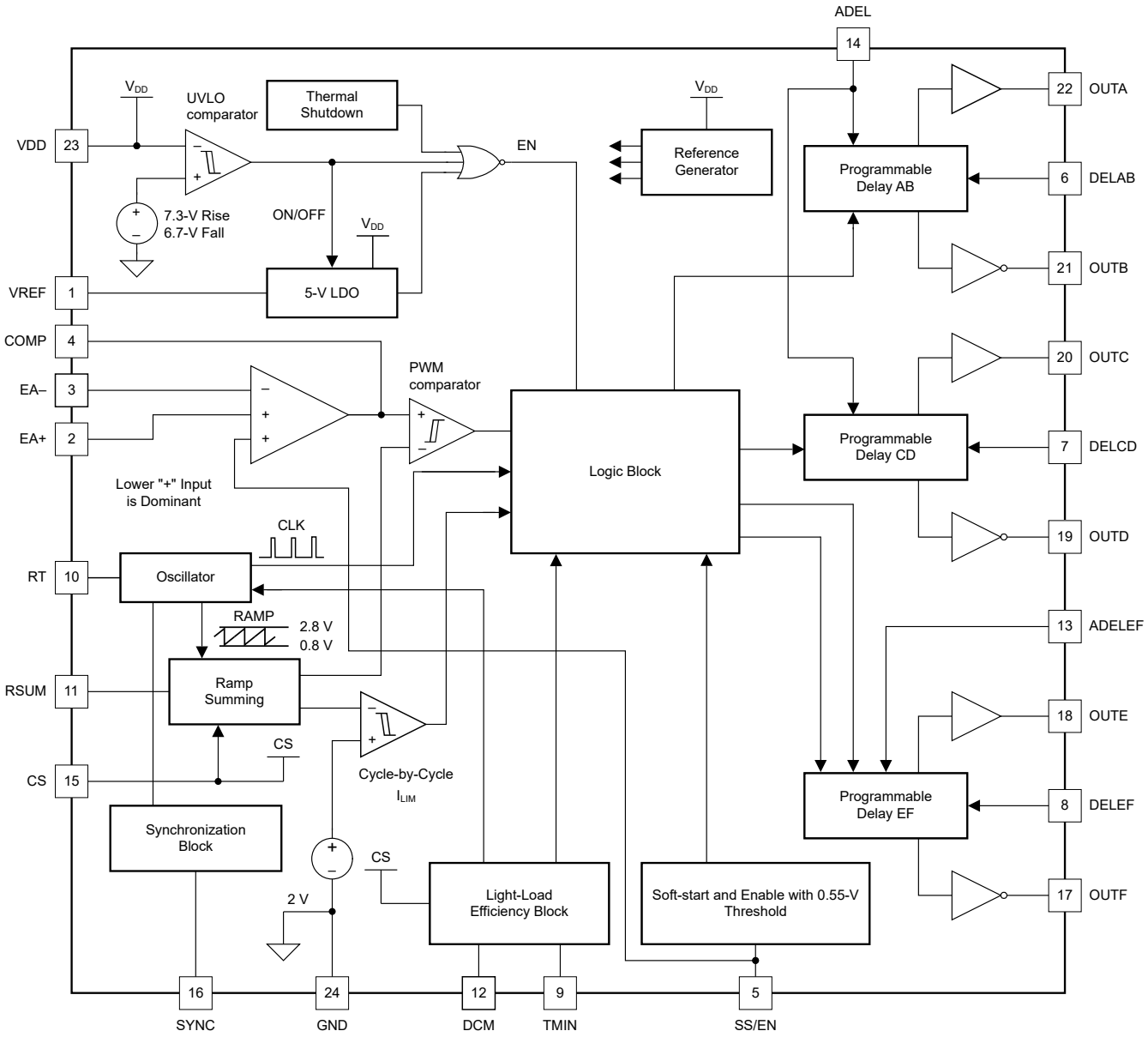

Figure 1-1. Functional Block Diagram

UCC28951-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for UCC28951-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (100 mW, 200 mW, 300 mW)	17, 19, 22
Die FIT Rate (100 mW, 200 mW, 300 mW)	3, 4, 6
Package FIT Rate (100 mW, 200 mW, 300 mW)	14, 15, 16

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW, 200 mW, 300 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC28951-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
One or more primary side drivers stuck high or low	31
Primary Drivers at wrong duty cycle	17.5
Wrong SR duty cycle	18.5
SYNC capability lost	2
Adaptive delay is wrong	13
Burst mode lost or wrong burst mode threshold	8.5
Frequency setting is wrong	6
No effect	3.5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC28951-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the UCC28951-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC28951-Q1 data sheet.

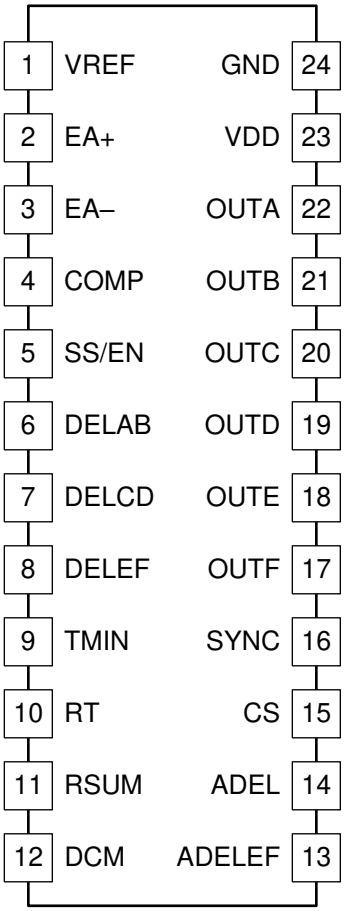

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The IC is connected according to the application schematic shown in datasheet Figure 48, UCC28951-Q1 Typical Application

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VREF	1	VREF short circuit protection	B
EA+	2	FB disabled	B
EA-	3	FB disabled	B
COMP	4	Zero Duty Cycle Demanded	B
SS/ENABLE	5	System will not start up	B
DELAB	6	OUTA, OUTB, minimum turn-on delay, hard switching	C
DELCD	7	OUTC, OUTD, minimum turn-on delay, hard switching	C
DELEF	8	OUTE, OUTF, minimum turn-on delay, hard switching	C
TMIN	9	Minimum duty cycle not set, burst mode threshold unpredictable	C
RT	10	Frequency set maximum value	B
RSUM	11	No Slope compensation, stability Issues	C
DCM	12	DCM mode disable, reverse current is SRs is possible	B
ADELEF	13	No OUTE, OUTF adaptive delay	B
ADEL	14	No OUTA&OUTB, OUTC&OUTD adaptive delay	C
CS	15	Converter will operate at 100% feedback, with no over current protection	B
SYNC	16	Possible device damage	A
OUTF	17	SR FET OFF, OUTF damaged	A
OUTE	18	SR FET OFF, OUTE damaged	A
OUTD	19	OUTD damage; power stage might not be able to regulate output voltage	A
OUTC	20	OUTC damage; power stage might not be able to regulate output voltage	A
OUTB	21	OUTB damage; power stage might not be able to regulate output voltage	A
OUTA	22	OUTA damage; power stage might not be able to regulate output voltage	A
VDD	23	UCC28951-Q1 has no power, supply will not start up.	B
GND	24	No effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VREF	1	VREF voltage raises to ~6V, possible stability Issues	B
EA+	2	No feedback reference to control the output voltage	B
EA-	3	The voltage loop has no feedback and the converter will demand maximum duty cycle	B
COMP	4	The feedback loop is broken, possible stability issues	B
SS/ENABLE	5	No soft start, over shoot at power up, possible noise and stability issues.	C
DELAB	6	OUTA=0, OUTB, OUTC, and OUTD switching normally. Transformer saturation	B
DELCD	7	OUTC=0, OUTA, OUTB, and OUTD switching normally. Transformer saturation	B
DELEF	8	OUTE or OUTF remains high, transformer saturation	B
TMIN	9	Tmin will beset to maximum, OUTC and OUTD switch sporadically, transformer saturation	B
RT	10	OUTA, OUTB, OUTC, and OUTD remain low	B
RSUM	11	No slope compensation, stability issues	C
DCM	12	Loss of DCM function, OUTE and OUTF behaviors are unpredictable. Possible power stage damage	B
ADELEF	13	Erratic delays on OUTE and OUTF. Possible power stage damage	B
ADEL	14	Delay sets to minimum, loss of ZVS	C
CS	15	Becomes voltage mode control, possible transformer saturation and power MOSFET damage	B
SYNC	16	Loss of sync function	C
OUTF	17	SR controlled by OUTF will not turn on, loss of efficiency	C

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUTE	18	SR controlled by OUTE will not turn on, loss of efficiency	C
OUTD	19	Possible transformer saturation, H-bridge FET failure that could lead to IC damage	A
OUTC	20	Possible transformer saturation, H-bridge FET failure that could lead to IC damage	A
OUTB	21	Possible transformer saturation, H-bridge FET failure that could lead to IC damage	A
OUTA	22	Possible transformer saturation, H-bridge FET failure that could lead to IC damage	A
VDD	23	UCC28951-Q1 has no power, supply will not start up.	B
GND	24	Unpredictable current paths could damage the UCC28951-Q1 and system	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VREF	1	EA+	Maximum phase-shift equivalent to maximum duty cycle	B
EA+	2	EA-	Maximum phase-shift equivalent to maximum duty cycle	B
EA-	3	COMP	Error amplifier behaves as a voltage follower, output voltage regulates at a lower value	B
COMP	4	SS/ENABLE	OUTA, OUTB, OUTC, and OUTD remain at low	B
SS/ENABLE	5	DELAB	SS pin voltage remains at 0.75V	B
DELAB	6	DELCD	OUTA=0V, OUTB switch normally, OUTC and OUTD switch at half of the switching frequency. Transformer saturates	B
DELCD	7	DELEF	OUTC=0V, OUTA, OUTB, and OUTD switch normally. OUTE and OUTF remain low. Transformer saturates.	B
DELEF	8	TMIN	OUTC and OUTD behaviors are unpredictable	B
TMIN	9	RT	OUTA, OUTB, OUTC, and OUTD remain low	B
RT	10	RSUM	Slope compensation and frequency will not be accurate	C
RSUM	11	DCM	Slope compensation and DCM thresholds will not be accurate	C
DCM	12	N/A	N/A	N/A
ADELEF	13	ADEL	Turn-on delay time affected, could cause reverse current in SRs. Unpredictable OUTE and OUTF behaviors	B
ADEL	14	CS	Turn-on delay times for ABCD FETs will not be accurate	C
CS	15	SYNC	OCP triggered	B
SYNC	16	OUTF	The SYNC pins maximum voltage rating will be exceeded	A
OUTF	17	OUTE	SR FETs will have 100% duty cycle, OUTE and OUTF damage	A
OUTE	18	OUTD	SR and H Bridge FET timing off could lead to system damage, OUTE and OUTF damage	A
OUTD	19	OUTC	Transformer saturation possible, which could lead to FET and IC failure. OUTC and OUTD damage.	A
OUTC	20	OUTB	Transformer saturation possible, which could lead to FET and IC failure. OUTC and OUTB damage.	A
OUTB	21	OUTA	Transformer saturation possible, which could lead to FET and IC failure. OUTB and OUTA damage.	A
OUTA	22	VDD	Transformer saturation possible, which could lead to FET and IC failure. OUTA damage.	A
VDD	23	GND	No power to the UCC28951-Q1 the system will not start up	B
GND	24	N/A	N/A	N/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VREF	1	Max voltage exceeded, IC damage	A
EA+	2	Max voltage exceeded, IC damage	A
EA-	3	Max voltage exceeded, IC damage	A
COMP	4	Max voltage exceeded, IC damage	A
SS/ENABLE	5	Max voltage exceeded, IC damage	A
DELAB	6	Max voltage exceeded, IC damage	A
DELCD	7	Max voltage exceeded, IC damage	A
DELEF	8	Max voltage exceeded, IC damage	A
TMIN	9	Max voltage exceeded, IC damage	A
RT	10	Max voltage exceeded, IC damage	A
RSUM	11	Max voltage exceeded, IC damage	A
DCM	12	Max voltage exceeded, IC damage	A
ADELEF	13	Max voltage exceeded, IC damage	A
ADEL	14	Max voltage exceeded, IC damage	A
CS	15	Max voltage exceeded, IC damage	A
SYNC	16	Max voltage exceeded, IC damage	A
OUTF	17	OUTF remains high. IC damage	A
OUTE	18	OUTE remains high, IC damage	A
OUTD	19	OUTD remains high. IC damage	A
OUTC	20	OUTC remains high. IC damage	A
OUTB	21	OUTB remains high. IC damage	A
OUTA	22	OUTA remains high. IC damage	A
VDD	23	No effect	D
GND	24	No power to the UCC28951-Q1 the system will not start up	B

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