Application Report

How to Understand LC Table and Select LC About TPS563202

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ABSTRACT

The TPS563202 data sheet includes a table recommending LC. This application report introduces the theory of calculating inductor and output capacitance. Secondly it also introduces how LC affects the loop stability with several typical applications. Finally, it gives a rule to select LC.

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Trademarks

1 Introduction

TPS563202 is the next generation part of TPS563201. TPS563202 uses small SOT563 package which is 1.6mmx1.6mm and uses HotRod package technology. It has good thermal performance and stability. Table 1-1 includes the SOT563 package parts. These parts can be widely used in TV, STB, Routers, switches, AP, and so on.

Table 1-1. SOT563 Package Part Comparison Table

PN	Max loading	Mode	Frequency	Vref voltage	Vref accuracy At room temp
TPS563202	3A	ECO	580k	0.8	2%
TPS563207	3A	FCCM	580k	0.8	2%
TPS562202	2A	ECO	580k	0.8	2%
TPS562207	2A	FCCM	580k	0.8	2%
TPS563231	3A	ECO	600k	0.6	2%
TPS562231	2A	ECO	850k	0.6	2%
TPS563202S	3A	ECO	580k	0.8	1.5%
TPS563207S	3A	FCCM	580k	0.8	1.5%
TPS562202S	2A	ECO	580k	0.8	1.5%
TPS562207S	2A	FCCM	580k	0.8	1.5%

2 The Calculation of LC

2.1 DCAP2 Topology

Application note SLVA546 gives DCAP2 topology block diagram and system function. TPS563202 employ DCAP2 topology, so it can use the way in SLVA546 to assess loop stability. DCAP2 topology block diagram as shown in Figure 2-1 and open transfer function shown in Equation 1 and Equation 2.

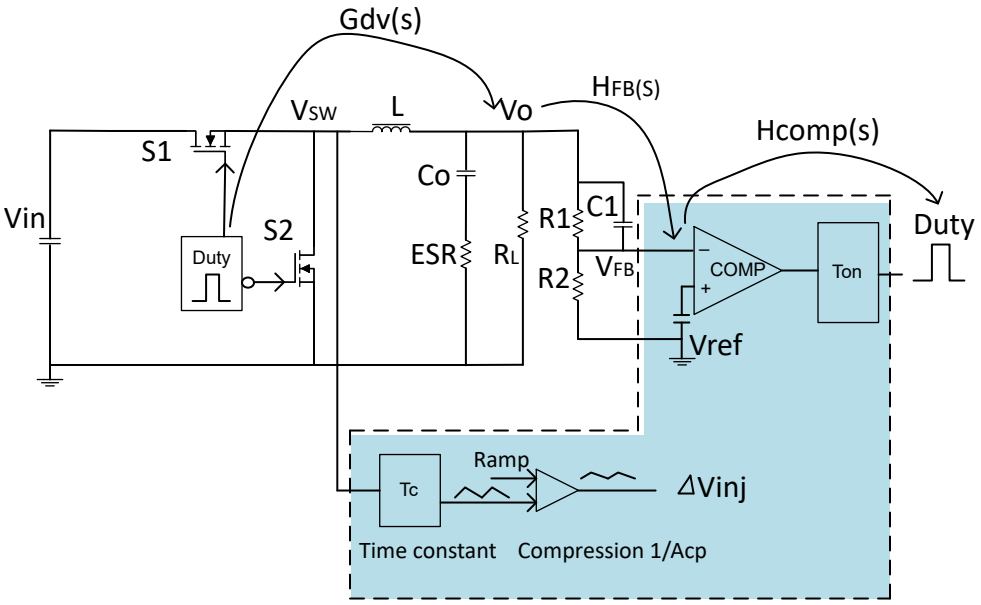

Figure 2-1. DCAP2 Topology Block Diagram

$$G_{open}(s) = G_{dv}(s) \times H_{FB}(s) \times H_{COMP}(s) \times H_d(s)$$
$$= \frac{V_{in} \times (1 + \frac{s}{w_{esr}})}{1 + 2\delta\frac{s}{w_0} + (\frac{s}{w_0})^2} \times \frac{V_{ref}}{V_{out}} \times \frac{A_{cp}}{V_{in}}(1 + sT_c) \times e^{-\frac{sTon}{2}}$$
$$\delta = \frac{\sqrt{\frac{L}{C_{out}}} + R_L(r_L + r_C)\sqrt{C_{out}/L}}{2R_L\sqrt{1 + r_L/R_L}}$$
$$w_0 = \sqrt{\frac{1 + r_L/R_L}{LC_{out}}} \quad (1)$$

$$G_{open}(0) = A_{cp} \times \frac{V_{ref}}{V_o} \quad (2)$$

In Equation 1, $G_{dv}(s)$ is the transfer function from Duty to Vout, $H_{FB}(s)$ is the transfer function of the feedback divider network from Vout to V_{FB}, $H_{COMP}(s)$ is the transfer function from V_{FB} to Duty, $H_d(s)$ is the delay due to fixed on time.

Equation 1 introduces TPS563202 system function. The bode-plot is shown in Figure 2-2 from SLVA546. From the system function and bode-plot, there is a double pole which is decided by inductance and output capacitance. There is a zero which is decided by internal ripple injection circuit. In TPS563202 this zero is constant which is 24kHz. From system function, there is also an ESR zero which is decided by ESR of output capacitance and output capacitance. Normally this zero frequency is put largely after than crossover frequency.

So this zero does not have an effect on bandwidth and phase margin. Figure 2-2 does not show this zero. The DC gain is made by Acp, Vref and output voltage as Equation 2.

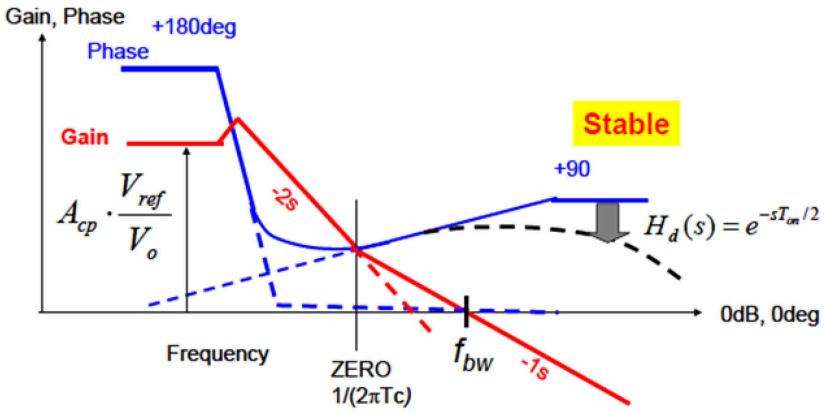

Figure 2-2. Bode plot

2.2 How to Calculate Inductor

To calculate the value of the inductor, LIR is used. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In every cycle, inductor current is LIR times of max output current from Equation 3. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. A good rule is that LIR is normally from 0.2 to 0.5 for the majority of applications. So inductor can be received with Equation 4 based on this rule.

$$\Delta U = L\frac{dI}{dT} = L\frac{I_o \times LIR}{T_{on}} \tag{3}$$

$$L = \frac{V_{in} - V_{out}}{I_o \times LIR} \times \frac{V_{out}}{V_{in} \times f_{sw}} \tag{4}$$

Sometimes the real maximum loading is less than 3A, such as like 1A. In this condition, it still uses maximum loading of the used part to calculate inductance. TPS563202 is a 3A part. It's stable at 3A, of course it's also stable with any below 3A loading, similar to 1A. And it doesn't need to worry about output voltage ripple. Even though the inductor peak to peak current is larger compared with real 1A loading, output voltage ripple is still very small.

Here is uses an example of 12 V input voltage to 5 V output voltage based on TPS563202. Maximum loading of TPS563202 is 3A. The real loading is only 1A in one application. Based on Equation 4, LIR is set to 0.35. So inductor should be set to 4.7uH. If so, inductor peak to peak current is about 1.05A which is even larger than real 1A loading. But it's no any problems in real application. Figure 2-3 is waveform at 1A loading, Figure 2-4 is waveform at 3A loading. From waveforms, inductor peak to peak current does be 1A, but output voltage ripple is less than 50mV at both 1A and 3A loading.

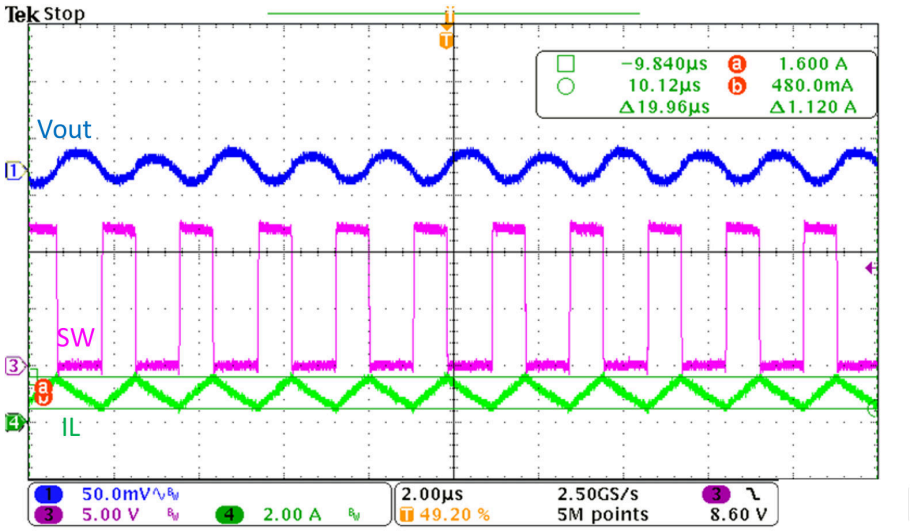

Figure 2-3. Ripple at 1A Loading

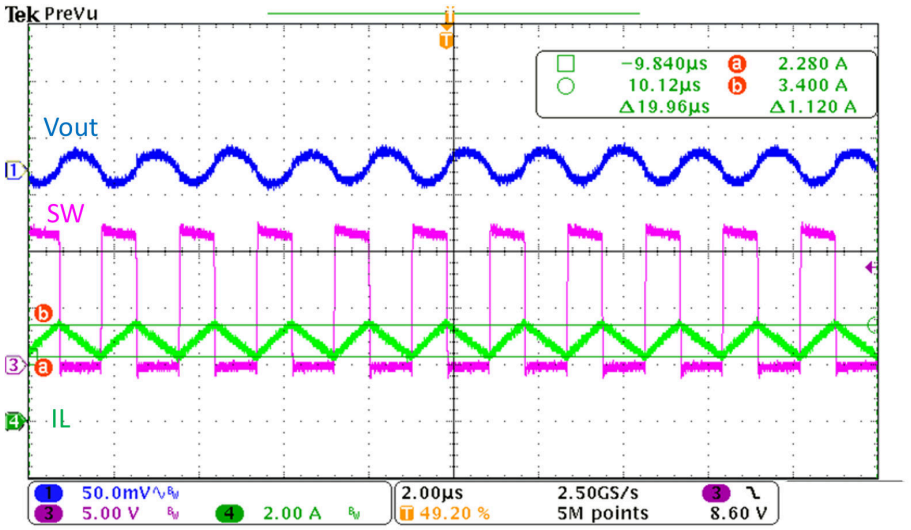

Figure 2-4. Ripple at 3A loading

2.3 How to Calculate Output Capacitance

In second chapter, it introduces system and bode plot of DCAP2 topology. It's suggested to put double pole frequency marginally smaller than internal zero frequency. The internal zero can boost phase higher. So the system can get a larger bandwidth and a higher phase margin at crossover frequency. The internal zero frequency of TPS563202 is 24kHz, So it's good to put double pole frequency to about 20kHz as Equation 5. Output capacitance Cout is received from Equation 6.

$$f_{double\ pole} = \frac{1}{2\pi\sqrt{LC_{out}}} = 20kHz \tag{5}$$

$$C_{out} = \frac{1}{L \times (2\pi f_{double\ pole})^2} \tag{6}$$

MLCC capacitance is widely used in application because of its small size, low ESR and good price. But degrading of MLCC capacitance is very large when adding a DC bias voltage, especially at higher DC bias voltage. The degrading couldn't be ignored in calculating output capacitance. It introduces an example of MuRata capacitance GRM21BR61A226ME44 which is 10V, 22uF, and 0805 footprint. Figure 2-5 is degrading curve. From the figure, the capacitance degrades by 50% at 5V bias voltage. If the MLCC capacitance rated voltage is smaller, or footprint is smaller, it degrades much larger. In the calculation of output capacitance, the degrading of MLCC capacitance could not be ignored.

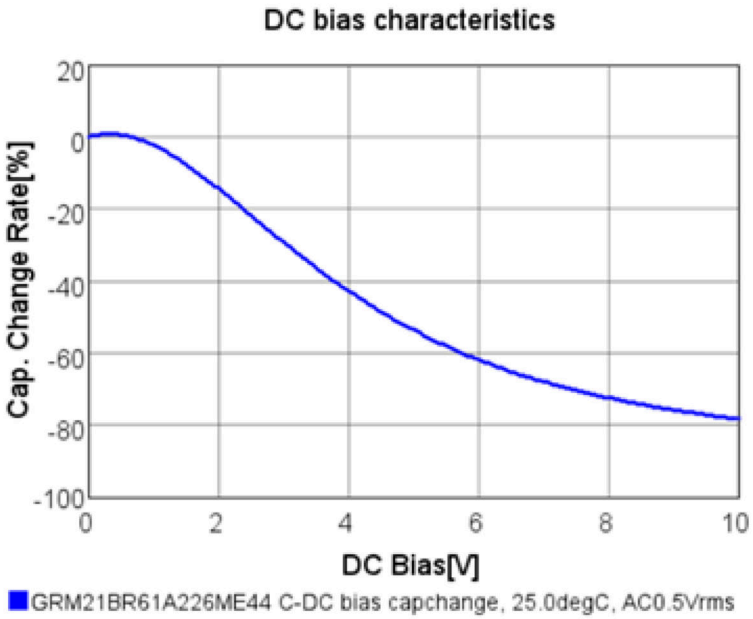

Figure 2-5. GRM21BR61A226ME44 C-DC Bias Voltage

3 Typical Application

The first example is a typical application which input voltage is 12 V, output voltage is 1.5 V. In the following examples, input voltage and output voltage do not change. It only changes inductance or output capacitance to see how they affect loop stability. And output capacitance uses GRM21BR61A226ME44 which is introduced in previous chapter.

Based on Equation 4, if LIR is set to 0.4, calculated inductance is 1.89uH. This example inductor uses 1.5uH.

Based on Equation 6, output capacitance should be 42.3uF. The output capacitance degrades by 10% at 1.5 V bias voltage. The effective capacitance is 19.8uF. Here output capacitance uses 2pcs capacitance. The total effective capacitance is 39.6uF. Double pole should be 20.6kHz. The schematic is shown in Figure 3-1.

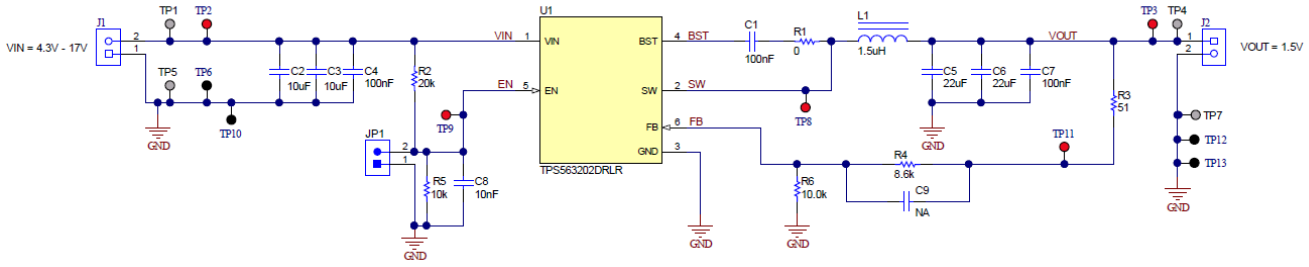

Figure 3-1. Schematic of 12Vin to 1.5Vout

By using frequency response analyzer to run AC analysis, bode plot is shown in Figure 3-2. Double pole is about 20kHz. Internal zero is 24kHz. After double pole gain curve decreases at -40dB per decade rate. And after zero point it decreases at -20dB/Dec. The ESR of MLCC capacitance is very small about 2mohm, so zero frequency is very high about 1.88MHz which doesn't have any effect on bandwidth and phase. Crossover frequency is 152.64kHz. Phase margin is 46 degree. It's stable and bandwidth is large, so it has good load transient response.

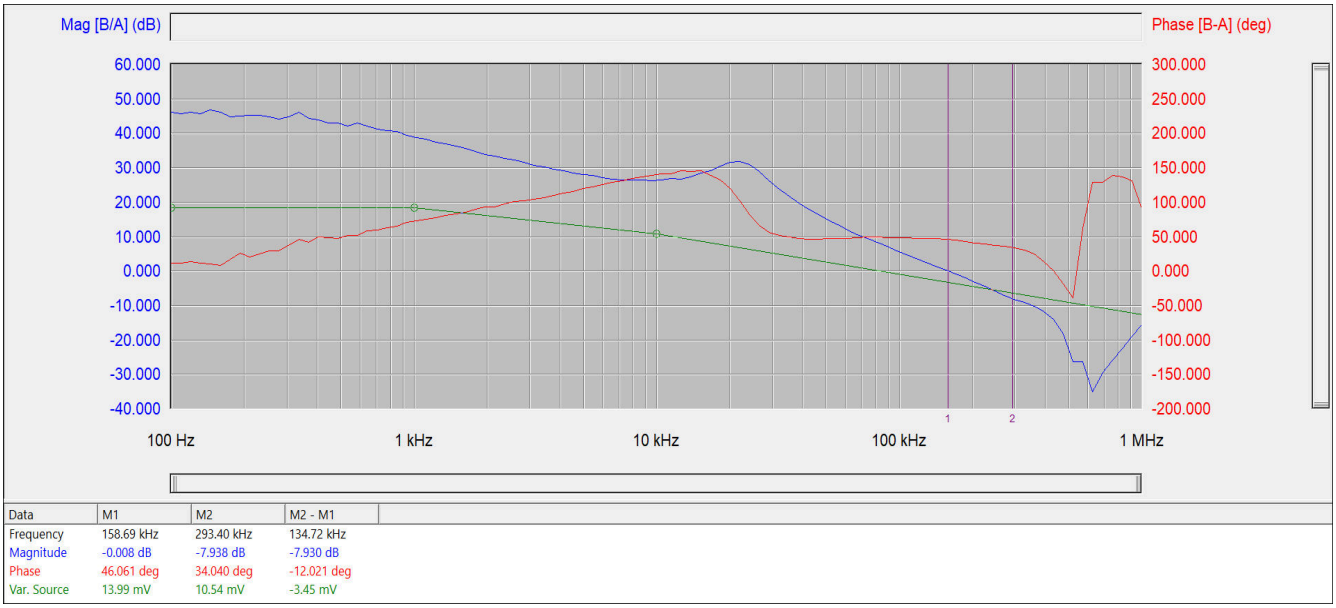

Figure 3-2. Bode Plot of 12Vin to 1.5Vout with 1.5uH Inductor and 2x22uF Capacitance

Some might be curious about the result that double pole is set to be higher or lower than 20kHz or what is the range of double pole. The following uses several cases to explain the process.

If setting double pole to 10kHz, it needs to increase inductor and output capacitance together. Based on Equation 4, if LIR is set to 0.2, calculated inductance is 3.77uH. In this case inductor uses 3.3uH. Based on Equation 6, calculated capacitance is 76.8uF. Here output capacitance uses 4pcs 22uF capacitance.

Use frequency response analyzer to run AC analysis. Bode plot shown in Figure 3-3. Double pole is about 10kHz which match with calculated value. At 10kHz, gain curve begin to decrease at -40dB/Dec. After 24kHz, slew rate changes to -20dB/Dec. So bandwidth is smaller which is 55kHz. At 10kHz, phase drops too much because of double pole effect. Then phase curve begins to increase slowly by the effect of internal zero. Phase margin is 44 degree.

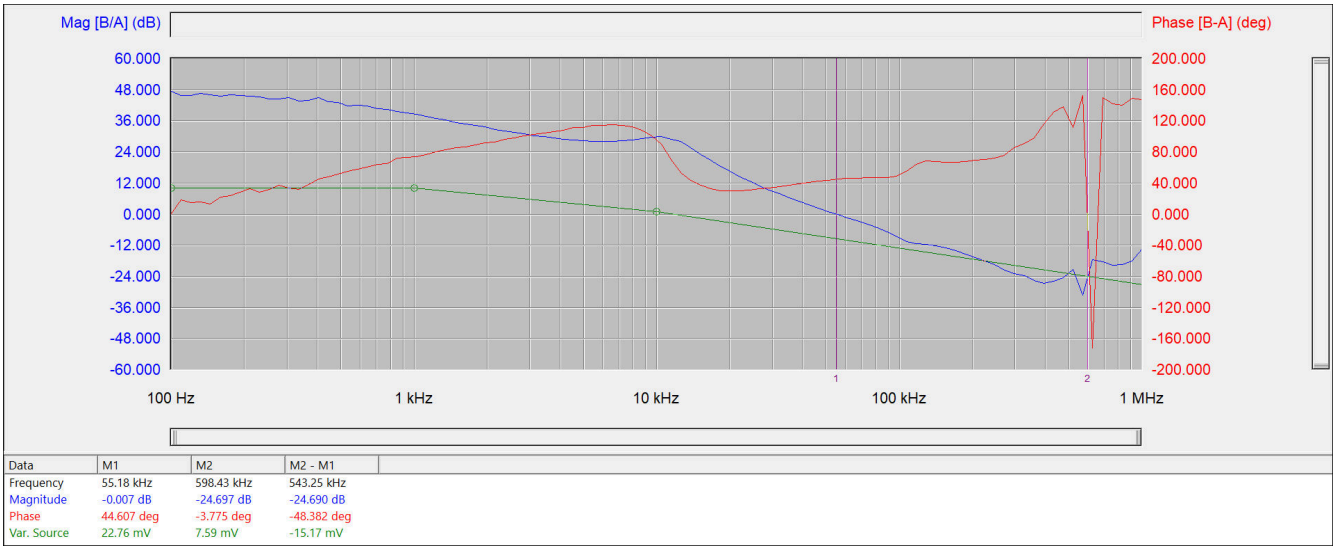

Figure 3-3. Bode Plot of 12Vin to 1.5Vout with 3.3uH Inductor and 4x22uF Capacitance

In this condition, it is suggested to add a 100pF CFF to increase phase margin. This CFF capacitance will increase a zero point and a pole point which frequency are as shown in Equation 7.

$$f_{CFF\_zero} = \frac{1}{2\pi R_{top} CFF}$$

$$f_{CFF\_pole} = \frac{1}{2\pi (R_{top} // R_{bottom}) CFF} \quad (7)$$

Based on Equation 7, f_{CFF_zero} is 185kHz, f_{CFF_pole} is 346kHz. So this CFF zero point only increases phase from 18.5kHz, and doesn't have an effect on gain. Figure 3-4 is tested bode plot with 100pF CFF. Bandwidth is still 59kHz and phase margin improves to 55 degree.

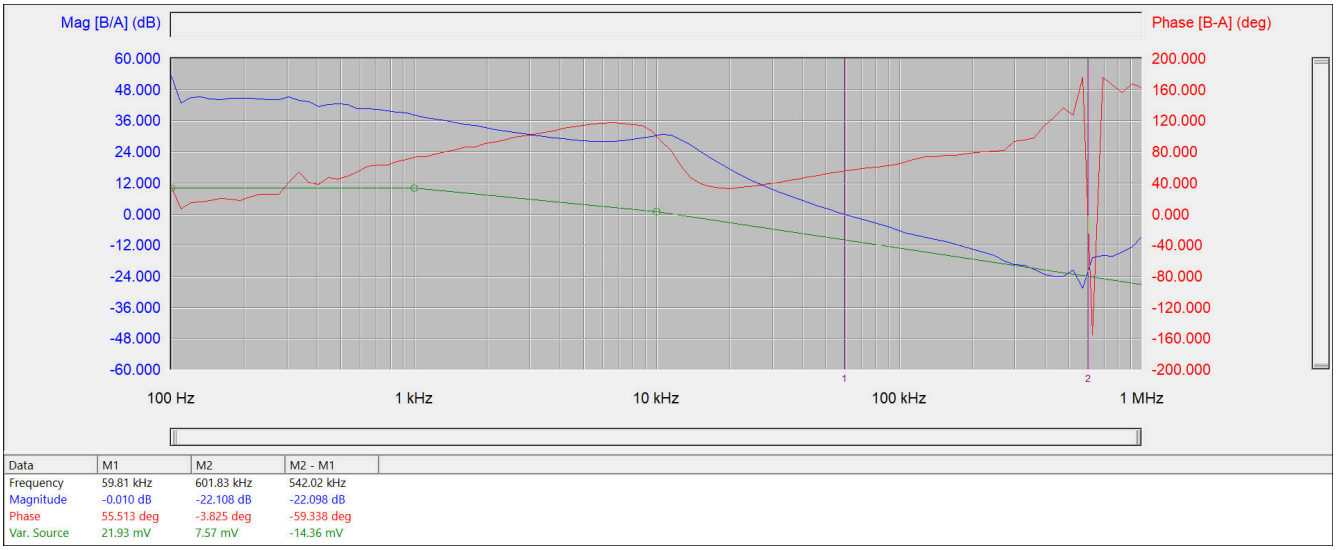

Figure 3-4. Bode Plot of 12Vin to 1.5Vout with 3.3uH Inductor, 4x22uF Capacitance and 100pF CFF

Another condition about lower double pole is to add a bulk output capacitance. Sometimes customers like to add a bulk capacitance at output port such as 100uF or even 220uF. Normally this kind of bulk capacitance has larger ESR. Larger ESR and bulk output capacitance make the frequency of zero small. So in this conditions ESR zero point couldn't be ignored. Because it affects bandwidth and phase.

Based on previous case of 1.5uH inductor and 2x22uF output capacitance, it adds another 220uF electronic capacitance which ESR is 25m ohm. The double pole frequency is 8kHz. And ESR zero frequency is 24.3kHz. Figure 3-5 is tested bode plot. After double pole, there is an ESR zero at 24.3kHz and internal zero at 24kHz. So gain curve becomes flat after 30kHz. The gain curve will drop at a pole frequency which is added by internal Ramp circuit. The pole frequency of TPS563202 is about 200kHz. Because ESR zero is in bandwidth, it makes bandwidth large.

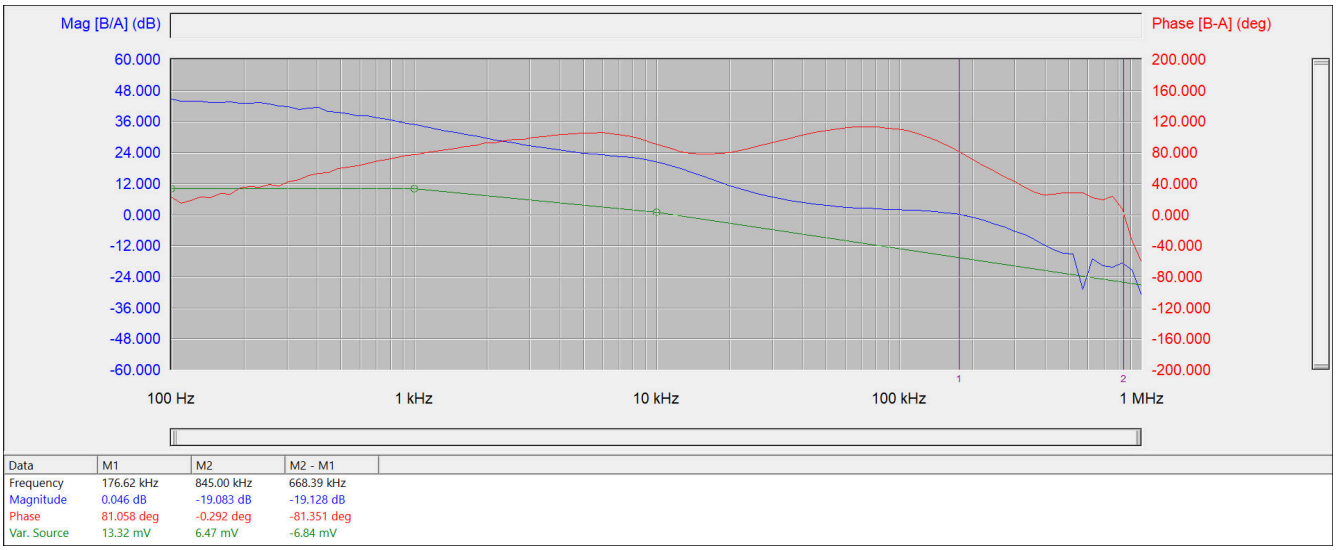

Figure 3-5. Bode Plot of 12Vin to 1.5Vout with 1.5uH Inductor and 2x22uF+220uF Capacitance

If setting double pole to 30kHz, inductor still uses 1.5uH, and calculated capacitance is 18.8uF based on Equation 6. It uses only one 22uF capacitance. Figure 3-6 is tested bode plot. Double pole is 30kHz, bandwidth is 262kHz. In high frequency the on time delay(Hds) makes phase drop quickly. Phase is only 24 degree. So it's not suggested to put double pole after internal zero.

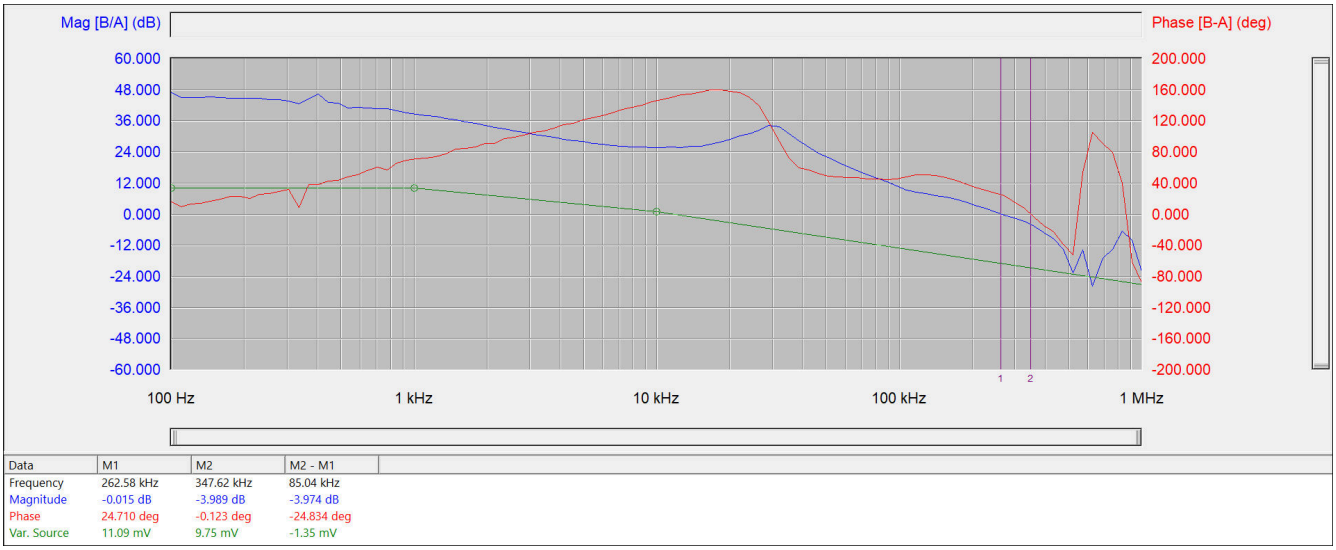

Figure 3-6. Bode Plot of 12Vin to 1.5Vout with 1.5uH Inductor and 22uF Capacitance

From the examples, it is suggested to set double pole marginally before internal zero. It can get large bandwidth and good phase margin. Also, it is not a problem to set double pole before or largely before internal zero. And in this condition, it is suggested to add a CFF capacitance to increase phase margin. Finally it's not suggested to put double pole after internal zero.

4 Summary

This application report presents how to calculate inductor and output capacitance and how they affect loop stability about TPS563202. It also gives a typical rule to select inductor and output capacitance. It is recommended to put double pole before internal zero frequency. To be safer please follow recommended LC table. The zero frequency of the SOT563 package parts in Table 1-1 is 24kHz.

5 References

- Texas Instruments, D-CAP2TM Frequency Response Model based on frequency domain analysis of Fixed On-Time with Bottom Detection having Ripple Injection application report.
- Texas Instruments, TPS563202 4.3-V to 17-V Input, 3-A Synchronous Buck Converter in SOT563 data sheet.

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