Application Note

Most Frequently Asked Questions About the UCC25640x LLC Resonant Controller

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ABSTRACT

This application note discusses the UCC25640x LLC resonant controller's most frequently asked questions when used in different applications.

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1 UCC25640x Frequently Asked Questions

1.1 For the Time Domain Simulation and Fundamental Harmonic Analysis of LLC Resonant Converters, What Model of the Transformer Should be Used?

The LLC topology can be realizable with the following:

- An external inductor and a tightly coupled transformer, or
- With a integrated transformer with a poor coupling which integrates both resonant and magnetizing inductors.

In both of these implementations, the transformer can be modeled as T-type [1] or APR models which are shown in the following images. These two models can be used for both time domain simulation and also for fundamental harmonic analysis. Equation 1, Equation 2, Equation 3 describe the behavior of all the models given in Figures 1 to 4. Reference [2] shows the different transformer model derivations from a coupled inductor transformer model. Also, the videos given here: Clarifying Coupled Inductor and Transformer Modeling, Transformer leakage in LLC converters, Leakage models of multi-winding transformer and implications to LLC converter demonstrates different transformer models and their performance using spice simulation tool.

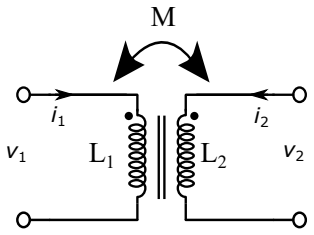


Figure 1-1. Mutual Inductance Model

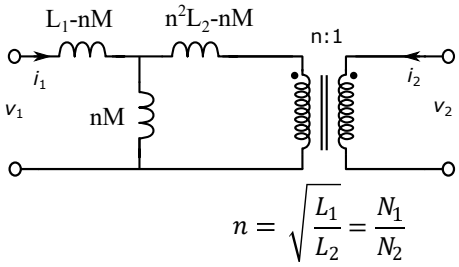


Figure 1-2. T Type Transformer Model

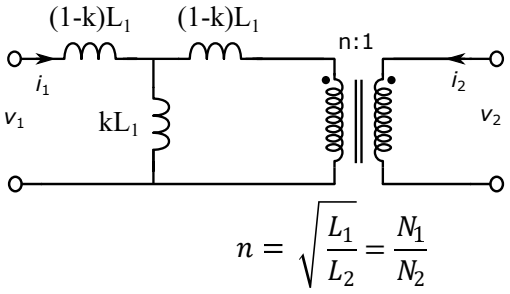


Figure 1-3. T Type Transformer Model Considering Coupling Coefficient k

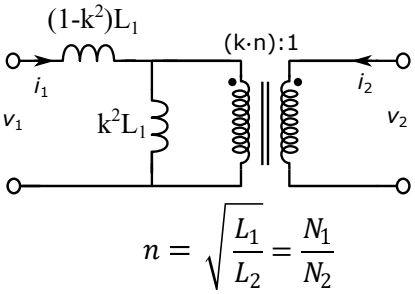


Figure 1-4. All Primary Referred (APR) Model

$$v_1 = L_1\frac{di_1}{dt} + M\frac{di_2}{dt} \quad (1)$$

$$v_2 = L_2\frac{di_2}{dt} + M\frac{di_1}{dt} \quad (2)$$

$$k = \frac{M}{\sqrt{L_1 L_2}} \quad (3)$$

where L_1, L_2, M, k are primary open circuit inductance, secondary open circuit inductance, mutual inductance, coupling coefficient respectively.

The parameters of the models shown above can be calculated from the transformer data sheet parameters where primary open circuit Inductance (L_p) and primary inductance when secondaries are short (L_{lk}), turns ratio are provided.

$$k = \sqrt{1 - \frac{L_{lk}}{L_p}} \quad (4)$$

$$L_1 = L_p \quad (5)$$

$$n = \text{turns ratio} \quad (6)$$

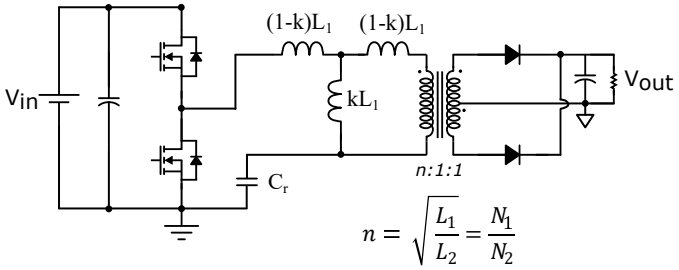


Figure 1-5. T-type Transformer Model for LLC Design and Analysis

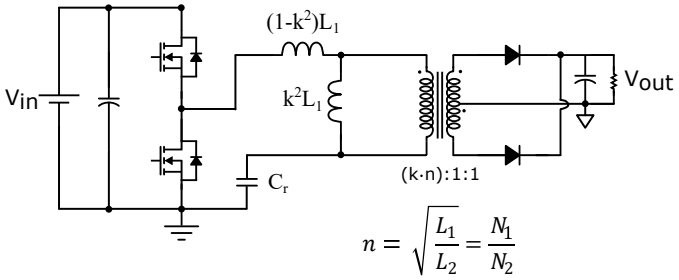


Figure 1-6. APR-Type Transformer Model for LLC Design and Analysis

To validate models, a closed loop simplis simulation with both T-type model shown in Figure 1-5 and APR model shown in Figure 1-6 has been built with the same transformer parameters as that of UCC25640x EVM hardware [3] where integrated transformer from Wurth Electronics [4] is used. In the transformer data sheet, L_p, L_{lk}, n are given as 510uH, 82uH, 16.5 respectively. From Equation 4, Equation 5, Equation 6, the parameters of the transformer obtained as k =0.916, L_1=510uH, n=16.5, k*n=15.115. Figure 1-7 shows the comparison between EVM measurements and closed loop Simplis models. We can observe that in all the cases the operating frequency is almost same for a given input voltage.

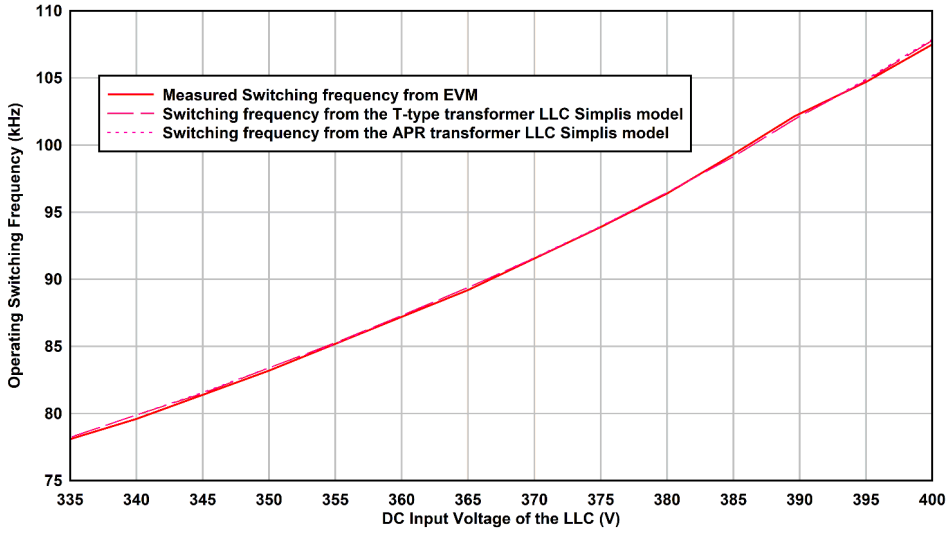


Figure 1-7. Input Voltage vs Switching Frequency From Closed Loop Simulation Model and From the EVM Measurements at 12 V, 15 A Load

1.1.1 LLC Design Using T Type Transformer Model

The reference [19] shows the LLC design using APR model whereas the reference [1] shows the LLC design using T-type transformer model. Here, for this design example, UCC25640xEVM specifications[3] with T-type transformer model is considered.

Table 1-1. UCC25640EVM-020 Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
	INPUT CHARACTERISTICS					
	DC voltage range		365	390	410	VDC
	AC voltage range		85		265	VAC
	AC voltage frequency		47		63	Hz
	Input DC UVLO On			365		VDC
	Input DC UVLO Off			330		VDC
	OUTPUT CHARACTERISTICS					
V_{OUT}	Output voltage - Normal mode	Burst mode threshold to full load = 15 A		12		VDC
I_{OUT}	Output load current	365 to 410 VDC			15	A
	Output voltage ripple	390 VDC and full load = 15 A		120		mVpp
	SYSTEM CHARACTERISTICS					
	Resonant frequency			100		kHz
	Peak efficiency	390 VDC, load = 8 A		93%		
	Operating temperature	Natural convection		25		°C

LLC Voltage Gain with T-type Transformer Model

Equation 7 gives voltage gain expression for T-type transformer model shown in Figure 1-5.

$$\text{Voltage Gain: } M(k,fr,Q) = \frac{1}{\sqrt{\left[\frac{1}{k}\left[1-\frac{1-k^2}{fr^2}\right]^2\right]^2 + \left[\frac{1}{k\cdot Q}\left[fr-\frac{1}{fr}\right]\right]^2}} \tag{7}$$

where

Normalized frequency: $fr = \frac{\omega}{\omega_0}$

Angular resonant frequency between leakge inductance (primary-side inductance when the secondary side is completely short-circuited) and Cr: $\omega_0 = \frac{1}{\sqrt{L_{lk}\cdot C_r}}$

Angular resonant frequency between primary inductance (self-inductance of the primary winding) and Cr: $\omega_s = \frac{1}{\sqrt{L_p\cdot C_r}}$

Characteristic impedance: $Z_0 = \sqrt{\frac{L_{lk}}{C_r}}$

$$Q = \frac{R_{ac}}{Z_0} = \frac{8\cdot n^2}{\pi^2}\cdot\frac{R_L}{Z_0}$$

n : primary to secondary turns ratio

k : Coupling coefficient between primary and secondary winding of the transformer

Design Example

Nominal Input Voltage: $V_{in\_Nom} = 390V$ (8)

Output Voltage: $V_{out} = 12V$ (9)

Nominal Output Power: $P_{out} = 180W$ (10)

Output Voltage ripple: $120mVpp$ (11)

Voltage drop due to power losses: $V_{loss} = \frac{\frac{180W}{93\,\%} \cdot 7\,\%}{15A} = 0.9V$ (12)

Coupling coefficient considered for this design: $k = 0.92$ (13)

Gain at the resonant frequency: $M_{fo} = \frac{1}{k} = 1.087$ (14)

Primary to Secondary turns ratio: $n = M_{fo} \cdot \frac{V_{in\_Nom}}{2 \cdot (V_{out} + V_{loss})} \cong 16.5$ (15)

Equivalent Output Load Resistance: $R_L = \frac{12V^2}{180W} = 0.8\Omega$ (16)

Equivalent AC Load Resistance: $R_{ac} = \frac{8 \cdot n^2}{\pi^2} \cdot R_L = 176.542$ (17)

Minimum DC Input Voltage: $V_{in\_\min} = 365V$ (18)

Maximum DC Input Voltage: $V_{in\_\min} = 410V$ (19)

Maximum gain requirement: $M_{\max} = \frac{2n \cdot (V_{out\_\max} + V_{loss})}{V_{in\_\min}} = \frac{2 \cdot 16.5 \cdot (12 + 0.06 + 0.9)}{365} = 1.172$ (20)

Minimum gain requirement: $M_{\min} = \frac{2n \cdot (V_{out\_\min} + V_{loss})}{V_{in\_\max}} = \frac{2 \cdot 16.5 \cdot (12 - 0.06 + 0.9)}{410} = 1.033$ (21)

Q of 3.5 is considered for this design (22)

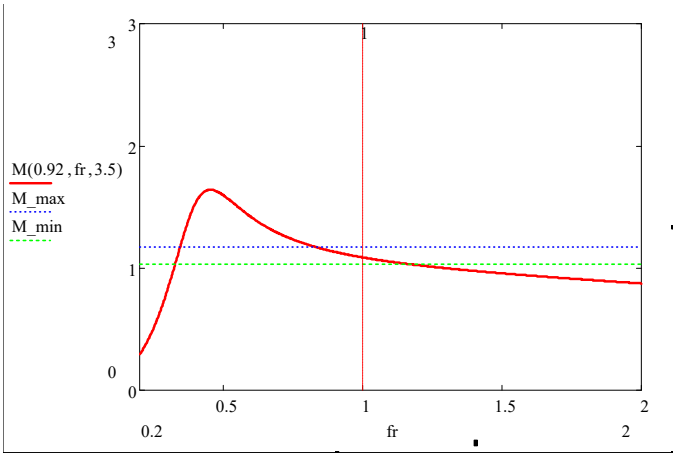


Figure 1-8. Gain Frequency Plot for k=0.92 and Q=3.5

Characteristic Impedance: $Z_0 = \frac{R_{ac}}{Q} = \frac{176.542}{3.5} = 51.5$ (23)

Resonant Frequency: $f_o = 100kHz$ (24)

Resonant Capacitor Value: $C_r = \frac{1}{2\pi \cdot Z_0 \cdot f_o} = 31.5nF$ (25)

Primary Leakage Inductance when the secondaries are short circuited: $L_{lk} = \frac{Z_0}{2\pi f_o} = 80\mu H$ (26)

Primary Inductance when the secondaries are open circuited: $L_p = \frac{L_{lk}}{1 - k^2} = 522\mu H$ (27)

Final value of resonant capacitor value selected: $C_r = 30nF$ (28)

Leakage Inductance, primary Inductance, turns ratio values given in the transformer data sheet: $L_{lk} = 82\mu H, L_p = 510\mu H, n = 16.5$ (29)

The final resonant frequency: $f_0 = \frac{1}{2\pi\sqrt{L_{lk} \cdot C_r}} = 101.5kHz$ (30)

1.2 How to Connect External Gate Drivers to the UCC25640x for High Gate Driver Current Capability?

Figure 1-9 shows a simpler way of connecting external gate drivers to the UCC25640x. Here two low-side drivers such as UCC27517A [5] is used which has a higher output current capability. Here the external high side driver is bootstrapped just like the internal driver of the UCC25640x.

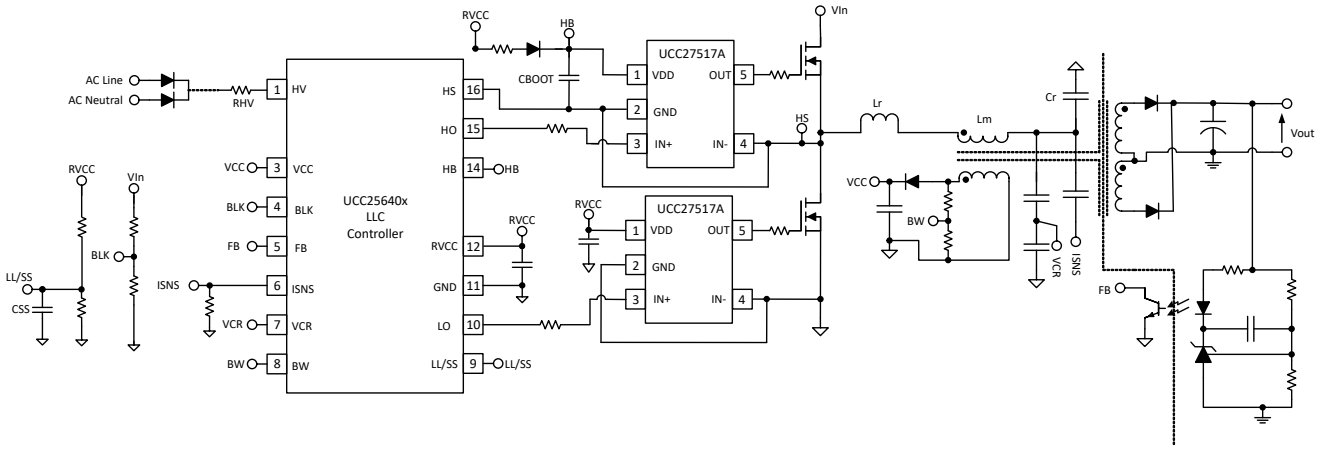


Figure 1-9. External Driver Interface to the UCC25640x

1.3 When Powering on the PFC-LLC AC-DC Converter, What Sequence is Recommended?

Normally, LLC can start switching before the PFC output voltage starts rising or vice versa depending on system requirement.

In general, PFC output voltage starts rising before the LLC converter starts switching. The output voltage rising is done to make sure the LLC is able to achieve regulation when starting into heavy load without risking going into the capacitive region. UCC25640x RVCC is designed for this purpose. In case of UCC256402/404, once the AC input is provided and VCC reaches 26-V level, RVCC voltage is generated to power up PFC controller for PFC to boost. Once PFC boost to a level above UCC25640x BLK setting, LLC DC-DC start to operate. For any reason, if the BLK voltage reaches below BLKstop, switching stops.

In the case of TVs, during light load, LLC converter need to startup before PFC output voltage rises. In this type of scenario, UCC256404 is recommended, since the BLK turn on threshold of this controller is only 1 V. Since LLC transformer was designed for input voltage>300 V and full load, there is not any issue of triggering OCP protection.

1.4 How to Eliminate the Nuisance ZCS Detection During the Light Load?

During light load, the magnitude of resonant current is very small at the turn off of high-side or low-side MOSFET. This step can trigger the ZCS protection.

The following methods helps to avoid nuisance ZCS detection during light load:

1. Increasing the burst mode threshold (BMTH): ZCS is disabled if the FBreplica signal is lower than BMTH threshold during light load.
2. Reducing the magnetizing inductance of the transformer to increase the magnetizing current at light load.
3. Reducing output voltage of PFC if there is PFC in the application.

1.5 What is the Purpose of Maintaining the FB Pin Voltage of the UCC25640x Controllers at a Constant Level?

The UCC25640x controller attempts to loosely regulate the FB pin voltage to around 5.6 V. This regulating is done to provide better transient response and avoid some of the delays associated with the opto-coupler being saturated. When a current pulled out of the FB pin is within 0uA to FB pin maximum source current (164 uA for 402 and 404 devices, 246 uA for 403), the FB pin voltage can be around 5.6 V. When the opto-coupler pulls more current than the FB pin can support, the controller can allow the FB pin voltage to collapse to 0 V.

1.6 How to Improve the Slew Rate Detection at HS Pin of the UCC25640x Controller?

UCC25640x has a minimum detectable slew rate of 100 mV/ns. As soon as the high side gate (HO) is turned off, the low side gate (LO) is be turned on after the slew rate has been detected. If the slew rate detection is missed, the dead time depends on the resonant current polarity (Section 1.19). Figure 1-10 shows a way of extracting slew rate information during the dead time [10]. In this simulation Infineon IPW6075CP MOSFET is used as an example. Figure 1-11 shows the switch node voltage transition when a current of 0.7 A is being pulled out from switch node. Here we can observe that switch node voltage has different slew rates during the transition which is due to non linear capacitance (Figure 1-15) seen at the switch node. This non linear capacitance is combination of Coss of the both upper (voltage changing from 0 V to 390 V) and lower (voltage changing from 390 V to 0 V) MOSFETs as shown in Figure 1-13 and Figure 1-14. The Coss graphs of each MOSFETs are extracted using the SIMetrix simulation. The extractions are shown in Figure 1-12.

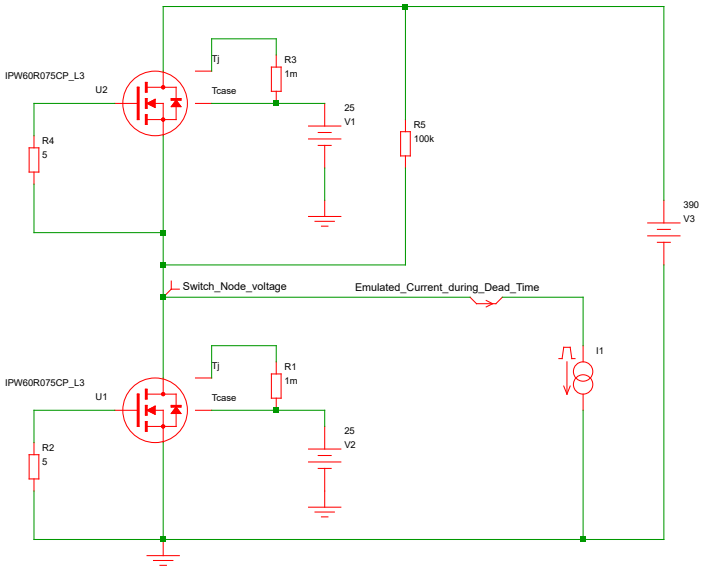


Figure 1-10. SIMetrix Simulation for Finding Switch Node Slew Rate During Dead Time

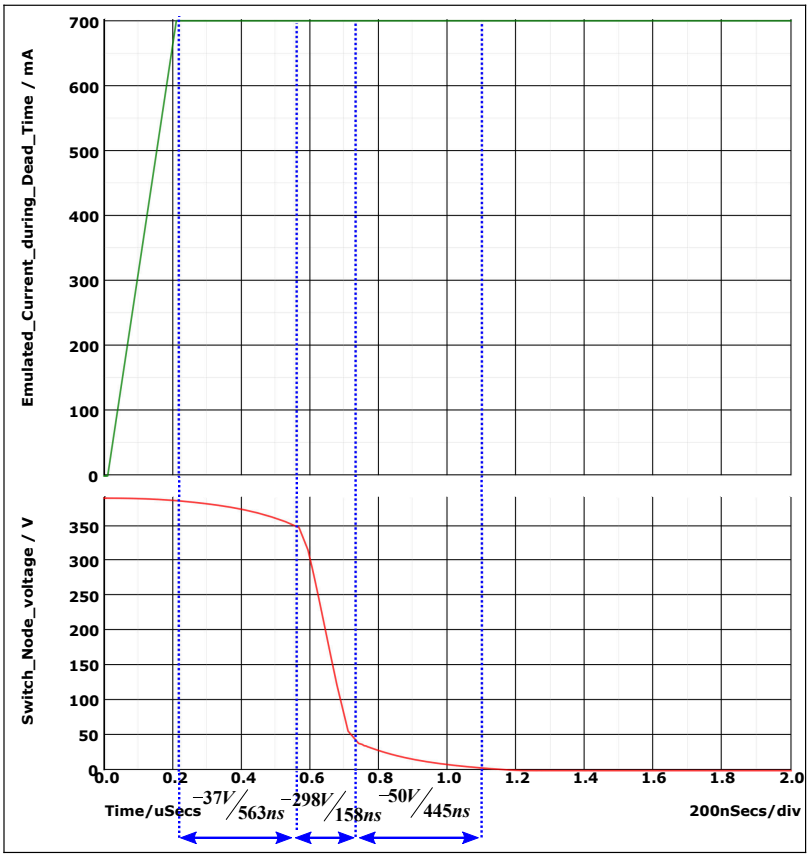


Figure 1-11. Switch Node Voltage Slew Rates During Dead Time

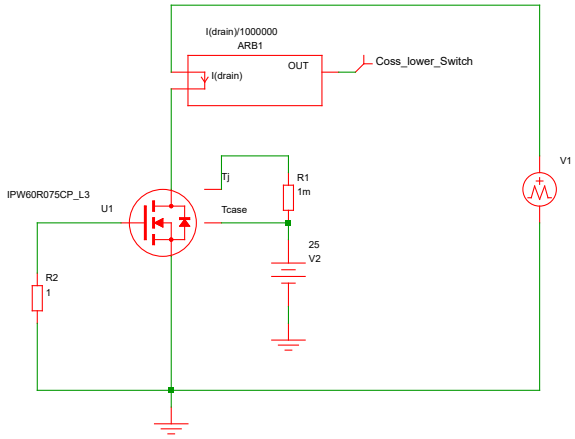


Figure 1-12. Coss Extraction From Device Model Using SIMetrix

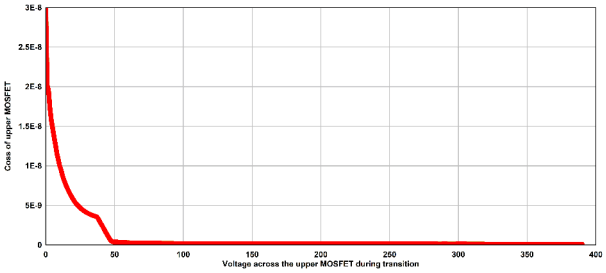


Figure 1-13. Upper MOSFETs Coss vs Drain to Source Voltage

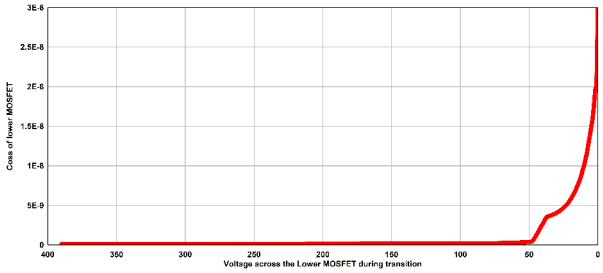


Figure 1-14. Lower MOSFETs Coss vs Drain to Source Voltage

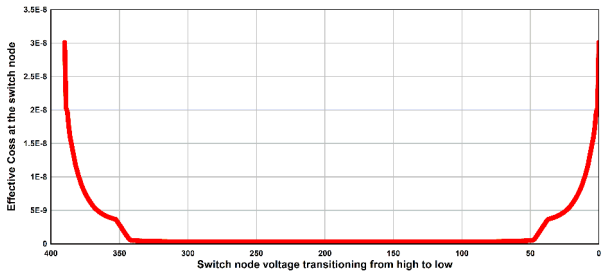


Figure 1-15. Coss Seen at the Switch Node vs Switch Node Voltage

The following methods can be followed to improve the slew rate detection:

1. Increase the MOSFET turn off speed: Most designs include a diode in the HO/LO gate drive paths to allow for independent turn on and turn off speed. Such a circuit is recommended to increase the turn off speed of the gate drive.
2. Using MOSFETs with lower output capacitance (Coss): The lower Coss allow for a faster switch node slew rate.
3. Using a higher burst mode setting: A higher burst mode setting have larger magnetizing current amplitude which help with achieving the dV/dt criteria (Increasing the burst threshold make the LLC burst with slightly more power within the burst packet and the resonant current amplitude can be higher.
4. Reducing any snubber capacitance on the switch node
5. Reducing the magnetizing inductance of the transformer to increase the magnetizing current at light load.

1.7 How to Operate the UCC25640x Controller in the Open Loop?

Running UCC25640x open loop can require some modifications to the VCR circuitry as well as the FB pin to sink a constant current out of the FB pin (Figure 1-16). Since the FB pin is loosely regulated to approximately 5.6 V, connecting a resistor (R_{FB}) from FB to ground sinks a fixed current (somewhere between 0 uA and 82 uA for 402/404 devices. 164 uA for 403 devices). The amount of current can determine the switching thresholds ((V_{TH}-V_{TL}) =$V_{vcr\_pk\_pk}$) for VCR. And then depopulate the top VCR capacitance so that charge control is completely disabled. Now the switching frequency (f_{sw}) is only dependent on the internal 2 mA ramp current and the lower VCR capacitance (C_{VCR_lower}).

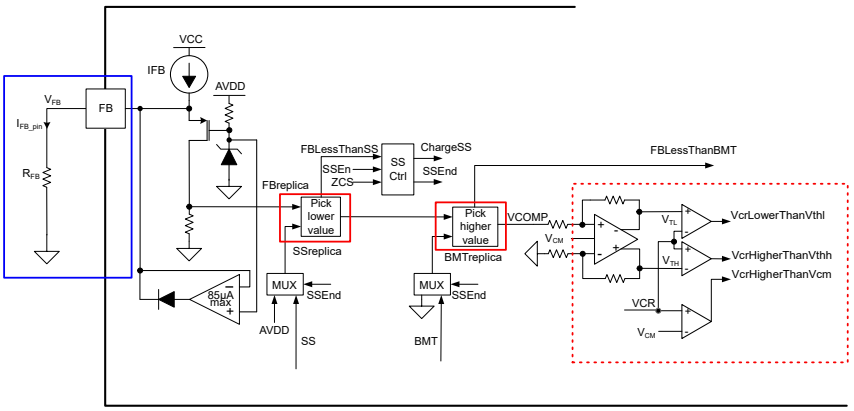


Figure 1-16. Operating the UCC25640x in the Open Loop by Connecting a Resistor at the FB Pin

The amount of current sunk out of the FB pin: $I_{FB\_pin} = \frac{V_{FB}}{R_{FB}} = \frac{5.6}{R_{FB}}$ (31)

VCR peak to peak voltage: $V_{vcr\_pk\_pk} = (82\mu A - I_{FB\_pin}) \cdot 100k\Omega$ (32)

Switching frequency: $f_{sw} = \frac{2mA}{2 \cdot V_{vcr\_pk\_pk} \cdot C_{VCR\_lower}}$ (33)

Design Example

Required Switching Frequency: $f_{sw} = 100kHz$ (34)

Value of Capacitor connected at the VCR pin to ground: $C_{VCR\_lower} = 10nF$ (35)

VCR pin peak to peak voltage would be: $V_{vcr\_pk\_pk} = \frac{2mA}{2 \times f_{sw} \times C_{VCR\_lower}} = \frac{2mA}{2 \times 100kHz \times 10nF} = 1V$ (36)

Current that needs be pulled out from the FB pin: $I_{FB\_pin} = 82\mu A - \frac{V_{vcr\_pk\_pk}}{100k\Omega} = 82\mu A - \frac{1V}{100k\Omega} = 72\mu A$ (37)

Resistance that needs to be connected at the FB pin: $R_{FB} = \frac{5.6V}{72\mu A} = 78k\Omega$ (38)

1.8 What Happens if the VCR Pin Peak to Peak Voltage of the Controller Exceeds 6 V?

VCR pin voltage is internally clamped. The voltage does not go above +7 V or below -0.8 V. 7 V is the internal AVDD rail that powers the VCR circuitry. At -0.8 V, the internal ESD diode can likely conduct. VFB replica peak to peak is clamped to 6 V. If the amplitude on the VCR pin exceeds 6 V peak to peak, the controller is unable to push the switching frequency any lower the controller has run out of room on the VCR, and as a result the converter gets clamped to this minimum switching frequency and the output voltage droops. If the peak to peak voltage on VCR exceeds 6 V, reducing the top VCR capacitor or increasing the bottom VCR capacitor can help to reduce the peak to peak voltage.

1.9 What UCC25640x settings effect the startup duration of the LLC?

In general, the soft start profile of the LLC is normally fine-tuned on bench by adjusting the LL/SS soft start capacitance, soft start initial voltage, VCR capacitors, and feedback loop response. Section 2 of the [7] gives more details on soft start timing and switching frequency tuning during the startup.

1.10 What is Causing the Current Imbalance in the LLC's Secondary Side Windings?

In the LLC center tapped transformer, if the primary to secondaries leakage inductance are different, we can observe that secondary peak currents can be different during each half of the switching period. This can cause one of the diodes overheating. To avoid this, both the secondary winding voltages has to be tightly coupled with the primary so that leakage inductance variation is very small between these windings.

To see the current imbalance on the secondary side, two simulations are considered. Case one: With the equal coupling between primary and secondary windings which is shown in Figure 1-17 (This figure shows all the T-type equivalent models) and Case 2: With the unequal couplings which is shown in Figure 1-18. The EVM parameters are used for both the simulations: k =0.916, L_1=510uH, n=16.5, C_r=30nF, f_{sw}=101.5kHz, Load Resistance=0.8 Ohm. We can observe the secondary side currents imbalance in Figure 1-20 compared to the currents shown in Figure 1-19.

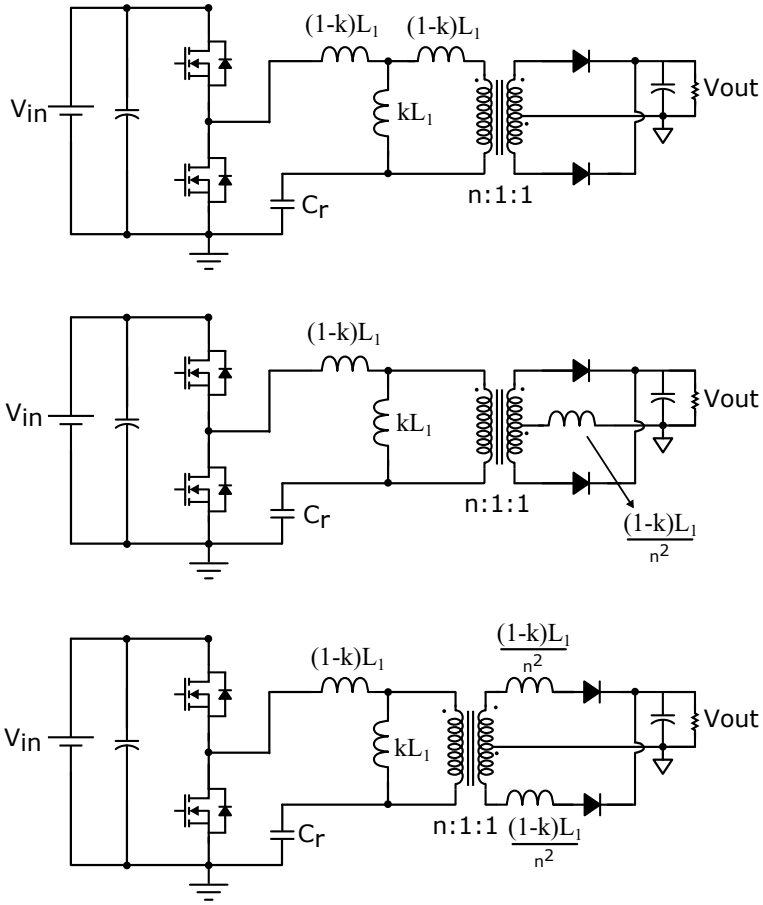


Figure 1-17. LLC T-type Equivalent Models

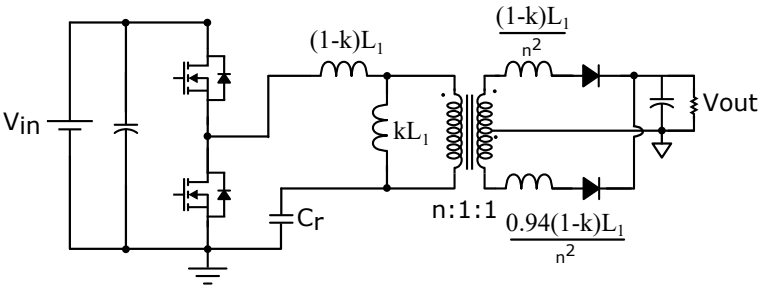


Figure 1-18. LLC Transformer With Unequal Coupling

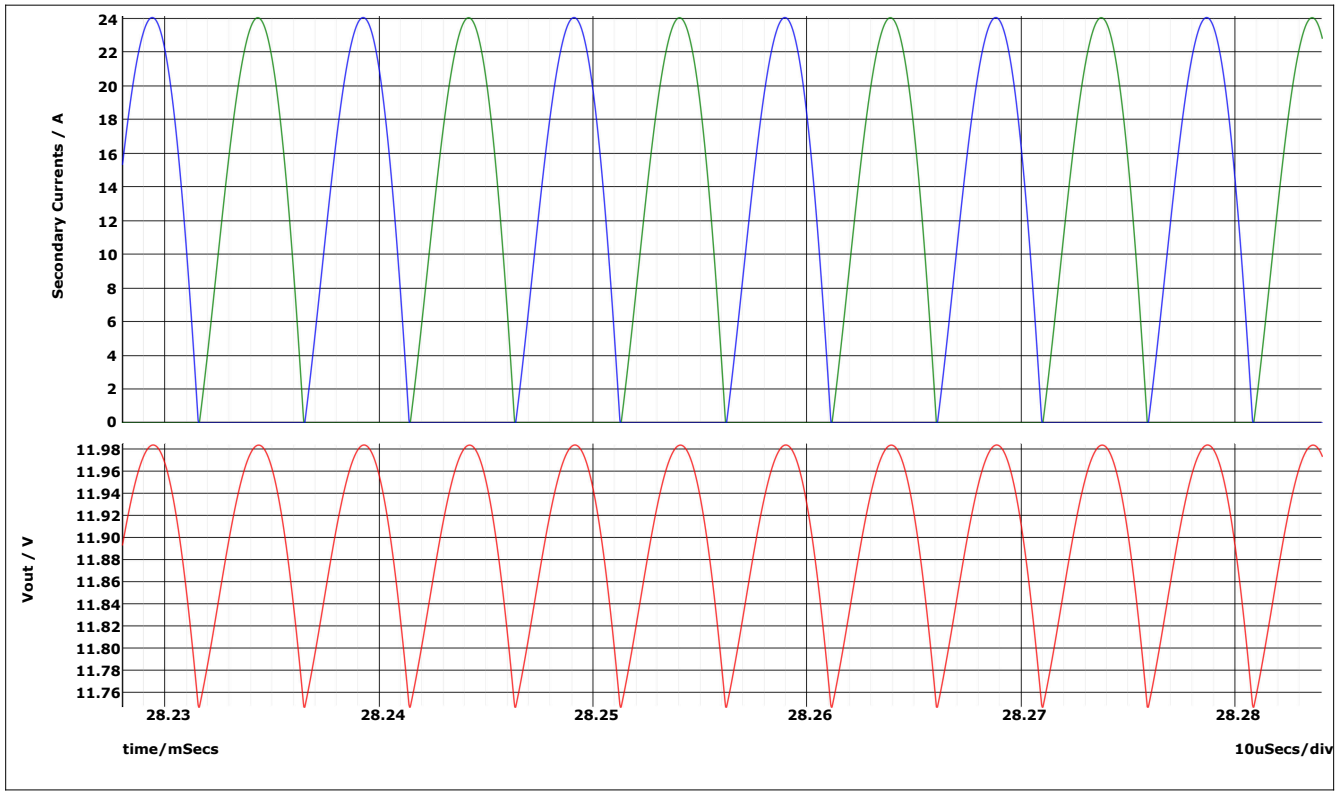


Figure 1-19. Case 1 Simulation Results

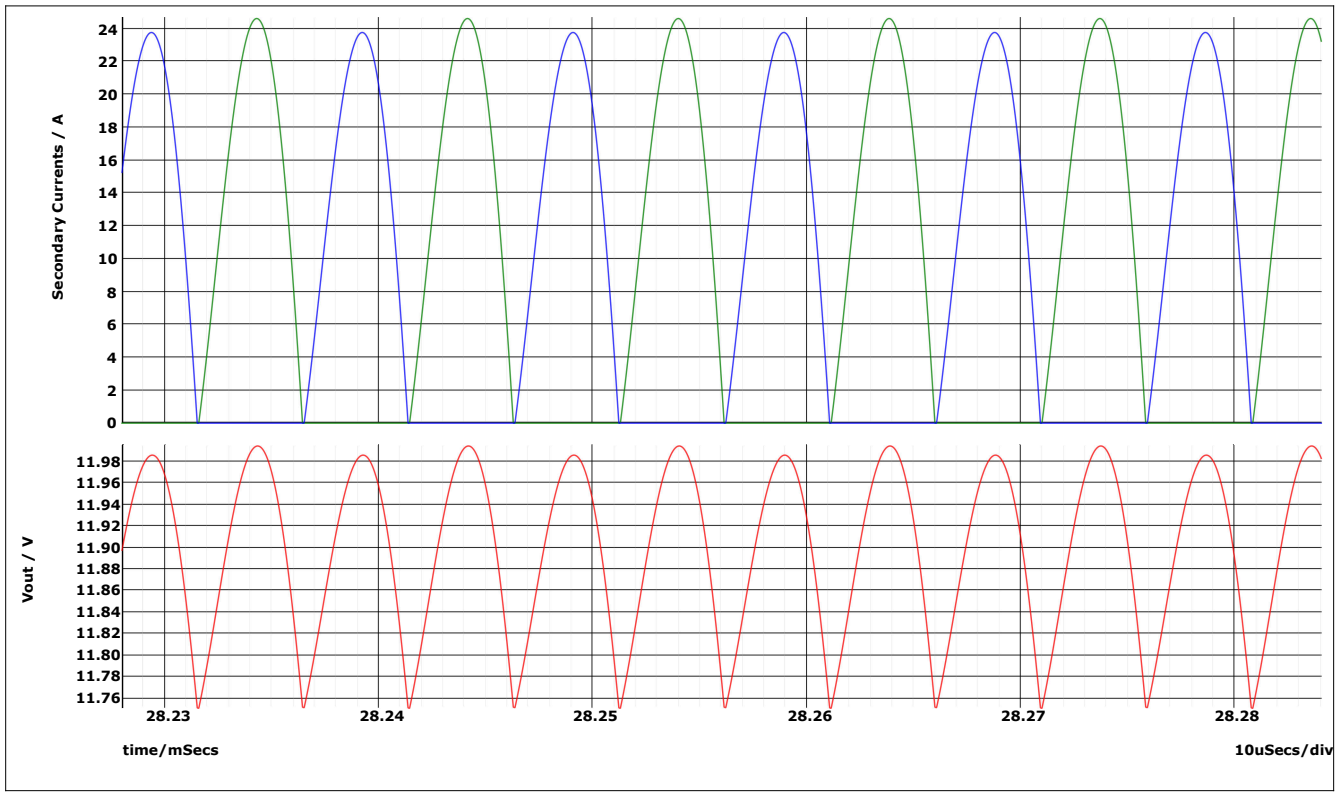


Figure 1-20. Case 2 Simulation Results

1.11 How to Design TL431 Compensator for LLC With UCC25640x Controller

1.11.1 LLC Plant Transfer Function Under HHC Control

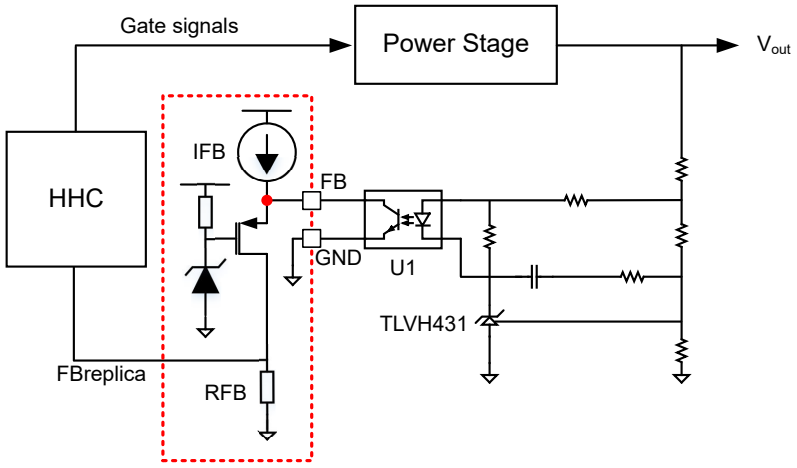


Figure 1-21. Feedback Chain Block Diagram

Reference [8] derives LLC plant transfer function$\left(\frac{V_{out}(s)}{FBreplica(s)}\right)$ when it is operated under Hybrid Hysteretic Control. Simplis tool can also be used to extract these transfer functions. This method is used here.

UCC25640x EVM Power stage [3] is considered for extracting the gain plots when it is operated under different input voltage and load conditions. In Figure 1-22, we can observe that plant gain plot is close to a single pole response in the low frequency region. A Type 2 compensator (zero of the compensator needs to be located below low frequency pole of the plant) can be sufficient for secondary output voltage or current regulation. Here low frequency pole is approximately located at $f_p = \frac{1}{\pi R_L \cdot C_{out}}$ where R_L is load resistance and C_{out} is output capacitance. If the cross over frequency needs to be improved, then Type 3 compensator is recommended as at higher frequency regions plant transfer function has double poles which can degrade the phase [8].

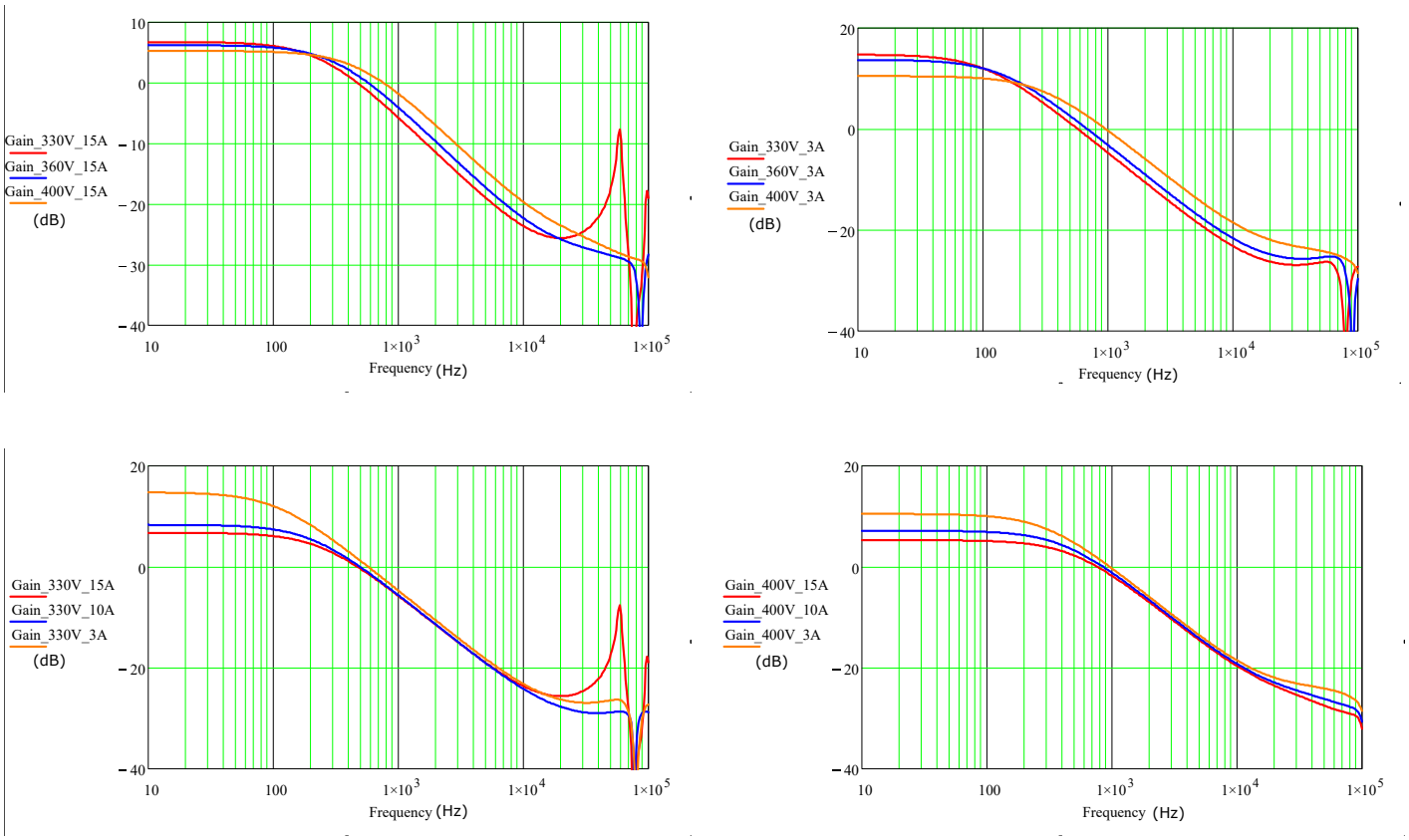


Figure 1-22. Gain Plots Under Different Input Voltage and Load Conditions

1.11.2 Type 2 and Type 3 Compensator with TL431[20]

1.11.2.1 Type 2 Compensator

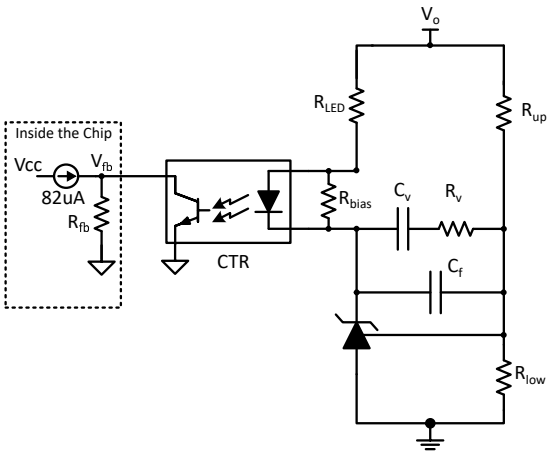


Figure 1-23. Type 2 Compensator with Fast Lane

$$G_c(s) = \left|\frac{V_{fb}(s)}{V_o(s)}\right| = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{\left(C_v + C_f\right)\cdot R_{up}}\frac{1 + R_vC_vs}{\left(1 + \frac{sR_vC_vC_f}{C_v + C_f}\right)s} + 1\right) \quad (39)$$

Assuming $C_f << C_v$, $G_c(s)$ further simplifies to

$$G_c(s) = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{C_v \cdot R_{up}}\frac{1+R_vC_vs}{\left(1+sR_vC_f\right)s}+1\right) \quad (40)$$

This can be written as $G_c(s) = G_o\left(\frac{\frac{\omega_L}{s}+1}{1+\frac{s}{\omega_{p1}}}\right)$ (41)

where $G_o = \frac{R_{fb}CTR}{R_{LED}}\left(1+\frac{R_v}{R_{up}}\right)$ $\omega_L = \frac{1}{\left(R_v+R_{up}\right)\cdot C_v}$ $\omega_{p1} = \frac{1}{R_v \cdot C_f}$ (42)

Here ω_L is low frequency inverted zero and ω_{p1} is a high frequency pole, CTR is current transfer ratio of optocoupler.

Note

- During the full load to light load transition, the current through the optocoupler LED needs to be able to vary more than I_{fb}/CTR to regulate the output voltage. Here I_{fb} is maximum current provided by the FB pin. So, $R_{LED} \leq \frac{V_o - V_{ref} - V_{LED}}{\left(I_{fb}/CTR\right)}$ where V_{ref} and V_{LED} are reference pin voltage and optocoupler LED drop when the current is conducing.
- The shunt regulator starts sinking current only when reference pin voltage reaches the V_{ref}. During startup, make sure that the voltage appeared across the shunt regulator does not exceeds the absolute maximum cathode to anode voltage. Otherwise, the voltage can be destroyed. In cases where LLC output voltage is higher than abs max of shunt regulators, Type 2 compensator without fast lane is recommended. Here Zener diode is used in the fast lane to clamp the voltage.

1.11.2.2 Type 2 Compensator Without Fast Lane

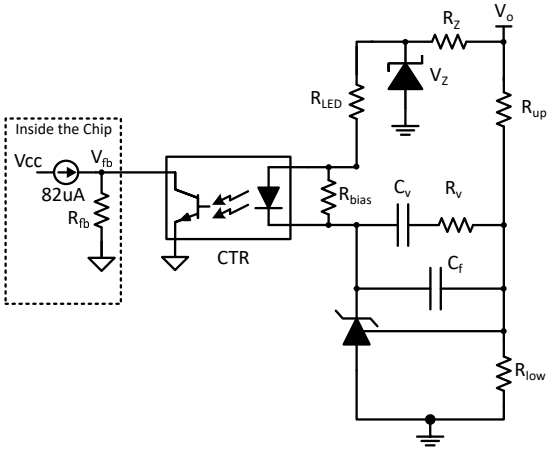


Figure 1-24. Type 2 Compensator Without Fast Lane

$$G_c(s) = \left|\frac{V_{fb}(s)}{V_o(s)}\right| = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{\left(C_v+C_f\right)\cdot R_{up}}\frac{1+R_vC_vs}{\left(1+\frac{sR_vC_vC_f}{C_v+C_f}\right)s}\right) \quad (43)$$

Assuming $C_f << C_v$, $G_c(s)$ further simplifies to

$$G_c(s) = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{C_v \cdot R_{up}}\frac{1+R_vC_vs}{\left(1+sR_vC_f\right)s}\right) \quad (44)$$

This can be written as $G_c(s) = G_o\left(\frac{\frac{\omega_L}{s}+1}{1+\frac{s}{\omega_{p1}}}\right)$ (45)

where $G_o = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{R_v}{R_{up}}\right)$ $\omega_L = \frac{1}{R_v \cdot C_v}$ $\omega_{p1} = \frac{1}{R_v \cdot C_f}$ (46)

Here ω_L is low frequency inverted zero and ω_{p1} is a high frequency pole.

1.11.2.3 Type 3 Compensator with Fast Lane

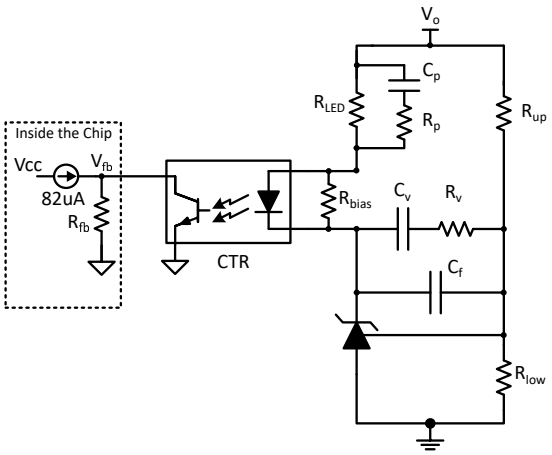


Figure 1-25. Type 3 Compensator with Fast Lane

$$G_c(s) = \left|\frac{V_{fb}(s)}{V_o(s)}\right| = R_{fb}CTR\left(\frac{1}{\left(C_v+C_f\right)\cdot R_{up}}\frac{1+R_vC_vs}{\left(1+\frac{sR_vC_vC_f}{C_v+C_f}\right)s}+1\right)\left(\frac{1+sC_p\left(R_{LED}+R_p\right)}{R_{LED}\left(1+R_pC_ps\right)}\right) \quad (47)$$

Assuming $C_f << C_v$, $G_c(s)$ further simplifies to

$$G_c(s) = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{C_v\cdot R_{up}}\frac{1+R_vC_vs}{\left(1+sR_vC_f\right)s}+1\right)\left(\frac{1+sC_p\left(R_{LED}+R_p\right)}{1+R_pC_ps}\right) \quad (48)$$

This can be written as $G_c(s) = G_o\left(\frac{\frac{\omega_L}{s}+1}{1+\frac{s}{\omega_{p1}}}\right)\left(\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_{p2}}}\right)$ (49)

where $G_o = \frac{R_{fb}CTR}{R_{LED}}\left(1+\frac{R_v}{R_{up}}\right)$ $\omega_L = \frac{1}{\left(R_v+R_{up}\right)\cdot C_v}$ $\omega_{p1} = \frac{1}{R_v\cdot C_f}$

$\omega_z = \frac{1}{\left(R_{LED}+R_p\right)\cdot C_p}$ $\omega_{p2} = \frac{1}{R_p\cdot C_p}$ (50)

Here assuming $\omega_L \ll \omega_z \ll \omega_c \ll \omega_{p2} \ll \omega_{p1}$, ω_z and ω_{p2} creates the phase lead whereas ω_L implements the integrator to reduce the steady state error, and ω_{p1} eliminates the effect of high frequency noise on the control loop. Here ω_c is cross over frequency.

1.11.2.4 Type 3 Compensator Without Fast Lane

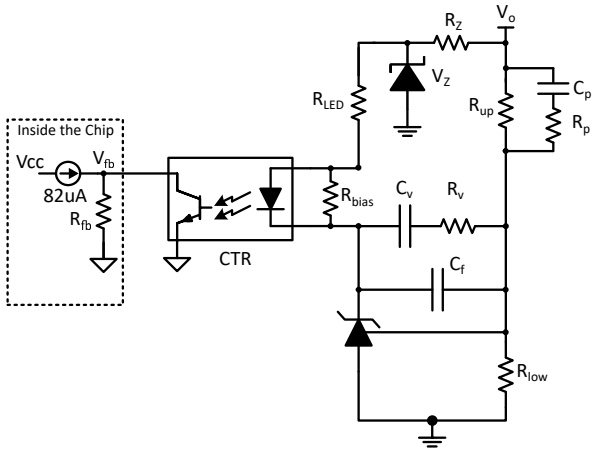


Figure 1-26. Type 3 Compensator Without Fast Lane

$$G_c(s) = \left|\frac{V_{fb}(s)}{V_o(s)}\right| = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{(C_v + C_f)}\frac{1 + R_vC_vs}{\left(1 + \frac{sR_vC_vC_f}{C_v + C_f}\right)s}\right)\left(\frac{1 + sC_p(R_{up} + R_p)}{R_{up}(1 + R_pC_ps)}\right) \quad (51)$$

Assuming $C_f << C_v$, $G_c(s)$ further simplifies to

$$G_c(s) = \frac{R_{fb}CTR}{R_{LED}R_{up}}\left(\frac{1}{C_v}\frac{1 + R_vC_vs}{(1 + sR_vC_f)s}\right)\left(\frac{1 + sC_p(R_{up} + R_p)}{1 + R_pC_ps}\right) \quad (52)$$

$$\text{This can be written as } G_c(s) = G_o\left(\frac{\frac{\omega_L}{s} + 1}{1 + \frac{s}{\omega_{p1}}}\right)\left(\frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_{p2}}}\right) \quad (53)$$

$$\text{where } G_o = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{R_v}{R_{up}}\right) \quad \omega_L = \frac{1}{R_v \cdot C_v} \quad \omega_{p1} = \frac{1}{R_v \cdot C_f}$$
$$\omega_z = \frac{1}{(R_{up} + R_p) \cdot C_p} \quad \omega_{p2} = \frac{1}{R_p \cdot C_p} \quad (54)$$

Here assuming $\omega_L \ll \omega_z \ll \omega_c \ll \omega_{p2} \ll \omega_{p1}$, ω_z and ω_{p2} creates the phase lead whereas ω_L implements the integrator to reduce the steady state error, and ω_{p1} eliminates the effect of high frequency noise on the control loop. Here ω_c is cross over frequency.

1.11.3 Type 3 Compensator Design Example

The power stage of the UCC25640x EVM [3] is considered to demonstrate the Type 3 compensator [1.12.2.3] design which is shown in Figure 1-27. Lets consider 10kHz as a cross over frequency (f_c) for the loop gain.

1. From Figure 1-22, the open loop gain $\left(G_{plant}(s) = \frac{V_{out}(s)}{FBreplica(s)}\right)$ is close to -25dB at 10kHz.
2. So $G_c(s)$ should be 25dB at the cross over frequency.
3. Assuming $f_L \ll f_z \ll f_c \ll f_{p2} \ll f_{p1}$ in [1.12.2.3], $G_c(s)$ can be approximated as $G_o \cdot \frac{f_c}{f_z}$. For a given phase lead (θ), cross over frequency (f_c), f_z, f_{p2} can be found out using following equations [Chapter 9.5 in Reference 9]: $f_c = \sqrt{f_z \cdot f_{p2}}$, $f_z = f_c\sqrt{\frac{1 - \sin(\theta)}{1 + \sin(\theta)}}$, $f_{p2} = f_c\sqrt{\frac{1 + \sin(\theta)}{1 - \sin(\theta)}}$. So, $G_c(s) \cong G_o \cdot \frac{f_c}{f_z} = G_o \cdot \frac{\sqrt{f_z \cdot f_{p2}}}{f_z} = G_o \cdot \sqrt{\frac{f_{p2}}{f_z}}$.

4. For a phase lead of 52°, f_z and f_{p2} should be 3.4kHz and 29kHz respectively.
5. Since f_z, f_{p2} are found out, G_o can be obtained using following expression: $G_o \cdot \sqrt{\frac{f_{p2}}{f_z}} = 17.78 \Rightarrow G_o = 6.126$ (25dB=17.78).
6. f_{p1} is a high frequency pole which is used to eliminate the high frequency noise. It is recommended to place this pole close to ESR of the output capacitor. Here f_{p1} is chosen as 479kHz.
7. f_L should be chosen such that controller should be able to regulate the output voltage when the converter operates in the burst mode. So, f_L should be less than the burst mode frequency. In this design, f_L is considered as 88Hz.
8. Rup and Rlow can be found out using following expressions: $\frac{V_o - V_{ref}}{R_{up}} = I_{ref} + \frac{V_{ref}}{R_{low}}$ where V_o is output voltage and V_{ref}, I_{ref} are reference voltage and bias current through the reference pin of the shunt regulator. To make V_o independent of the I_{ref}, the I_{ref} should be much lower than $\frac{V_o - V_{ref}}{R_{up}}$. So, $\frac{V_o - V_{ref}}{R_{up}} = \frac{V_{ref}}{R_{low}}$. In the EVM, TLVH431 is considered for which reference voltage is given as 1.24V. For this design, $\frac{V_o - V_{ref}}{R_{up}}$ is considered as 73uA. So R_{up} obtained as 147kOhm. And from $\frac{V_o - V_{ref}}{R_{up}} = \frac{V_{ref}}{R_{low}}$, R_{low} obtained as 16.98kohm.
9. Consider C_f as 10pF. So, R_v can be obtained as
   $\omega_{p1} = \frac{1}{R_v \cdot C_f} \Rightarrow f_{p1} = \frac{1}{2 \cdot \pi \cdot R_v \cdot C_f} \Rightarrow R_v = \frac{1}{2 \cdot \pi \cdot 479kHz \cdot C_f} \Rightarrow R_v = 33.2kohm$
10. R_{LED} can be obtained as
    $G_o = \frac{R_{fb} CTR}{R_{LED}}\left(1 + \frac{R_v}{R_{up}}\right) \Rightarrow R_{LED} = \frac{R_{fb} CTR}{G_o}\left(1 + \frac{R_v}{R_{up}}\right) \Rightarrow R_{LED} = \frac{100 \cdot 10^3 \cdot 0.2}{6.126}\left(1 + \frac{33.2k}{147k}\right) \Rightarrow R_{LED} = 4kohm$
11. C_v can be obtained as
    $\omega_L = \frac{1}{(R_v + R_{up}) \cdot C_v} \Rightarrow C_v = \frac{1}{2 \cdot \pi \cdot f_L \cdot (R_v + R_{up})} \Rightarrow C_v = \frac{1}{2 \cdot \pi \cdot 88 \cdot (33.2k + 147k)} \Rightarrow C_v = 10nF$
12. C_p, R_p are obtained as
    $\omega_z = \frac{1}{(R_{LED} + R_p) \cdot C_p}$, $\omega_{p2} = \frac{1}{R_p \cdot C_p} \Rightarrow f_z = \frac{1}{2 \cdot \pi \cdot (R_{LED} + R_p) \cdot C_p}$, $f_{p2} = \frac{1}{2 \cdot \pi \cdot R_p \cdot C_p}$
    $\Rightarrow 3.4kHz = \frac{1}{2 \cdot \pi \cdot (R_{LED} + R_p) \cdot C_p}$, $29\text{kHz} = \frac{1}{2 \cdot \pi \cdot R_p \cdot C_p} \Rightarrow C_p = 10nF$, $R_p = 540ohm$.
13. R_{bias} is used to bias the shunt regulator. R_{bias} is obtained as $R_{bias} = \frac{V_{opto}}{I_{bias}} = \frac{1V}{1mA} = 1kohm$.

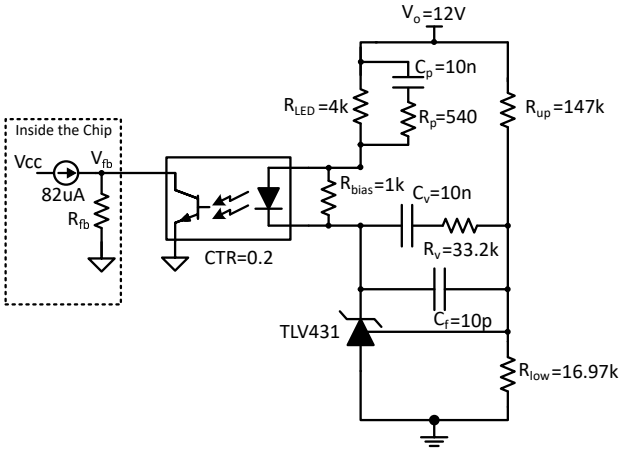


Figure 1-27. Type 3 Compensator

1.12 How to Design LLC for Battery Charging and LED Driver Applications?

The battery chargers and LED drivers exhibits different effective output resistance variation with the change in their output voltages (*Implementation of Wide Output LLC for Chargers and LED Drivers Applications*). In case of battery chargers, the effective output resistance increases with the output voltage whereas in case of LED drivers, the voltage can be reduced. When LLC is designed in these applications, we need to make sure required voltage gains are met.

1.12.1 LED Driver Design Example

Table 1-2. 160W LED Driver Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
DC voltage range (V_{in})		365	390	410	V
LED CHARACTERISTICS[10]					
Forward Voltage at I_F=1 A		2.8	3.2	3.8	V
Rated Forward Current (I_F)			1		A
Forward Voltage at I_F=100 mA			2.8		V
OUTPUT CHARACTERISTICS [11]					
LED Array Voltage (V_{out}) (Array consists of three branches and each branch has 14 LEDs)		39.2	44.8	53.2	V
LED Array Current		0.3 (100mA per branch)		3	A
Output Power at LED array current = 3 A		117.6	134.4 (P_{out_typ})	159.6 (P_{out_Max})	W
Output Power at LED array current = 0.3 A (P_{out_Min})			11.76		W
Output Voltage Ripple				300	mVpp
Output Voltage at No Load				57	V
Resonant frequency f_{res}			100		kHz
Peak efficiency	At Peak output Power		92%		

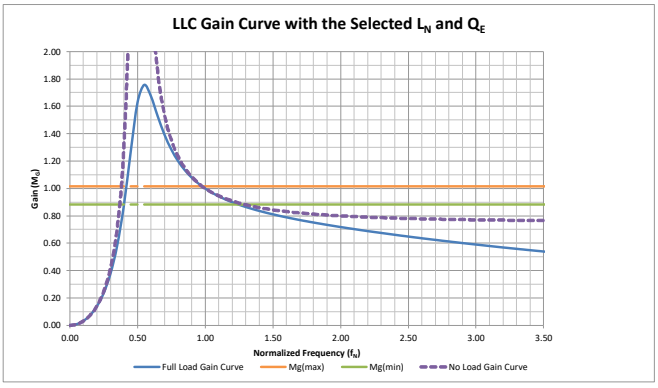
1. The LLC tank parameters and the turns ratio are chosen based on the $V_{in\_typ} = 390V$, $V_{out\_typ} = 44.8V$, $P_{out\_typ} = 134.4W$, $f_{res} = 100kHz$. This is shown in Figure 1-28 [12].
2. It is important to make sure that the maximum and minimum gain requirements are met once the tank parameters have been chosen.
3. Maximum Gain and Minimum frequency $\left(G_{max}=\frac{V_{out_Max}}{V_{in_Min}}\right)$requirement occurs at P_{out_Max}

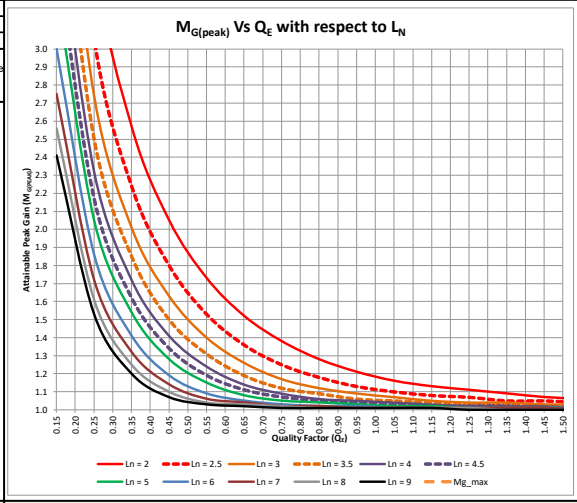
   Where as Minimum Gain and Maximum frequency $\left(G_{min}=\frac{V_{out_Min}}{V_{in_Max}}\right)$requirement occurs at P_{out_Min} . These are shown in Figure 1-29 and Figure 1-30.
4. To protect the converter against the over voltage during no load, output voltage is regulated at 57 V.

Select Which Device You Are Using		UCC256404		Refer datasheet for the difference of UCC25640x devices
%				
OUTPUT				
Output Voltage	V_{OUT}	44.8	V	Enter required nominal output voltage of converter
Maximum Output Power	P_{OUT}	134.4	W	Enter required maximum converter output power in Watts
Full Load Output Current	I_{OUT}	3	A	
Maximum Output Voltage Ripple	$V_{OUT(pk-pk)}$	300	mV	Enter the desired maximum output voltage ripple
Target Efficiency	η	0.92		Enter the Overall Efficiency here
%				
INPUT				
Nominal Input Voltage	V_{BLK}	390	V	Enter the nominal input voltage
Maximum DC Input Voltage	$V_{BLK(max)}$	410	V	Enter the maximum input voltage
Minimum DC Input Voltage	$V_{BLK(hu)}$	365	V	Enter the minimum input voltage

LLC STAGE				
Nominal LLC Switching Frequency	f_{LLC}	100	kHz	Enter desired nominal LLC switching frequency
LLC Transformer				
Recommended Primary/Secondary Turns Ratio	$N_{PS(recommended)}$	4.352678571		
Actual Primary/Secondary Turns Ratio	N_{PS}	4.00		Enter Actual Primary/Secondary Turns Ratio
Recommended Primary/Bias Turns Ratio	$N_{PB(recommended)}$	13.00		
Actual Primary/Bias Turns Ratio	N_{PB}	13.00		Enter Actual Primary/Bias Turns Ratio
LLC Effective Load Resistance at 110% Full Load	R_E	176.1	Ω	
LLC Effective Load Resistance at Full Load	$R_{E(full\ load)}$	193.7	Ω	
LLC Gain Range				
Minimum LLC Gain	$M_{G(min)}$	**0.884**		
Maximum LLC Gain Including Losses	$M_{G(max)}$	**1.015**		
Predicted Voltage Drop Due to Losses	V_{LOSS}	1.000	V	Enter the predicted voltage drop due to conversion losses in circuit
Select L_N and Q_E				
From the figure on the right, $M_{G(peak)}$ Vs Q_E with respect to L_N, select a point on an Ln curve that has an Ln and Qe point that corresponds to an Attainable $M_{G(PEAK)}$ value that is greater than $M_{G(max)}$. Enter the selected values in the L_N and Q_E cells below.				
For example, if $M_{G(max)}$, calculated above and shown by the horizontal line, was calculated to be 1.4, then using Ln = 5 and Qe 0.35 would result in an attainable $M_{G(PEAK)}$ = 1.52 (interpolated from Ln = 5 curve) which satisfies the requirement that the Attainable $M_{G(PEAK)} > M_{G(max)}$				
Selected Primary Inductance Ratio	$L_{N(selected)}$	3.00		
Selected Quality Factor for Resonant Network	$Q_{E(selected)}$	0.41		
Gain Required at No-Load	$M_{G(noload)}$	0.750		
f_N at Maximum Switching Frequency	$f_{N(max)}$	3.50		

The selected L_N and Q_E values should result in an LLC Gain Curve, shown below, that intersects with the $M_{G(min)}$ and $M_{G(max)}$ traces. The Gain curve from an overload condition is also plotted, showing the minimum gain at maximum frequency.

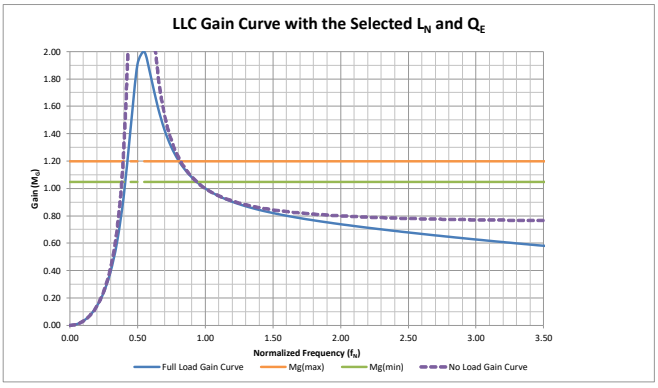




Parameters of the LLC Resonant Circuit				
Discrete resonant inductor or transformer leakage inductance used for L_R?		Discrete Inductor		
		0.9		Ignore this row
Recommended Resonant Capacitor Value	CR(recommended)	0.020	uF	
Actual Total Value of Resonant Capacitor Used	CR	0.02	uF	Enter actual value of Resonant Capacitor used
Recommended Resonant Inductor Value	LR(recommended)	126.651	uH	
Actual Resonant Inductor Value Used	LR	126	uH	Enter the actual value of the Resonant Inductor Value used
Recommended Transformer Magnetizing Inductance	LM(recommended)	378	uH	
Actual Transformer Magnetizing Inductance Used	LM	378	uH	Enter the actual value of the magnetizing inductance value used
Resultant Series Resonant Frequency	f_0	100.3	kHz	
No Load Resonant Frequency	f_P	50.1	kHz	
Resultant Inductance Ratio	L_N	**3.00**		Re-enter this value in the LN(selected) cell above to see the actual normalized frequency at MG(max) and MG(min)
Resultant Quality Factor at Full Load	Q_E	**0.41**		Re-enter this value in the $Q_{E(selected)}$ cell above to see the actual normalized frequency at $M_{G(max)}$ and $M_{G(min)}$
Gain Curve Graph Up to Date?		Yes		
f_N at $M_{G(max)}$	$f_{N(Mg\_max)}$	1		Enter f_N value at the second intersection of the $M_{G(max)}$ line and LLC Gain Curve shown in figure above
f_N at $M_{G(min)}$	$f_{N(Mg\_min)}$	1.3		Enter f_N value at the second intersection of the $M_{G(min)}$ line and LLC Gain Curve shown in figure above
Maximum Switching Frequency	$f_{SW(max)}$	130.3	kHz	
Minimum Switching Frequency	$f_{SW(min)}$	100.3	kHz	

Figure 1-28. LLC Design for Typical Output Voltage of the LED Driver and at Typical Output Power

Select Which Device You Are Using		UCC256404		Refer datasheet for the difference of UCC25640x devices
%				
OUTPUT				
Output Voltage	V_{OUT}	53.2	V	Enter required nominal output voltage of converter
Maximum Output Power	P_{OUT}	160	W	Enter required maximum converter output power in Watts
Full Load Output Current	I_{OUT}	3.007518797	A	
Maximum Output Voltage Ripple	$V_{OUT(pk-pk)}$	300	mV	Enter the desired maximum output voltage ripple
Target Efficiency	η	0.92		Enter the Overall Efficiency here
%				
INPUT				
Nominal Input Voltage	V_{BLK}	390	V	Enter the nominal input voltage
Maximum DC Input Voltage	$V_{BLK(max)}$	410	V	Enter the maximum input voltage
Minimum DC Input Voltage	$V_{BLK(hu)}$	365	V	Enter the minimum input voltage
LLC STAGE				
Nominal LLC Switching Frequency	f_{LLC}	100	kHz	Enter desired nominal LLC switching frequency
LLC Transformer				
Recommended Primary/Secondary Turns Ratio	$N_{PS(recommended)}$	3.665413534		
Actual Primary/Secondary Turns Ratio	N_{PS}	4.00		Enter Actual Primary/Secondary Turns Ratio
Recommended Primary/Bias Turns Ratio	$N_{PB(recommended)}$	13.00		
Actual Primary/Bias Turns Ratio	N_{PB}	13.00		Enter Actual Primary/Bias Turns Ratio
LLC Effective Load Resistance at 110% Full Load	R_E	208.6	Ω	
LLC Effective Load Resistance at Full Load	$R_{E(full\ load)}$	229.4	Ω	
LLC Gain Range				
Minimum LLC Gain	$M_{G(min)}$	**1.048**		
Maximum LLC Gain Including Losses	$M_{G(max)}$	**1.199**		
Predicted Voltage Drop Due to Losses	V_{LOSS}	1.000	V	Enter the predicted voltage drop due to conversion losses in circuit
Select L_N and Q_E				
From the figure on the right, $M_{G(peak)}$ Vs Q_E with respect to L_N, select a point on an Ln curve that has an Ln and Qe point that corresponds to an Attainable $M_{G(PEAK)}$ value that is greater than $M_{G(max)}$. Enter the selected values in the L_N and Q_E cells below.				
For example, if $M_{G(max)}$, calculated above and shown by the horizontal line, was calculated to be 1.4, then using Ln = 5 and Qe 0.35 would result in an attainable $M_{G(PEAK)}$ = 1.52 (interpolated from Ln = 5 curve) which satisfies the requirement that the Attainable $M_{G(PEAK)} > M_{G(max)}$				
Selected Primary Inductance Ratio	$L_{N(selected)}$	3.00		
Selected Quality Factor for Resonant Network	$Q_{E(selected)}$	0.35		
Gain Required at No-Load	$M_{G(noload)}$	0.750		
f_N at Maximum Switching Frequency	$f_{N(max)}$	3.50		
The selected L_N and Q_E values should result in an LLC Gain Curve, shown below, that intersects with the $M_{G(min)}$ and $M_{G(max)}$ traces. The Gain curve from an overload condition is also plotted, showing the minimum gain at maximum frequency.				
Parameters of the LLC Resonant Circuit				
Discrete resonant inductor or transformer leakage inductance used for L_r?		Discrete Inductor		
		0.9		Ignore this row
Recommended Resonant Capacitor Value	CR(recommended)	0.020	uF	
Actual Total Value of Resonant Capacitor Used	CR	0.02	uF	Enter actual value of Resonant Capacitor used
Recommended Resonant Inductor Value	LR(recommended)	126.651	uH	
Actual Resonant Inductor Value Used	LR	126	uH	Enter the actual value of the Resonant Inductor Value used
Recommended Transformer Magnetizing Inductance	LM(recommended)	378	uH	
Actual Transformer Magnetizing Inductance Used	LM	378	uH	Enter the actual value of the magnetizing inductance value used
Resultant Series Resonant Frequency	f_0	100.3	kHz	
No Load Resonant Frequency	f_P	50.1	kHz	
Resultant Inductance Ratio	L_N	**3.00**		Re-enter this value in the LN(selected) cell above to see the actual normalized frequency at MG(max) and MG(min)
Resultant Quality Factor at Full Load	Q_E	**0.35**		Re-enter this value in the $Q_{E(selected)}$ cell above to see the actual normalized frequency at $M_{G(max)}$ and $M_{G(min)}$
Gain Curve Graph Up to Date?		Yes		
f_N at $M_{G(max)}$	$f_{N(Mg\_max)}$	0.85		Enter f_N value at the second intersection of the $M_{G(max)}$ line and LLC Gain Curve shown in figure above
f_N at $M_{G(min)}$	$f_{N(Mg\_min)}$	0.95		Enter f_N value at the second intersection of the $M_{G(min)}$ line and LLC Gain Curve shown in figure above
Maximum Switching Frequency	$f_{SW(max)}$	95.2	kHz	
Minimum Switching Frequency	$f_{SW(min)}$	85.2	kHz	



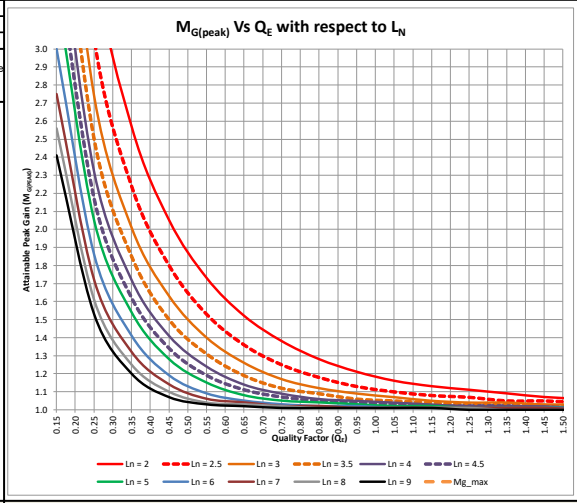
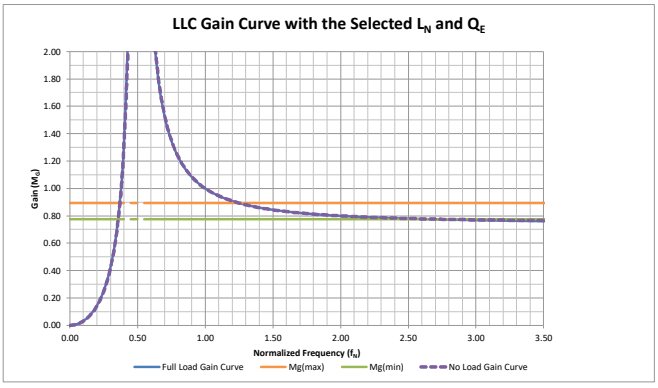
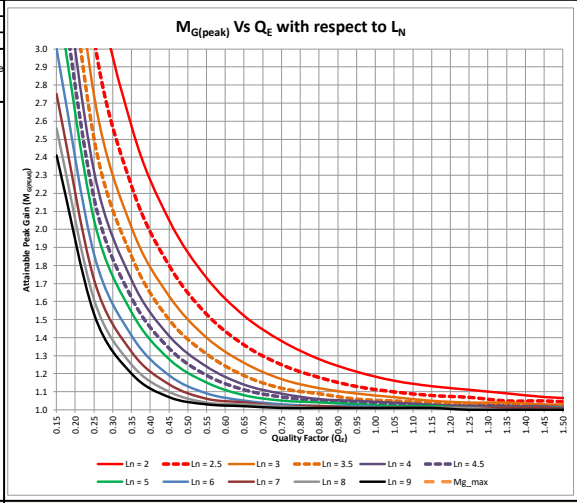


Figure 1-29. LLC Maximum Gain Verification at Maximum Output Power

Select Which Device You Are Using		UCC256404		Refer datasheet for the difference of UCC25640x devices
%				
OUTPUT				
Output Voltage	V_{OUT}	39.2	V	Enter required nominal output voltage of converter
Maximum Output Power	P_{OUT}	11.7	W	Enter required maximum converter output power in Watts
Full Load Output Current	I_{OUT}	0.298469388	A	
Maximum Output Voltage Ripple	$V_{OUT(pk-pk)}$	300	mV	Enter the desired maximum output voltage ripple
Target Efficiency	η	0.92		Enter the Overall Efficiency here
%				
INPUT				
Nominal Input Voltage	V_{BLK}	390	V	Enter the nominal input voltage
Maximum DC Input Voltage	$V_{BLK(max)}$	410	V	Enter the maximum input voltage
Minimum DC Input Voltage	$V_{BLK(hu)}$	365	V	Enter the minimum input voltage

LLC STAGE				
Nominal LLC Switching Frequency	f_{LLC}	100	kHz	Enter desired nominal LLC switching frequency
LLC Transformer				
Recommended Primary/Secondary Turns Ratio	$N_{PS(recommended)}$	4.974489796		
Actual Primary/Secondary Turns Ratio	N_{PS}	4.00		Enter Actual Primary/Secondary Turns Ratio
Recommended Primary/Bias Turns Ratio	$N_{PB(recommended)}$	13.00		
Actual Primary/Bias Turns Ratio	N_{PB}	13.00		Enter Actual Primary/Bias Turns Ratio
LLC Effective Load Resistance at 110% Full Load	R_E	1548.5	Ω	
LLC Effective Load Resistance at Full Load	$R_{E(full\ load)}$	1703.3	Ω	
LLC Gain Range				
Minimum LLC Gain	$M_{G(min)}$	**0.775**		
Maximum LLC Gain Including Losses	$M_{G(max)}$	**0.892**		
Predicted Voltage Drop Due to Losses	V_{LOSS}	1.000	V	Enter the predicted voltage drop due to conversion losses in circuit
Select L_N and Q_E				
From the figure on the right, $M_{G(peak)}$ Vs Q_E with respect to L_N, select a point on an Ln curve that has an Ln and Qe point that corresponds to an Attainable $M_{G(PEAK)}$ value that is greater than $M_{G(max)}$. Enter the selected values in the L_N and Q_E cells below.				
For example, if $M_{G(max)}$, calculated above and shown by the horizontal line, was calculated to be 1.4, then using Ln = 5 and Qe 0.35 would result in an attainable $M_{G(PEAK)}$ = 1.52 (interpolated from Ln = 5 curve) which satisfies the requirement that the Attainable $M_{G(PEAK)} > M_{G(max)}$				
Selected Primary Inductance Ratio	$L_{N(selected)}$	3.00		
Selected Quality Factor for Resonant Network	$Q_{E(selected)}$	0.05		
Gain Required at No-Load	$M_{G(noload)}$	0.750		
f_N at Maximum Switching Frequency	$f_{N(max)}$	3.50		
The selected L_N and Q_E values should result in an LLC Gain Curve, shown below, that intersects with the $M_{G(min)}$ and $M_{G(max)}$ traces. The Gain curve from an overload condition is also plotted, showing the minimum gain at maximum frequency.				





Parameters of the LLC Resonant Circuit				
Discrete resonant inductor or transformer leakage inductance used for L_r?		Discrete Inductor		
		0.9		Ignore this row
Recommended Resonant Capacitor Value	CR(recommended)	0.019	uF	
Actual Total Value of Resonant Capacitor Used	CR	0.02	uF	Enter actual value of Resonant Capacitor used
Recommended Resonant Inductor Value	LR(recommended)	126.651	uH	
Actual Resonant Inductor Value Used	LR	126	uH	Enter the actual value of the Resonant Inductor Value used
Recommended Transformer Magnetizing Inductance	LM(recommended)	378	uH	
Actual Transformer Magnetizing Inductance Used	LM	378	uH	Enter the actual value of the magnetizing inductance value used
Resultant Series Resonant Frequency	f_0	100.3	kHz	
No Load Resonant Frequency	f_P	50.1	kHz	
Resultant Inductance Ratio	L_N	**3.00**		Re-enter this value in the LN(selected) cell above to see the actual normalized frequency at MG(max) and MG(min)
Resultant Quality Factor at Full Load	Q_E	**0.05**		Re-enter this value in the $Q_{E(selected)}$ cell above to see the actual normalized frequency at $M_{G(max)}$ and $M_{G(min)}$
Gain Curve Graph Up to Date?		Yes		
f_N at $M_{G(max)}$	$f_{N(Mg\_max)}$	1.3		Enter f_N value at the second intersection of the $M_{G(max)}$ line and LLC Gain Curve shown in figure above
f_N at $M_{G(min)}$	$f_{N(Mg\_min)}$	2.5		Enter f_N value at the second intersection of the $M_{G(min)}$ line and LLC Gain Curve shown in figure above
Maximum Switching Frequency	$f_{SW(max)}$	250.6	kHz	
Minimum Switching Frequency	$f_{SW(min)}$	130.3	kHz	

Figure 1-30. LLC Minimum Gain Verification at Minimum Output Power

1.12.2 Battery Charger Design Example

Table 1-3. 500W Battery Charger Specifications

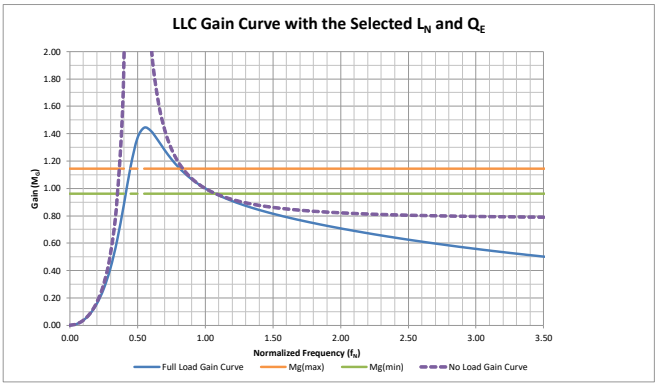
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
DC voltage range (V_{in})		350	390	410	V
OUTPUT CHARACTERISTICS [13]					
Battery Voltage (V_{out}) at constant current charging mode =7A		46.2	58.7	<71.2	V
Battery Charging Current				7	A
Output Power (P_{out}) at Charging current = 7 A		323.4	410.9	498.4	W
Output Voltage Ripple				712	mVpp
Output Voltage at Constant voltage mode				71.2	V
Resonant frequency f_{res}			100		kHz
Peak efficiency	At Peak output Power		92%		

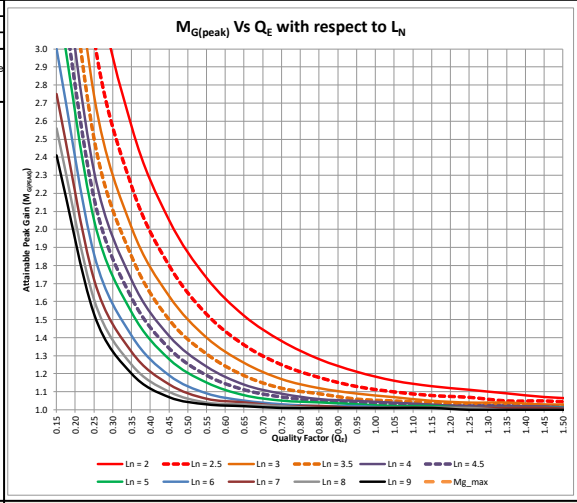
1. The LLC tank parameters and the turns ratio are chosen based on the $V_{in\_typ} = 390V$, $V_{out\_typ} = 58.7V$, $P_{out\_typ} = 410.9W$, $f_{res} = 100kHz$. This is shown in Figure 1-31 [12].
2. It is important to ensure that the maximum and minimum gain requirements are met once the tank parameters have been chosen.
3. Maximum Gain and Minimum frequency $\left(G_{max}=\frac{V_{out_Max}}{V_{in_Min}}\right)$requirement occurs at P_{out_Max}

   Where as Minimum Gain and Maximum frequency $\left(G_{min}=\frac{V_{out_Min}}{V_{in_Max}}\right)$requirement occurs at P_{out_Min} . These are shown in Figure 1-32 and Figure 1-33.

Select Which Device You Are Using		UCC256404		Refer datasheet for the difference of UCC25640x devices
%				
OUTPUT				
Output Voltage	V_{OUT}	58.7	V	Enter required nominal output voltage of converter
Maximum Output Power	P_{OUT}	410.9	W	Enter required maximum converter output power in Watts
Full Load Output Current	I_{OUT}	7	A	
Maximum Output Voltage Ripple	$V_{OUT(pk-pk)}$	587	mV	Enter the desired maximum output voltage ripple
Target Efficiency	η	0.92		Enter the Overall Efficiency here
%				
INPUT				
Nominal Input Voltage	V_{BLK}	390	V	Enter the nominal input voltage
Maximum DC Input Voltage	$V_{BLK(max)}$	410	V	Enter the maximum input voltage
Minimum DC Input Voltage	$V_{BLK(hu)}$	350	V	Enter the minimum input voltage

LLC STAGE				
Nominal LLC Switching Frequency	f_{LLC}	100	kHz	Enter desired nominal LLC switching frequency
LLC Transformer				
Recommended Primary/Secondary Turns Ratio	$N_{PS(recommended)}$	3.3219761		
Actual Primary/Secondary Turns Ratio	N_{PS}	3.33		Enter Actual Primary/Secondary Turns Ratio
Recommended Primary/Bias Turns Ratio	$N_{PB(recommended)}$	13.00		
Actual Primary/Bias Turns Ratio	N_{PB}	11.00		Enter Actual Primary/Bias Turns Ratio
LLC Effective Load Resistance at 110% Full Load	R_E	68.5	Ω	
LLC Effective Load Resistance at Full Load	$R_{E(full load)}$	75.4	Ω	
LLC Gain Range				
Minimum LLC Gain	$M_{G(min)}$	**0.962**		
Maximum LLC Gain Including Losses	$M_{G(max)}$	**1.146**		
Predicted Voltage Drop Due to Losses	V_{LOSS}	1.000	V	Enter the predicted voltage drop due to conversion losses in circuit
Select L_N and Q_E				
From the figure on the right, $M_{G(peak)}$ Vs Q_E with respect to L_N, select a point on an Ln curve that has an Ln and Qe point that corresponds to an Attainable $M_{G(PEAK)}$ value that is greater than $M_{G(max)}$. Enter the selected values in the L_N and Q_E cells below.				
For example, if $M_{G(max)}$, calculated above and shown by the horizontal line, was calculated to be 1.4, then using Ln = 5 and Qe 0.35 would result in an attainable $M_{G(PEAK)}$ = 1.52 (interpolated from Ln = 5 curve) which satisfies the requirement that the Attainable $M_{G(PEAK)} > M_{G(max)}$				
Selected Primary Inductance Ratio	$L_{N(selected)}$	3.45		
Selected Quality Factor for Resonant Network	$Q_{E(selected)}$	0.48		
Gain Required at No-Load	$M_{G(noload)}$	0.775		
f_N at Maximum Switching Frequency	$f_{N(max)}$	3.50		
The selected L_N and Q_E values should result in an LLC Gain Curve, shown below, that intersects with the $M_{G(min)}$ and $M_{G(max)}$ traces. The Gain curve from an overload condition is also plotted, showing the minimum gain at maximum frequency.				



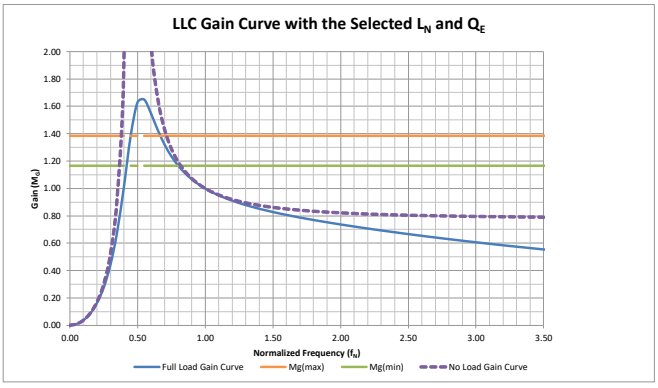


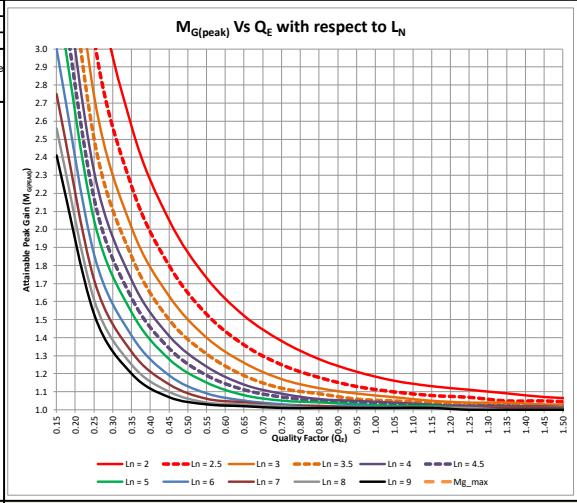
Parameters of the LLC Resonant Circuit				
Discrete resonant inductor or transformer leakage inductance used for L_R?		Discrete Inductor		
		0.9		Ignore this row
Recommended Resonant Capacitor Value	CR(recommended)	0.044	uF	
Actual Total Value of Resonant Capacitor Used	CR	0.044	uF	Enter actual value of Resonant Capacitor used
Recommended Resonant Inductor Value	LR(recommended)	57.569	uH	
Actual Resonant Inductor Value Used	LR	58	uH	Enter the actual value of the Resonant Inductor Value used
Recommended Transformer Magnetizing Inductance	LM(recommended)	200	uH	
Actual Transformer Magnetizing Inductance Used	LM	200	uH	Enter the actual value of the magnetizing inductance value used
Resultant Series Resonant Frequency	f_0	99.6	kHz	
No Load Resonant Frequency	f_P	47.2	kHz	
Resultant Inductance Ratio	L_N	**3.45**		Re-enter this value in the LN(selected) cell above to see the actual normalized frequency at MG(max) and MG(min)
Resultant Quality Factor at Full Load	Q_E	**0.48**		Re-enter this value in the $Q_{E(selected)}$ cell above to see the actual normalized frequency at $M_{G(max)}$ and $M_{G(min)}$
Gain Curve Graph Up to Date?		Yes		
f_N at $M_{G(max)}$	$f_{N(Mg\_max)}$	0.85		Enter f_N value at the second intersection of the $M_{G(max)}$ line and LLC Gain Curve shown in figure above
f_N at $M_{G(min)}$	$f_{N(Mg\_min)}$	1.1		Enter f_N value at the second intersection of the $M_{G(min)}$ line and LLC Gain Curve shown in figure above
Maximum Switching Frequency	$f_{SW(max)}$	109.6	kHz	
Minimum Switching Frequency	$f_{SW(min)}$	84.7	kHz	

Figure 1-31. LLC Design for Battery Charger at Typical Output Voltage, Typical Output Power

Select Which Device You Are Using		UCC256404		Refer datasheet for the difference of UCC25640x devices
%				
OUTPUT				
Output Voltage	V_{OUT}	71.2	V	Enter required nominal output voltage of converter
Maximum Output Power	P_{OUT}	498.4	W	Enter required maximum converter output power in Watts
Full Load Output Current	I_{OUT}	7	A	
Maximum Output Voltage Ripple	$V_{OUT(pk-pk)}$	712	mV	Enter the desired maximum output voltage ripple
Target Efficiency	η	0.92		Enter the Overall Efficiency here
%				
INPUT				
Nominal Input Voltage	V_{BLK}	390	V	Enter the nominal input voltage
Maximum DC Input Voltage	$V_{BLK(max)}$	410	V	Enter the maximum input voltage
Minimum DC Input Voltage	$V_{BLK(hu)}$	350	V	Enter the minimum input voltage

LLC STAGE				
Nominal LLC Switching Frequency	f_{LLC}	100	kHz	Enter desired nominal LLC switching frequency
LLC Transformer				
Recommended Primary/Secondary Turns Ratio	$N_{PS(recommended)}$	2.738764045		
Actual Primary/Secondary Turns Ratio	N_{PS}	3.33		Enter Actual Primary/Secondary Turns Ratio
Recommended Primary/Bias Turns Ratio	$N_{PB(recommended)}$	13.00		
Actual Primary/Bias Turns Ratio	N_{PB}	11.00		Enter Actual Primary/Bias Turns Ratio
LLC Effective Load Resistance at 110% Full Load	R_E	83.1	Ω	
LLC Effective Load Resistance at Full Load	$R_{E(full\ load)}$	91.4	Ω	
LLC Gain Range				
Minimum LLC Gain	$M_{G(min)}$	**1.165**		
Maximum LLC Gain Including Losses	$M_{G(max)}$	**1.383**		
Predicted Voltage Drop Due to Losses	V_{LOSS}	1.000	V	Enter the predicted voltage drop due to conversion losses in circuit
Select L_N and Q_E				
From the figure on the right, $M_{G(peak)}$ Vs Q_E with respect to L_N, select a point on an Ln curve that has an Ln and Qe point that corresponds to an Attainable $M_{G(PEAK)}$ value that is greater than $M_{G(max)}$. Enter the selected values in the L_N and Q_E cells below.				
For example, if $M_{G(max)}$, calculated above and shown by the horizontal line, was calculated to be 1.4, then using Ln = 5 and Qe 0.35 would result in an attainable $M_{G(PEAK)}$ = 1.52 (interpolated from Ln = 5 curve) which satisfies the requirement that the Attainable $M_{G(PEAK)} > M_{G(max)}$				
Selected Primary Inductance Ratio	$L_{N(selected)}$	3.45		
Selected Quality Factor for Resonant Network	$Q_{E(selected)}$	0.40		
Gain Required at No-Load	$M_{G(noload)}$	0.775		
f_N at Maximum Switching Frequency	$f_{N(max)}$	3.50		
The selected L_N and Q_E values should result in an LLC Gain Curve, shown below, that intersects with the $M_{G(min)}$ and $M_{G(max)}$ traces. The Gain curve from an overload condition is also plotted, showing the minimum gain at maximum frequency.				



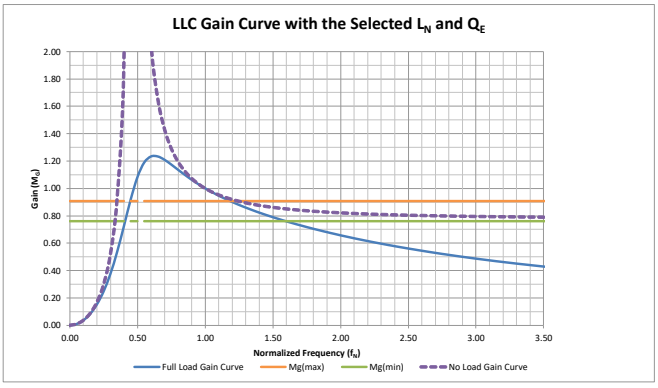


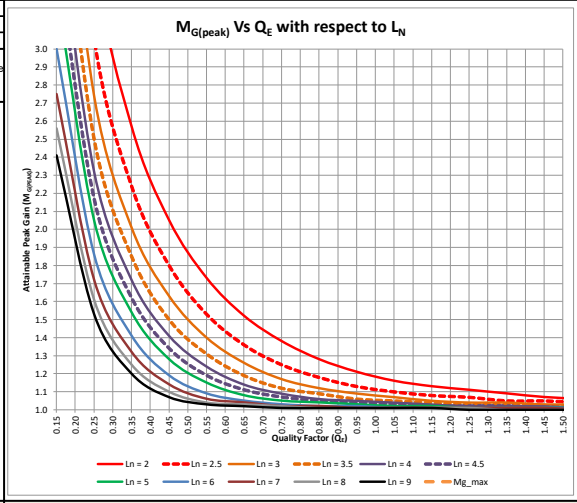
Parameters of the LLC Resonant Circuit				
Discrete resonant inductor or transformer leakage inductance used for L_s?		Discrete Inductor		
		0.9		Ignore this row
Recommended Resonant Capacitor Value	CR(recommended)	0.044	uF	
Actual Total Value of Resonant Capacitor Used	CR	0.044	uF	Enter actual value of Resonant Capacitor used
Recommended Resonant Inductor Value	LR(recommended)	57.569	uH	
Actual Resonant Inductor Value Used	LR	58	uH	Enter the actual value of the Resonant Inductor Value used
Recommended Transformer Magnetizing Inductance	LM(recommended)	200	uH	
Actual Transformer Magnetizing Inductance Used	LM	200	uH	Enter the actual value of the magnetizing inductance value used
Resultant Series Resonant Frequency	f_0	99.6	kHz	
No Load Resonant Frequency	f_P	47.2	kHz	
Resultant Inductance Ratio	L_N	**3.45**		Re-enter this value in the LN(selected) cell above to see the actual normalized frequency at MG(max) and MG(min)
Resultant Quality Factor at Full Load	Q_E	**0.40**		Re-enter this value in the $Q_{E(selected)}$ cell above to see the actual normalized frequency at $M_{G(max)}$ and $M_{G(min)}$
Gain Curve Graph Up to Date?		Yes		
f_N at $M_{G(max)}$	$f_{N(Mg\_max)}$	0.65		Enter f_N value at the second intersection of the $M_{G(max)}$ line and LLC Gain Curve shown in figure above
f_N at $M_{G(min)}$	$f_{N(Mg\_min)}$	0.8		Enter f_N value at the second intersection of the $M_{G(min)}$ line and LLC Gain Curve shown in figure above
Maximum Switching Frequency	$f_{SW(max)}$	79.7	kHz	
Minimum Switching Frequency	$f_{SW(min)}$	64.8	kHz	

Figure 1-32. LLC Maximum Gain Verification at Maximum Output Power

Select Which Device You Are Using		UCC256404		Refer datasheet for the difference of UCC25640x devices
%				
OUTPUT				
Output Voltage	V_{OUT}	46.2	V	Enter required nominal output voltage of converter
Maximum Output Power	P_{OUT}	323.4	W	Enter required maximum converter output power in Watts
Full Load Output Current	I_{OUT}	7	A	
Maximum Output Voltage Ripple	$V_{OUT(pk-pk)}$	462	mV	Enter the desired maximum output voltage ripple
Target Efficiency	η	0.92		Enter the Overall Efficiency here
%				
INPUT				
Nominal Input Voltage	V_{BLK}	390	V	Enter the nominal input voltage
Maximum DC Input Voltage	$V_{BLK(max)}$	410	V	Enter the maximum input voltage
Minimum DC Input Voltage	$V_{BLK(hu)}$	350	V	Enter the minimum input voltage

LLC STAGE				
Nominal LLC Switching Frequency	f_{LLC}	100	kHz	Enter desired nominal LLC switching frequency
LLC Transformer				
Recommended Primary/Secondary Turns Ratio	$N_{PS(recommended)}$	4.220779221		
Actual Primary/Secondary Turns Ratio	N_{PS}	3.33		Enter Actual Primary/Secondary Turns Ratio
Recommended Primary/Bias Turns Ratio	$N_{PB(recommended)}$	13.00		
Actual Primary/Bias Turns Ratio	N_{PB}	11.00		Enter Actual Primary/Bias Turns Ratio
LLC Effective Load Resistance at 110% Full Load	R_E	54.0	Ω	
LLC Effective Load Resistance at Full Load	$R_{E(full\ load)}$	59.4	Ω	
LLC Gain Range				
Minimum LLC Gain	$M_{G(min)}$	**0.759**		
Maximum LLC Gain Including Losses	$M_{G(max)}$	**0.908**		
Predicted Voltage Drop Due to Losses	V_{LOSS}	1.000	V	Enter the predicted voltage drop due to conversion losses in circuit
Select L_N and Q_E				
From the figure on the right, $M_{G(peak)}$ Vs Q_E with respect to L_N, select a point on an Ln curve that has an Ln and Qe point that corresponds to an Attainable $M_{G(PEAK)}$ value that is greater than $M_{G(max)}$. Enter the selected values in the L_N and Q_E cells below.				
For example, if $M_{G(max)}$, calculated above and shown by the horizontal line, was calculated to be 1.4, then using Ln = 5 and Qe 0.35 would result in an attainable $M_{G(PEAK)}$ = 1.52 (interpolated from Ln = 5 curve) which satisfies the requirement that the Attainable $M_{G(PEAK)} > M_{G(max)}$				
Selected Primary Inductance Ratio	$L_{N(selected)}$	3.45		
Selected Quality Factor for Resonant Network	$Q_{E(selected)}$	0.61		
Gain Required at No-Load	$M_{G(noload)}$	0.775		
f_N at Maximum Switching Frequency	$f_{N(max)}$	3.50		
The selected L_N and Q_E values should result in an LLC Gain Curve, shown below, that intersects with the $M_{G(min)}$ and $M_{G(max)}$ traces. The Gain curve from an overload condition is also plotted, showing the minimum gain at maximum frequency.				





Parameters of the LLC Resonant Circuit				
Discrete resonant inductor or transformer leakage inductance used for L_r?		Discrete Inductor		
		0.9		Ignore this row
Recommended Resonant Capacitor Value	CR(recommended)	0.044	uF	
Actual Total Value of Resonant Capacitor Used	CR	0.044	uF	Enter actual value of Resonant Capacitor used
Recommended Resonant Inductor Value	LR(recommended)	57.569	uH	
Actual Resonant Inductor Value Used	LR	58	uH	Enter the actual value of the Resonant Inductor Value used
Recommended Transformer Magnetizing Inductance	LM(recommended)	200	uH	
Actual Transformer Magnetizing Inductance Used	LM	200	uH	Enter the actual value of the magnetizing inductance value used
Resultant Series Resonant Frequency	f_0	99.6	kHz	
No Load Resonant Frequency	f_P	47.2	kHz	
Resultant Inductance Ratio	L_N	**3.45**		Re-enter this value in the LN(selected) cell above to see the actual normalized frequency at MG(max) and MG(min)
Resultant Quality Factor at Full Load	Q_E	**0.61**		Re-enter this value in the $Q_{E(selected)}$ cell above to see the actual normalized frequency at $M_{G(max)}$ and $M_{G(min)}$
Gain Curve Graph Up to Date?		Yes		
f_N at $M_{G(max)}$	$f_{N(Mg\_max)}$	1.25		Enter f_N value at the second intersection of the $M_{G(max)}$ line and LLC Gain Curve shown in figure above
f_N at $M_{G(min)}$	$f_{N(Mg\_min)}$	1.6		Enter f_N value at the second intersection of the $M_{G(min)}$ line and LLC Gain Curve shown in figure above
Maximum Switching Frequency	$f_{SW(max)}$	159.4	kHz	
Minimum Switching Frequency	$f_{SW(min)}$	124.5	kHz	

Figure 1-33. LLC Minimum Gain Verification at Minimum Output Power

1.13 How to Implement CC-CV Feedback Control?

As shown in Section 1.12, LED drivers and battery chargers must operate in either current control or voltage control, depending on the effective load resistance. The effective load resistance determines the operating point of the CC-CV controlled power supply as shown in Figure 1-34.

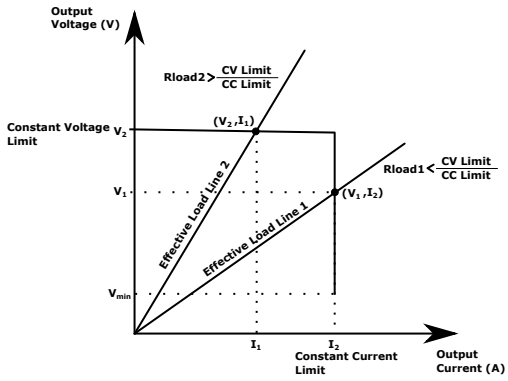


Figure 1-34. V-I Characteristics of a Power Supply With CC-CV Control Circuit

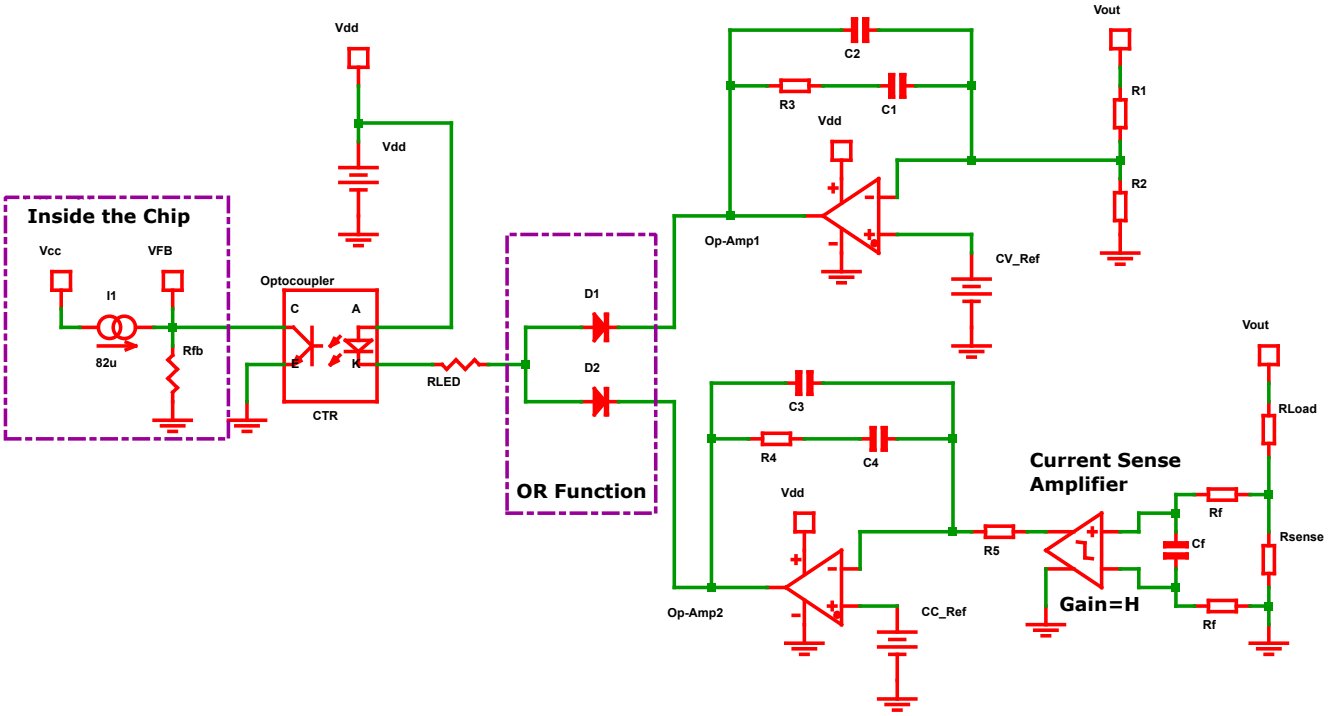


Figure 1-35. CC-CV Control Loop Circuit

1. In CC Mode, $CC_{ref} = \frac{V_{out}}{R_{load}} \cdot R_{sense} \cdot H$ where H is current sense amplifier gain.
2. In CV Mode, $CV_{ref} = \frac{R_2}{R_1 + R_2} \cdot V_{out}$

Note

- Here D1 and D2 implements the OR function such that only one control variable is controlled at a time (During CC mode, where output voltage is less than CV limit will reverse bias the D1. In CV mode, where output current is less than CC limit can reverse bias the diode D2).
- During the full load to light load transition, the current through the optocoupler LED needs to be able to vary more than I_{fb}/CTR to regulate the output voltage/current. Here I_{fb} is maximum current provided by the FB pin. So, $R_{LED} \leq \frac{V_{dd} - V_F - V_{LED}}{\left(I_{fb}/CTR\right)}$ where V_{dd}, V_F, V_{LED} are auxiliary supply voltage, diode forward voltage drop (D1 or D2), optocoupler LED drop respectively.

1.13.1 Voltage Feedback Loop (Type 2) Transfer Function

$$G_{cv}(s) = \left|\frac{V_{fb}(s)}{V_o(s)}\right| = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{(C_1 + C_2)\cdot R_1}\frac{1 + R_3C_1s}{\left(1 + \frac{sR_3C_1C_2}{C_1 + C_2}\right)s}\right) \quad (55)$$

Assuming $C_2 << C_1$, $G_{cv}(s)$ further simplifies to

$$G_{cv}(s) = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{C_1 \cdot R_1}\frac{1 + R_3C_1s}{(1 + sR_3C_2)s}\right) \quad (56)$$

This can be written as $G_{cv}(s) = G_o\left(\frac{\frac{\omega_L}{s} + 1}{1 + \frac{s}{\omega_{p1}}}\right)$ (57)

where $G_o = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{R_3}{R_1}\right)$ $\omega_L = \frac{1}{R_3 \cdot C_1}$ $\omega_{p1} = \frac{1}{R_3 \cdot C_2}$ (58)

Here ω_L is low frequency inverted zero and ω_{p1} is a high frequency pole.

1.13.2 Current Feedback Loop (Type 2) Transfer Function

$$G_{ci}(s) = \left|\frac{V_{fb}(s)}{V_{sense}(s)}\right| = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{H}{(C_3 + C_4)\cdot R_5}\frac{1 + R_4C_4s}{\left(1 + \frac{sR_4C_3C_4}{C_3 + C_4}\right)s}\right) \quad (59)$$

Assuming $C_3 << C_4$, $G_{ci}(s)$ further simplifies to

$$G_{ci}(s) = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{H}{C_4 \cdot R_5}\frac{1 + R_4C_4s}{(1 + sR_4C_3)s}\right) \quad (60)$$

This can be written as $G_{ci}(s) = G_o\left(\frac{\frac{\omega_L}{s} + 1}{1 + \frac{s}{\omega_{p1}}}\right)$ (61)

where $G_o = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{H \cdot R_4}{R_5}\right)$ $\omega_L = \frac{1}{R_4 \cdot C_4}$ $\omega_{p1} = \frac{1}{R_4 \cdot C_3}$ (62)

Here ω_L is low frequency inverted zero and ω_{p1} is a high frequency pole.

$$G_s(s) = \frac{V_{sense}(s)}{V_o(s)} = \frac{R_{sense}}{R_{Load}} \quad (63)$$

Current feedback loop transfer function would be $\left|\frac{V_{fb}(s)}{V_o(s)}\right| = G_{ci}(s)\cdot G_s(s)$ (64)

1.14 What is the Simplest Approach to Configure the Burst Mode Thresholds for UCC25640x Based on the Load Power?

Typically, the burst mode thresholds are set based on what load is the application desires to exit burst mode. For the controller to drop into burst mode, the Vcomp signal needs to drop below the BMTL threshold. In practice, the simplest way to accomplish this is to depopulate the top LL/SS resistor and adjust the output current to the required set point for burst mode entry/exit. To obtain BMTL threshold, measure the VCR waveform peak to peak when the high side and low side gates are turning off. The Excel design calculator [12] needs to be able to suggest a value for the LL/SS resistors once we have the BMTL voltage that we want to target (Let's say if we use BW option 6 do BMTH=BMTL/0.6 to get the BMTH level to put into the calculator). LL/SS pin resistors can then be populated to establish the burst mode thresholds.

1.15 How to Avoid the UCC25640x Controller to Enter into Burst Mode?

The burst mode threshold varies with input voltage. This is because as the input voltage increases, the magnitude of the resonant current drops, as does the magnitude of the AC voltage on the resonant capacitor. This means the VCR peak to peak voltage can decrease and make burst mode more likely. To avoid the burst mode, first depopulate the resistor between RVCC and LL/SS, then lower the bottom VCR capacitance. This can increase the peak to peak voltage of the VCR. The peak to peak VCR voltage needs to be higher than the burst threshold (BMT=0.2V when the resistor between RVCC and LL/SS is depopulated) in order to prevent burst mode.

1.16 What are the Methods for Preventing VCC From Decreasing Below the VCC Restart Threshold During Burst Mode?

In case of UCC256402/404, after the HV startup, the auxiliary winding can supply the VCC pin voltage. If the burst mode frequency is set too low, the VCC pin capacitor might not get enough energy from the auxiliary winding due to infrequent switching. As a result, the VCC voltage will drop below the restart threshold value. This can be avoided by using the following techniques:

1. Increasing the VCC capacitance: This will help having enough VCC voltage during burst off period.
2. Reducing the BMTL threshold so that converter switches more frequently: This can be done by either adjusting the LL/SS resistor divider or by reducing the capacitance between VCR and ground.

1.17 How Does BMTL Threshold Value Impacts the Output Voltage Ripple and the VCC Pin Voltage and Magnetizing Current?

Keeping the BMTL threshold low:

1. Makes the converter to operate at relatively higher switching frequencies. Due to the higher frequency at light load, the amplitude of the magnetizing current will be smaller and care must be taken to ensure ZVS is still achieved.
2. Makes the converter to switch more frequently during light load. Due to this, there will be enough energy supplied by the auxiliary winding so that controller's VCC pin voltage won't go below VCCrestartJFET threshold voltage. Also, the output voltage ripple will be small.

Keeping the BMTL threshold high:

1. Longer periods of no switching during light load. Due to this, higher output voltage ripple is expected
2. Limits how high the switching frequency will go during light load before ultimately dropping into burst mode. Because of this, during light load, converter can easily achieve ZVS as the there is enough magnetizing current during primary MOSFET's turn off instants.
3. Need to have relatively larger capacitance at the VCC and for boot strap so that controller doesn't hit the under-voltage limit during long burst off periods.

1.18 How to Design Magnetics for LLC?

This section provides a design of both a resonant inductor and LLC transformer. Despite the fact that this is not very optimized, it needs to be sufficient for the first prototype.

1.18.1 LLC Resonant Inductor Design

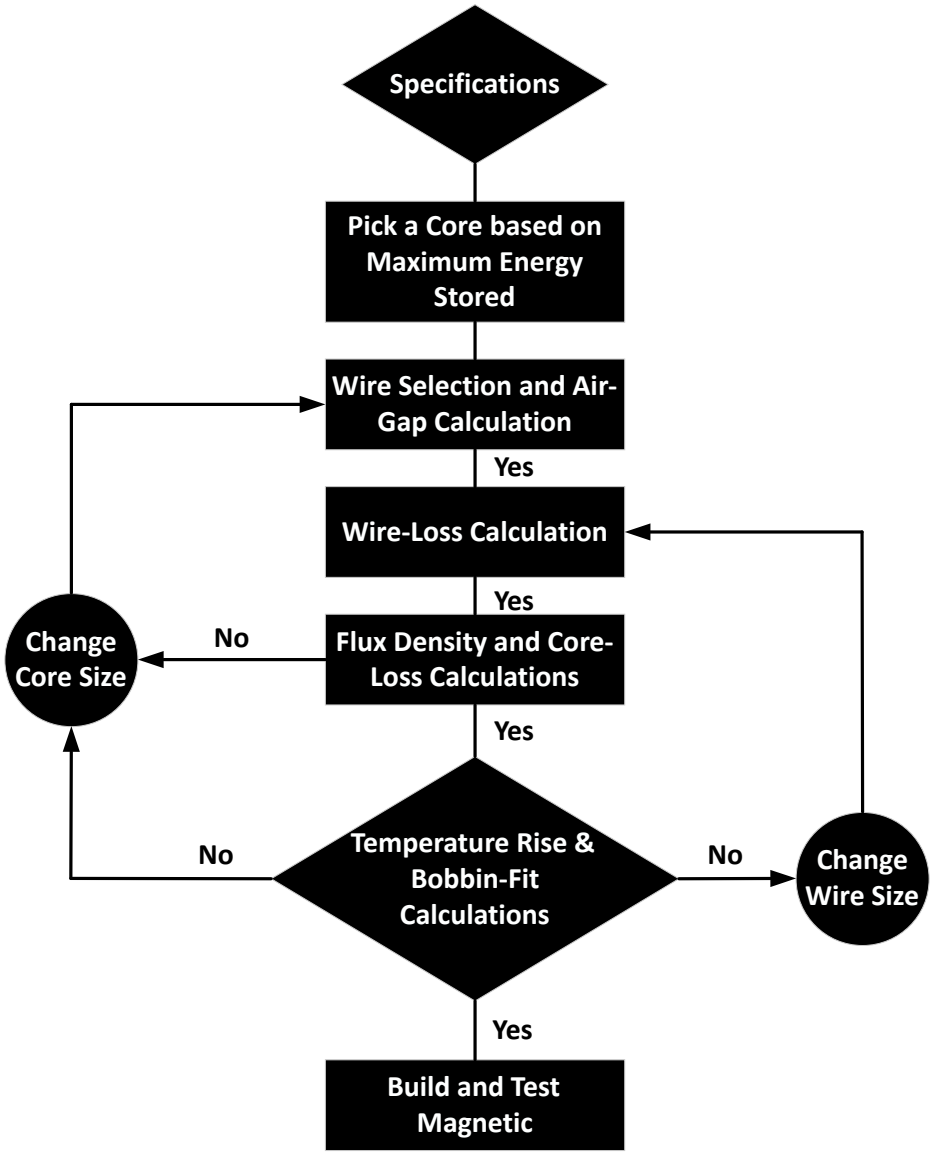


Figure 1-36. LLC Resonant Inductor Design Procedure

Here for designing the resonant inductor, the same method given in Reference [14] is followed. PFC LLC EVM [15] is considered as an design example.

Step 1: Specifications

Resonant Inductor value $L_r = 75uH$ (65)

At minimum Input voltage and at maximum output power:

Peak current of the resonant inductor $I_p = 1.9A$

RMS current of the resonant inductor $I_{rms} = 1.27A$ (66)

Switching frequency $f_{sw} = 77kHz$

At Rated Input voltage and at maximum output power:
Peak current of the resonant inductor $I_p = 1.78A$
RMS current of the resonant inductor $I_{rms} = 1.22A$
Switching frequency $f_{sw} = 88kHz$ (67)

Step 2: Pick a core based on the maximum energy to be stored

Area Product of a core $A_p = W_a A_c = \frac{LI_p{}^2}{K_u J_m B_m}(m^4)$ (68)

[Equation 10.100 in Reference 16]

where W_a is window area and A_c is core area (69)

K_u is window utilization factor (for Litz wire it is : 0.3 to 0.4) (70)

J_m is peak current density: 4 to $6A/mm^2$(under natural cooling condition) (71)

B_m is peak flux density of the core (72)

B_m is chosen such that at the operating frequency, core loss power density should be less than 150 mW/cm^3 for natural convection cooling.

In general, suggested magnetic materials for reducing core losses are 3C95, 3F4 from Ferroxcube (*Ferroxcube Cores and Accessories*) and PC47, PC90, PC95 from TDK (*TDK Cores and Accessories*).

For $K_u = 0.3,\ J_m = 4A/mm^2,\ B_m = 0.15T,\ A_p \geq 1320mm^4$ (73)

For this design, RM8 core with 3C95 material is selected. This core's effective cross section area $A_c = 63mm^2$ (*Ferroxcube RM8 core data sheet*) and minimum winding area $W_a = 31mm^2$ (*Ferroxcube RM8 bobbin data sheet*). Cores, Bobbin, Clamp can be obtained from following links: *RM8 with 3C95*, *RM8 Bobbin*, *Clamp for RM8 Core*.

Step 3: Wire Selection and Airgap calculation

The effective cross-sectional area of the bare winding is $A_w = \frac{I_p}{J_m} = \frac{1.78}{4} = 0.4450mm^2$ (74)

Let's initially select AWG21 which has a copper area about $0.4116mm^2$ which is closest to required copper area. (75)

So the actual current density would be $J_{m\_act} = \frac{1.78}{0.4116} = 4.32 A/mm^2$ (76)

In order to reduce both skin and proximity losses, Litz wire is considered for this design.

In general, for high frequency (around 100kHz) designs, AWG38-42 should be selected for each strand. (77)

The skin depth of copper at $88kHz$ is $\delta = \frac{66.2}{\sqrt{f}}\ (mm) = \frac{66.2}{\sqrt{88,000}} = 0.2232mm$ [Equation 10.148 in Reference 16]

Here AWG 38 is chosen with 50 strands for following reasons: (78)

1. Its over all copper area is equivalent to AWG21 copper area (79)
2. Each strand diameter is much less than skin depth so that current through the each strand will be uniform (80)
3. And its readily available (81)

(*Litz Wire Data from MWS Wire Industries*)

With insulation, the overall diameter (d_o) of the $UNSERVED\ LITZ\ WIRE$ of 38AWG with 50 strands is 0.9398mm (82)

(*Litz Wire Data from MWS Wire Industries*)

The cross sectional area of the insulated wire is $A_{wo} = \frac{\pi {d_o}^2}{4} = \frac{\pi \times 0.9398^2}{4} = 0.6937 mm^2$ (83)

The minimum number of turns is $N = \frac{K_u W_a}{A_{wo}} = \frac{0.3 \times 31}{0.6937} = 13.4$ (84)

Pick $N = 14$. The air-gap length is $l_g = \frac{\mu_o A_c N^2}{L_r} = \frac{4\pi \times 10^{-7} \times 63 \times 10^{-3} \times 14^2}{75 \times 10^{-6}} = 0.207 mm$ (85)

Step 4: Copper Loss Calculation

The winding width of the bobbin is 8.9mm (86)

(*Ferroxcube RM8 bobbin data sheet*)

Since there are 14 bundle turns each with 0.9398mm over all diameter, total number of bundled winding layers (N_l) would be 2. (87)

Each bundle has a total number of strands $k = 50$ (88)

(represented in Figure 1-37 as a 7 × 7 matrix)

The strands in each bundle are modelled as a square with $\sqrt{k}$ strands on each side of the bundle as shown in below figure (89)

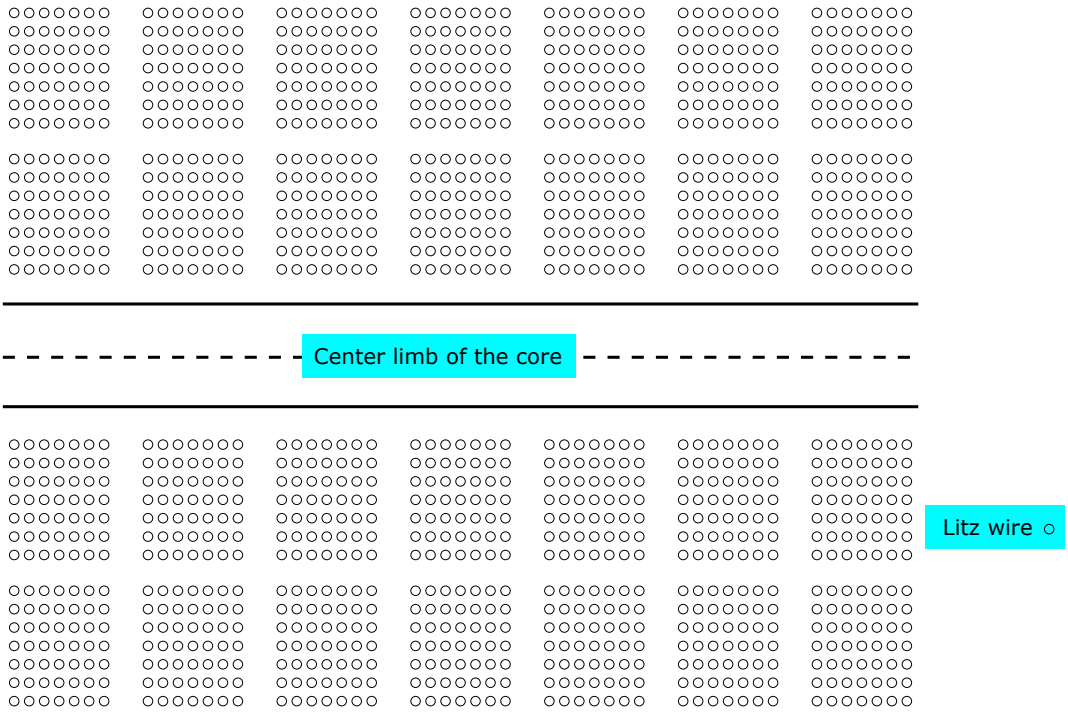


Figure 1-37. Model of the Litz Wire Winding Around a Central Core

The effective number of layers of the Litz-wire winding with the square arrangement of the strands in a bundle is given by $N_{ll} = N_l \times \sqrt{k} = 2 \times \sqrt{50} = 14.14 \simeq 14$ (90)

The total number of strands in each layer is given as N_{sl} =
the number of bundle turns in a layer × number of strands of each side of the square bundle (91)
$= 7 \times \sqrt{50} = 49.49 \simeq 50$

The mean length of the turn is $l_T = 42mm$ (92)

(*Ferroxcube RM8 bobbin data sheet*)

The DC resistance of the single AWG38 strand is $R_{wDCs} = l_T \times (AWG38$ DC resistance per m)
$= 42 \times 2.1266 = 89.32m\Omega$ (93)

The AC power loss of a single layer is given by P_{ac} = DC power loss of a single layer × φ × Q′(φ, m) (94)

[Table 10.1 in Reference 16]

[Equation 10.80 in Reference 9]

Here $\varphi = \sqrt{\eta}\sqrt{\frac{\pi}{4}}\frac{d_s}{\delta}$
where η is porosity factor, d_s is strand bare wire diameter, δ is skin depth for a given frequency (95)

[Equation 10.74 in Reference 9]

$$Q'(\varphi, m) = (2m^2 - 2m + 1)G_1(\varphi) - 4m(m-1)G_2(\varphi) \quad (96)$$

[Equation 10.81 in Reference 9]

$$G_1(\varphi) = \frac{\sinh(2\varphi) + \sin(2\varphi)}{\cosh(2\varphi) - \cos(2\varphi)}$$
$$G_2(\varphi) = \frac{\sinh(\varphi)\cos(\varphi) + \cosh(\varphi)\sin(\varphi)}{\cosh(2\varphi) - \cos(2\varphi)} \quad (97)$$

[Equation 10.76 in Reference 9]

m for each layer can be found by $m = \frac{mmf(h)}{mmf(h) - mmf(0)}$ (98)
where h is thickness of each layer

[Equation 10.81 in Reference 9]

In this design example, the DC power loss of a single layer is given as =
square of the RMS current through each strand × DC resistance of a single strand × total number of strands in a single layer (99)
$= \left(\frac{I_{rms}}{k}\right)^2 \times R_{wDCs} \times N_{sl} = \left(\frac{1.22}{50}\right)^2 \times 89.32m\Omega \times 50 = 2.66mW$

Porosity factor η = $\frac{\text{Number of strands per layer } (N_{sl}) \times S\text{trand diameter with insulation}}{\text{width of the bobbin}} = \frac{50 \times 0.124mm}{8.9\text{mm}} = 0.7$ (100)

[Equation 10.73 in Reference 9]

In this design, mmf due to each layer = current through each strand × number of strands in a layer = $\frac{I_{rms}}{k} \times N_{sl}$ (101)

$So,$ layer 1's m value can be determined by $m = \frac{\left(\frac{I_{rms}}{k} \times N_{sl}\right)}{\left(\frac{I_{rms}}{k} \times N_{sl}\right) - 0} = 1$ (102)

[Equation 10.90 in Reference 9]

Layer 2's m value can be determined by $m = \frac{2\left(\frac{I_{rms}}{k} \times N_{sl}\right)}{2\left(\frac{I_{rms}}{k} \times N_{sl}\right) - \left(\frac{I_{rms}}{k} \times N_{sl}\right)} = 2$ (103)

Similarly, m values for other adjacent layers increase by 1. Since there are 14 layers, m value increases up to 14. (104)

$$\varphi = \sqrt{\eta}\sqrt{\frac{\pi}{4}}\frac{d_s}{\delta} = \sqrt{0.7}\sqrt{\frac{\pi}{4}}\frac{0.1007}{0.2232} = 0.335 \quad (105)$$

where 0.1007 is AWG38 bare wire diameter in mm [Table 10.1 in Reference 16].

The copper loss for all the layers is given by P_w = DC power loss of a single layer $\times \sum_{m=1}^{14} \varphi Q'(\varphi, m) = 47mW$

Step 5: Flux Density and Core-Loss Calculation

The amplitude of the core magnetic flux density at rated input voltage is $B_m = \frac{\mu_o N I_p}{l_g} = \frac{4\pi \times 10^{-7} \times 14 \times 1.78}{0.2 \times 10^{-3}}$ (106)

$= 0.157T$

The core loss per unit volume (P_v) at $0.157T,\ 88kHz$ is $150mW/cm^3$ (107)

(Use power loss calculator in the Ferroxcube design tool for finding core loss of the material *Core Loss Calculator*)

The total core loss is $P_C = V_C P_v = 150mW/cm^3 \times 2440mm^3 = 366mW$ (108)

The amplitude of the core magnetic flux density at minimum input voltage is $B_{m\_\max} = \frac{\mu_o N I_{p\_\max}}{l_g}$ (109)

$= \frac{4\pi \times 10^{-7} \times 14 \times 1.9}{0.2 \times 10^{-3}} = 0.167T$

At worst case current, $B_{m\_\max}$ is less than saturation flux density of the ferrite material. (110)

Step 6: Temperature Rise and Bobbin Fit Calculations

Total power loss of the inductor is $P_{wc} = P_w + P_C = 0.4W$ (111)

The surface area of RM-8 core is $A_t = 20.2cm^2$ (112)

Table 3-43

The surface power loss density is $\psi = \frac{P_{wc}}{A_t} = \frac{0.4W}{20.2cm^2} = 0.0206W/cm^2$

The temperature rise of the inductor is $\Delta T = 450\psi^{0.826} = 450 \times \left(0.0206W/cm^2\right)^{0.826} = 18.25^oC$ (113)

[Equation 10.193 in Reference 16]

The actual core window utilization factor is $K_u = \frac{NA_{wo}}{W_a} = \frac{14 \times 0.6937}{31} = 0.3133$ (114)

1.18.2 LLC Transformer Design

Step 1: LLC Center-Tapped Transformer Specifications

Magnetizing Inductance value of the transformer $L_m = 510uH$ (115)

Turns ratio from primary to secondary $n = 16.5$ (116)

Forward voltage drop of the secondary diode $V_f = 0.7V$ (117)

At minimum Input voltage (365V) and at maximum output power (12V,15A):
- Peak current of the magnetizing inductor $I_{mp\_\max} = 1.15A$
- RMS current of the magnetizing inductor $I_{mrms\_\max} = 0.74A$
- Peak current of the primary winding $I_{p\_\max} = 1.9A$
- RMS current of the primary winding $I_{prms\_\max} = 1.27A$
- Peak current of the each secondary winding $I_{s\_\max} = 32.2A$
- RMS current of the each secondary winding $I_{srms\_\max} = 13.65A$
- Switching frequency $f_{sw\_\min} = 77kHz$

(118)

At Rated Input voltage (390V) and at maximum output power (12V,15A):
- Peak current of the magnetizing inductor $I_{mp} = 1.1A$
- RMS current of the magnetizing inductor $I_{mrms} = 0.68A$
- Peak current of the primary winding $I_p = 1.78A$
- RMS current of the primary winding $I_{prms} = 1.22A$
- Peak current of the each secondary winding $I_s = 28.9A$
- RMS current of the each secondary winding $I_{srms} = 13A$
- Switching frequency $f_{sw} = 88kHz$

(119)

Step 2: Pick a Core Based on the Output Power

Area Product of a core $A_p = W_a A_c = \frac{\sum_{n=1}^{m} \frac{I_n V_n}{J_{rms\_n}}}{4K_u f_{sw} B_m} (m^4)$ (120)

[Equation 11.12 in Reference 16]

where W_a is window area, A_c is core area (121)

I_n is rms value of the current through the nth winding (122)

V_n is rms value of the voltage across the nth winding (123)

J_{rms_n} is rms value of the current density of the nth winding: $4\ to\ 6A/mm^2$ (124)

K_u is window utilization factor (For Litz wire it is : 0.3 to 0.4) (125)

B_m is peak flux density of the core (126)

B_m should be chosen such that at the operating frequency, core loss power density should be less than 150 mW/cm^3 for natural convection cooling.

In general, suggested magnetic materials for reducing core losses are 3C95, 3F4 from Ferroxcube (*Ferroxcube Cores and Accessories*) and PC47, PC90, PC95 from TDK (*TDK Cores and Accessories*).

For $K_u = 0.3,\ J_{rms\_p} = 5A/mm^2, J_{rms\_s} = 6A/mm^2,\ B_m = 0.15T,\ A_p \geq 6476.9mm^4$ (127)

For this design, PQ26/25 core with 3C95 material is selected. This core's effective cross section area $A_c = 120mm^2$ (*Ferroxcube PQ26/25 core data sheet*) and minimum winding area, mean turn length are $W_a = 50.97mm^2, MLT = 56.2mm$ (*Ferroxcube PQ26/25 bobbin data sheet*). Cores, Bobbin, Clamp can be obtained at *PQ26/25 with 3C95*, *PQ26/25 Bobbin*, *Clamp for PQ26/25 Core*.

Step 3: Turns and airgap calculation

$$N_p \times A_c \times (2 \times B_m) = \frac{n \times (V_o + V_f)}{2 \times f_{sw}} \quad (128)$$

$$N_p = \frac{16.5 \times (12 + 0.7)}{120 \times 10^{-6} \times 2 \times 0.15 \times 2 \times 88 \times 10^{3}} = 33.0729 \quad (129)$$

$$N_s = \frac{N_p}{n} = \frac{33.07}{16.5} = 2.0044 \quad (130)$$

Lets consider primary number of turns (N_p) and secondary number of turns (N_s) as 33 and 2 respectively. (131)

The air-gap length is $l_g = \frac{\mu_o A_c {N_p}^2}{L_m} = \frac{4\pi \times 10^{-7} \times 120 \times 10^{-3} \times 33^2}{510 \times 10^{-6}} = 0.32mm$ (132)

Step 4: Wire selection for both primary and secondary

The effective cross-sectional area of the bare winding of the primary should be

$$A_{wp} = \frac{I_{prms}}{J_{rms}} = \frac{1.22}{5} = 0.244mm^2 \quad (133)$$

AWG23 has a copper area about $0.2558mm^2$ which is closest to required copper area. (134)

In general, for high frequency (around 100kHz) designs, AWG38-42 should be selected for each strand. (135)

The skin depth of copper at $88kHz$ is $\delta_w = \frac{66.2}{\sqrt{f}}\ (mm) = \frac{66.2}{\sqrt{88,000}} = 0.2232mm$ (136)

[Equation 10.148 in Reference 16]

Here AWG 38 is chosen with 30 strands for following reasons: (137)

1. Its over all copper area ($0.2432mm^2$) is closest to required copper area (138)
2. Each strand diameter is much less than skin depth so that current through the each strand will be uniform (139)
3. And its readily available (140)

(*Litz Wire Data from MWS Wire Industries*)

So the actual current density would be $J_{p\_act} = \frac{1.22}{0.2432} = 5.01 {}^{A}/_{mm^2}$ (141)

With insulation, the overall diameter (d_{op}) of the $SERVED\ LITZ\ WIRE$ of $38AWG$ with 30 strands is 0.7874mm (142)

Area required by the primary winding $= N_p \times \frac{\pi \times {d_{op}}^2}{4} = 33 \times \frac{\pi \times 0.7874^2}{4} = 16.0692mm^2$ (143)

For the each secondary winding, the effective cross-sectional area of the bare winding of the each secondary should be $A_{ws} = \frac{I_{srms}}{J_{rms}} = \frac{13}{6} = 2.167mm^2$ (144)

AWG14 has a copper area about $2.082mm^2$ which is closest to required copper area. (145)

Here AWG38 with 260 strands are considered for each secondary winding which has a bare copper about $2.1078mm^2$ (146)

So the actual current density of the each secondary winding would be $J_{s\_act} = \frac{13}{2.1078} = 6.16 {}^{A}/_{mm^2}$ (147)

With insulation, the overall diameter (d_{os}) of the $UNSERVED\ LITZ\ WIRE$ of $38AWG$ with 260 strands is 2.286mm (148)

(*Litz Wire Data from Remington Industries*, *Digikey Link*)

Area required by the each secondary winding $= N_s \times \frac{\pi \times {d_{os}}^2}{4} = 2 \times \frac{\pi \times 2.286^2}{4} = 8.2087mm^2$ (149)

Window utilization factor $K_u = \frac{Area\ occupied\ by\ each\ winding}{Overall\ Window\ Area} = \frac{16.0692 + 8.2087 + 8.2087}{50.97} = 0.637$ (150)

Step 5: Wire Loss Calculation with Interleaved Winding

The winding width of the bobbin is 13.56mm (151)

(*Ferroxcube PQ26/25 bobbin datasheet*)

In primary, since there are 33 bundle turns with 0.7874mm over all diameter, total number of bundled winding layers (N_{pl}) would be 2. (152)

Each bundle has a total number of strands $k_p = 30$ (153)

The strands in each bundle are modelled as a square with $\sqrt{k_p}=\sqrt{30} \cong 6$ strands on each side of the bundle (154)

The total number of strands in each layer is given as $N_{psl} =$ the number of bundle turns in a layer × number of strands of each side of the square bundle $= 17 \times 6 = 102$ (155)

The mean length of each turn is $l_T = 56.2mm$ (156)

(*Ferroxcube PQ26/25 bobbin datasheet*)

The DC resistance of the single AWG38 strand is $R_{wDCs} = l_T \times (AWG38$ DC resistance per m$) = 56.2mm \times 2.1266\ \Omega/m = 119.5m\Omega$ (157)

The AC power loss of a single layer is given by $P_{ac} =$ DC power loss of a single layer $\times\ \varphi \times Q'(\varphi, m)$ (158)

[Equation 10.80 in Reference 9]

Here $\varphi = \sqrt{\eta}\sqrt{\frac{\pi}{4}}\frac{d_s}{\delta}$ (159)

where η is porosity factor, d_s is strand bare wire diameter, δ is skin depth for a given frequency

[Equation 10.74 in Reference 9]

$Q'(\varphi, m) = (2m^2 - 2m + 1)G_1(\varphi) - 4m(m-1)G_2(\varphi)$ (160)

[Equation 10.81 in Reference 9]

$$G_1(\varphi) = \frac{\sinh(2\varphi) + \sin(2\varphi)}{\cosh(2\varphi) - \cos(2\varphi)}$$
$$G_2(\varphi) = \frac{\sinh(\varphi)\cos(\varphi) + \cosh(\varphi)\sin(\varphi)}{\cosh(2\varphi) - \cos(2\varphi)} \quad (161)$$

[Equation 10.76 in Reference 9]

m for each layer can be found by $m = \frac{mmf(h)}{mmf(h) - mmf(0)}$ (162)

where h is thickness of each layer

[Equation 10.81 in Reference 9]

In this design example, the DC power loss of a single layer of the primary is given as =
square of the RMS current through each strand × DC resistance of a single strand × total number of strands in a single layer (163)
$= \left(\frac{I_{rms}}{k}\right)^2 \times R_{wDCs} \times N_{psl} = \left(\frac{1.22}{30}\right)^2 \times 119.5m\Omega \times 102 = 20.6mW$

Porosity factor $\eta_p = \frac{\text{Number of strands per layer } (N_{psl}) \times S\text{trand diameter with insulation}}{\text{width of the bobbin}} = \frac{102 \times 0.124mm}{13.56\text{mm}} = 0.933$ (164)

For each of the secondary winding, since there are 2 bundle turns each with 2.286mm over all diameter, total number of bundled winding layers (N_{s1l}, N_{s2l}) would be 1. (165)

Each secondary winding bundle has a total number of strands $k_s = 260$ (166)

The strands in each bundle are modelled as a square with $\sqrt{k_s} = \sqrt{260} \cong 16$ strands on each side of the bundle (167)

The total number of strands in each layer of the secondary is given as N_{ssl} =
The number of bundle turns in a layer × number of strands of each side of the square bundle (168)
$= 2 \times 16 = 32$

The DC resistance of the single AWG38 strand of the secondary is $R_{wDCs} = l_T \times (AWG38 \text{ DC resistance per m})$ (169)
$= 56.2mm \times 2.1266\ \Omega/m = 119.5m\Omega$

The DC power loss of a single layer of the secondary is given as =
square of the RMS current through each strand × DC resistance of a single strand × total number of strands in a single layer (170)
$= \left(\frac{I_{rms}}{k}\right)^2 \times R_{wDCs} \times N_{ssl} = \left(\frac{13}{260}\right)^2 \times 119.5m\Omega \times 32 = 9.56mW$

Porosity factor $\eta_s = \frac{\text{Number of strands per layer } (N_{ssl}) \times S\text{trand diameter with insulation}}{\text{width of the bobbin}} = \frac{32 \times 0.124mm}{13.56\text{mm}} = 0.3$ (171)

So, layer sequence would be

1. 1st bundle layer of the primary winding
2. Secondry-1 bundle layer (172)
3. Secondry-2 bundle layer
4. 2nd bundle layer of the primary winding

For Primary, $\varphi_p = \sqrt{\eta}\sqrt{\frac{\pi}{4}}\frac{d_s}{\delta} = \sqrt{0.933}\sqrt{\frac{\pi}{4}}\frac{0.1007}{0.2232} = 0.386$ (173)

For Secondary, $\varphi_s = \sqrt{\eta}\sqrt{\frac{\pi}{4}}\frac{d_s}{\delta} = \sqrt{0.3}\sqrt{\frac{\pi}{4}}\frac{0.1007}{0.2232} = 0.219$ (174)

MMF due to the each layer of the primary = current through each strand × number of strands in a layer = $\frac{I_{prms}}{k_p} \times N_{psl}$ (175)

$So,$ layer 1's m value can be determined by $m = \frac{\left(\frac{I_{prms}}{k_p} \times N_{psl}\right)}{\left(\frac{I_{prms}}{k_p} \times N_{psl}\right) - 0} = 1$ (176)

Layer 2's m value can be determined by $m = \frac{2\left(\frac{I_{prms}}{k_p} \times N_{psl}\right)}{2\left(\frac{I_{prms}}{k_p} \times N_{psl}\right) - \left(\frac{I_{prms}}{k_p} \times N_{psl}\right)} = 2$ (177)

Similarly, m value for other adjacent layers increases by 1. Since there are 6 layers for the first bundled primary, m value increases upto 6. (178)

Same method has been followed to find out the m value for other layers (179)

The copper loss of all the layers in the primary is given by P_{pw}

$= \text{DC power loss of a single layer of the primary} \times \left[\sum_{m=1}^{6} \varphi Q'(\varphi, m) + \sum_{m=-8.043}^{-3.043} \varphi Q'(\varphi, m)\right] = 295mW$ (180)

The copper loss of all the layers in the secondary1 is given by P_{sw1}

$= \text{DC power loss of a single layer of the secondary1} \times \left[\sum_{m=-11.763}^{3.237} \varphi Q'(\varphi, m)\right] = 158mW$ (181)

The copper loss of all the layers in the secondary2 is given by P_{sw2}

$= \text{DC power loss of a single layer of the secondary2} \times \left[\sum_{m=4.237}^{19.237} \varphi Q'(\varphi, m)\right] = 170mW$ (182)

Total copper losses $P_w = P_{pw} + P_{sw1} + P_{sw2} = 295mW + 158mW + 170mW = 0.623mW$ (183)

Step 6: Flux Density and Core-Loss Calculation

The amplitude of the core magnetic flux density at rated input voltage is $B_m = \frac{L_m I_{mp}}{N_p A_c} = \frac{510 \times 10^{-6} \times 1.1}{33 \times 120 \times 10^{-6}} = 0.142T$ (184)

The core loss per unit volume (P_v) at $0.142T,\ 88kHz$ is $130mW/cm^3$ (185)

The total core loss is $P_C = V_C P_v = 130mW/cm^3 \times 6530mm^3 = 848mW$ (186)

The amplitude of the core magnetic flux density at minimum input voltage is $B_{m\_\max} = \frac{L_m I_{mp\_\max}}{N_p A_c}$ (187)

$= \frac{510 \times 10^{-6} \times 1.15}{33 \times 120 \times 10^{-6}} = 0.148T$

At worst case current, $B_{m\_\max}$ is less than saturation flux density of the ferrite material. (188)

Step 7: Temperature rise and Bobbin Fit Calculations

Total power loss of the transformer is $P_{wc} = P_w + P_C = 1.472W$ (189)

The surface area of PQ26/25 core is $A_t = 32.6cm^2$ (190)

Table 3-39

$$\text{The surface power loss density is } \psi = \frac{P_{wc}}{A_t} = \frac{1.472W}{32.6cm^2} = 0.045W/cm^2 \quad (191)$$

$$\text{The temperature rise of the transformer is } \Delta T = 450\psi^{0.826} = 450 \times \left(0.045W/cm^2\right)^{0.826} = 34.7\ ^oC \quad (192)$$

[Equation 10.193 in Reference 16]

$$\text{The actual core window utilization factor is } K_u = \frac{Area\ occupied\ by\ each\ winding}{Overall\ Window\ Area} = \frac{16.0692 + 8.2087 + 8.2087}{50.97} = 0.637 \quad (193)$$

1.19 How is the Dead Time in UCC25640x Determined During ZCS Detection and in the Absence of Valid Slew Rate Detection?

Case 1: Valid Slew Rate Detection and No ZCS

As soon as the high side gate (HO) is turned off, the low side gate (LO) will be turned on after the slew rate has been detected. The same dead time will be copied over during low side turn off to high side turn on.

Case 2: No Slew Rate Detection and No ZCS

If no valid slew rate detection occurs after the HO turn off, the dead time during both transitions (HO turn off to LO turn on) and (LO turn off to HO turn on) depends on the resonant current polarity. Furthermore, this dead time will not exceed 1.1us.

Case 3: ZCS during HO turn off and No ZCS during LO turn off

If the ZCS is detected during HO turn off, the dead time from HO off to LO on is determined by the following factors:

1. The slew rate detection .
2. If no appropriate slew rate detection is available, it is determined by the polarity of the resonant current (ISNS signal). The maximum dead time here will not exceed 150us.

The dead time during LO turn off to HO turn on depends on the resonant current polarity. Furthermore, this dead time will not exceed 1.1us.

Case 4: No ZCS during HO turn off and ZCS during LO turn off

The dead time during HO off to LO on depends on the slew rate detection similar to case1. However, If no valid slew rate detection occurs after the HO turn off, the dead time during HO turn off to LO turn on depends on the resonant current polarity. Furthermore, this dead time will not exceed 1.1us.

If the ZCS is detected during LO turn off, the dead time from LO off to HO on is determined by the polarity of the resonant current (ISNS signal). The maximum dead time here will not exceed 150 us.

Case 5: ZCS during both HO turn off and LO turn off

If the ZCS is detected during HO turn off, the dead time from HO off to LO on is determined by the following factors:

1. The slew rate detection
2. If no appropriate slew rate detection is available, it is determined by the polarity of the resonant current (ISNS signal). The maximum dead time here will not exceed 150 us.

If the ZCS is detected during LO turn off, the dead time from LO off to HO on is determined by the polarity of the resonant current (ISNS signal). The maximum dead time here will not exceed 150 us.

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