*Application Note*

# How to Avoid LMG3427 ZCD Timing Issue Caused by Inter-phase Capacitance in TCM PFC

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**ABSTRACT**

*This document was translated from a simplified Chinese source.* (ZHCAG12A)

This article describes the ZCD implementation principle of the LMG3427 and its application in interleaved triangular current mode (TCM) PFCs. It presents the application timing for interleaved TCM PFCs based on the LMG3427. It also analyzes the problematic waveforms and timings of ZCD timing issues caused by inter-phase capacitance in applications. Finally, it provides related design recommendations to avoid LMG3427 ZCD timing issues caused by inter-phase capacitance in TCM PFC applications.

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# 1 Implementation of LMG3427 in Interleaved TCM PFC

## 1.1 Topology of Interleaved TCM PFC

In TCM-controlled PFC applications, ZVS of active FETs is critical to improving system efficiency. The structure of a three-phase interleaved TCM PFC is shown in Figure 1-1. When the inductor current crosses zero, the LMG3427 generates a ZCD signal, and the MCU calculates the corresponding turn-on delay for sync FETs after it detects the ZCD signal, allowing the inductor to obtain a certain negative current to provide conditions for ZVS of the lower bridge FETs. Therefore, in TCM PFC applications, accurate detection of inductor current zero crossing becomes extremely important. If the zero-crossing signal is generated prematurely, it may result in insufficient negative current or the current may not actually cross zero, causing the lower FETs to lose their ZVS and thereby reducing system efficiency. Similarly, if the zero-crossing signal is generated late, the negative current may become too large, which increases turn-on losses and affects system efficiency. However, a TCM solution based on the ZCD feature of the LMG3427 enables accurate inductor current zero-crossing detection, achieving efficient operation of the entire system. Figure 1-1 shows the circuit diagram of a three-phase interleaved TCM PFC, where S11 and S12 are the fast FETs for the first phase, S21 and S22 are the fast FETs for the second phase, and S31 and S32 are the fast FETs for the third phase. These three phases are 120 degrees out of phase. SN1 and SN2 are slow FETs. L1, L2, and L3 are the phase inductors, Vin represents the AC input voltage, and Cout represents the output bus capacitance.

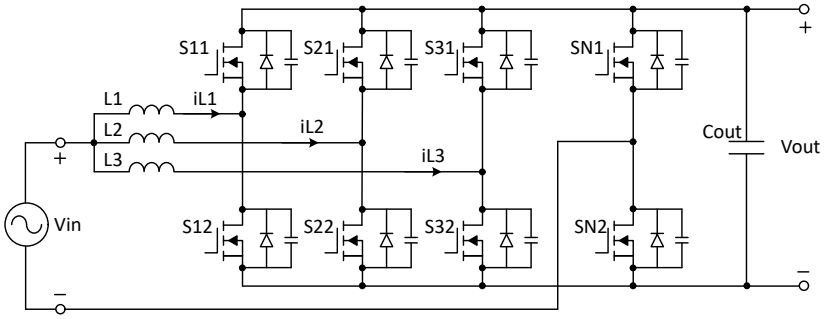


**Figure 1-1. Three-Phase Interleaved TCM PFC Topology**

## 1.2 ZCD Detection Principle for LMG3427

Figure 1-2 and Figure 1-3 show the ZCD detection timings for the LMG3427, with the positive direction of current being from drain to source.

As shown in Figure 1-2, when the IN pin is high, if the inductor current is negative at this point, at the moment that the current transitions from negative to positive after a duration of tzcd_Blank, after a ZCD signal detection delay of tzcd_det, the LMG3427 generates a ZCD pulse with a pulse width of twd_zcd. This ZCD pulse signal can be used to alert the MCU to the zero crossing of the inductor current.

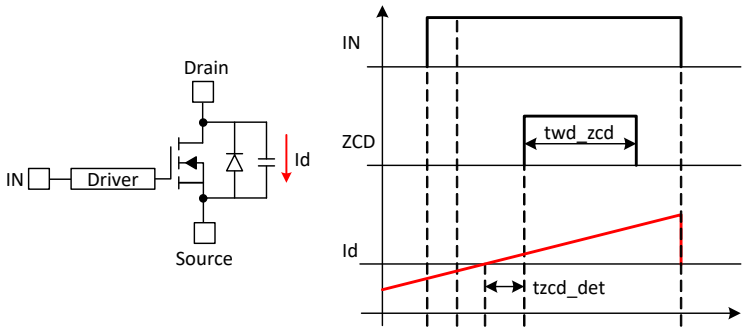


**Figure 1-2. ZCD Pulse Timing With Current Being Negative While the IN Pin Is Asserted High**

As shown in Figure 1-3, when the IN pin is high, if the current is already positive, after a duration of tzcd_Blank, the LMG3427 directly generates a ZCD pulse with a pulse width of twd_zvd.

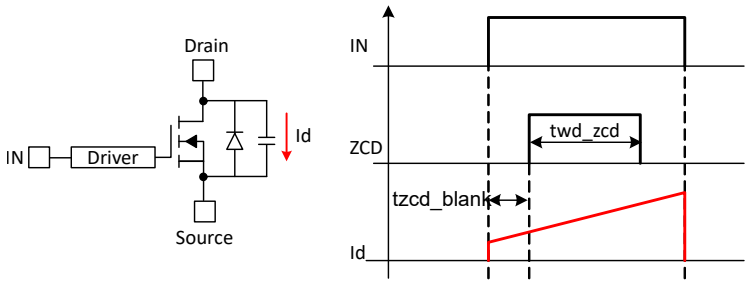


**Figure 1-3. ZCD Pulse Timing With Current Being Positive While the IN Pin Is Asserted High**

## 1.3 Application Timing for TCM PFC Based on LMG3427

In TCM PFCs, three phases operate in an interleaved manner. To simplify analysis, single-phase operation is used as an example to analyze the operating timing of the LMG3427 when applied in TCM PFCs. Figure 1-4 shows the operating structure of a single-phase TCM PFC.

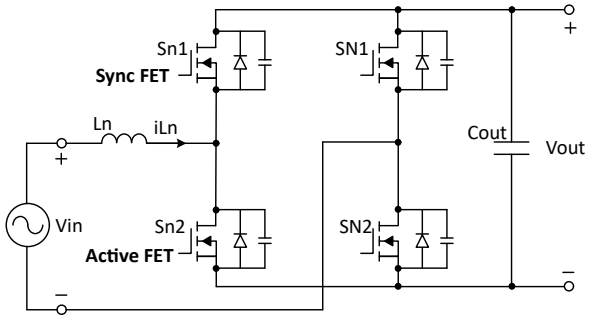


**Figure 1-4. Operating Structure of Single-Phase TCM PFC**

Figure 1-5 shows the operating timing analysis of an LMG3427-based TCM PFC.

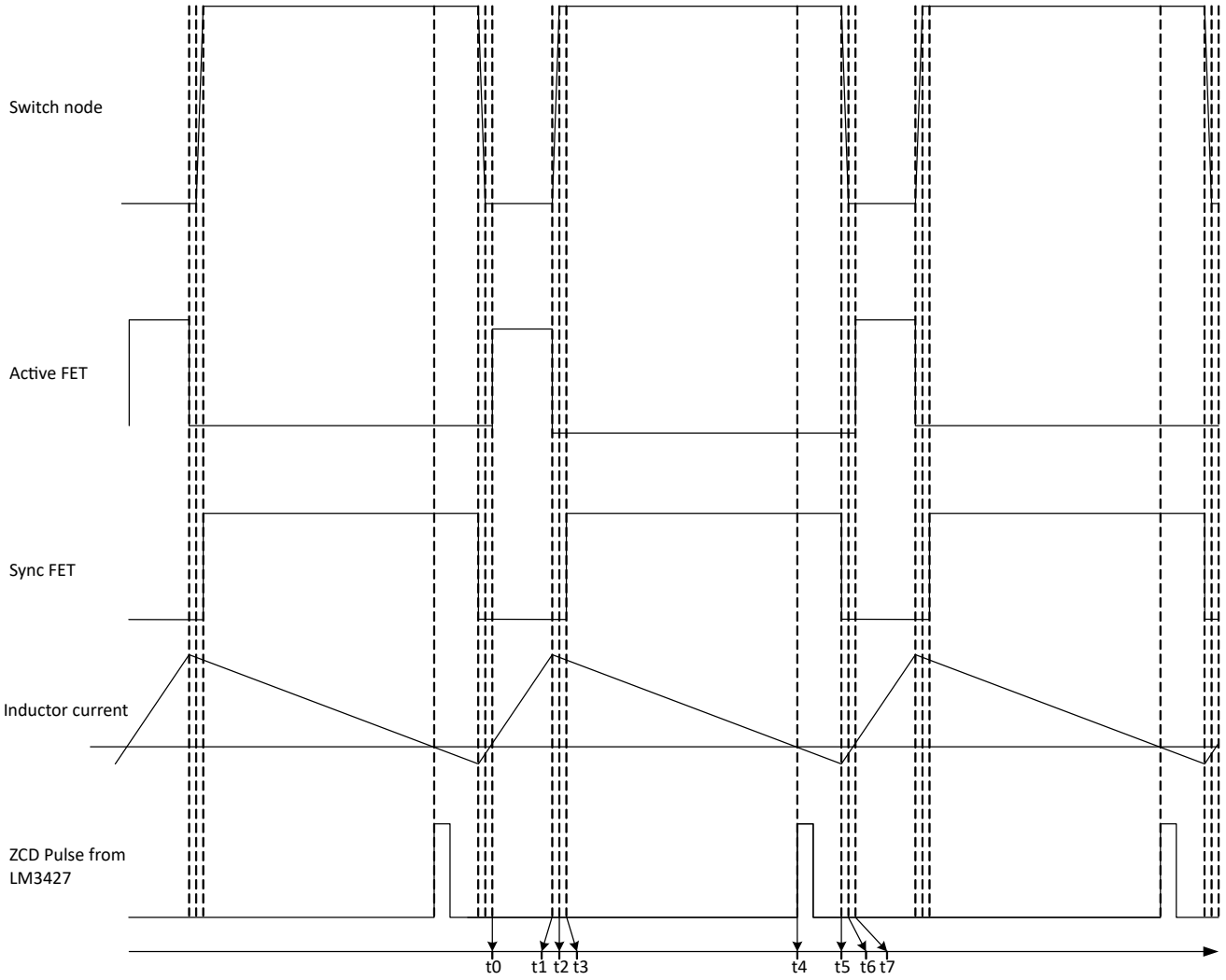


**Figure 1-5. Application Timing for TCM PFC Based on LMG3427**

Stage 1 (t0–t1): At t0, the active FET is turned on, and the inductor current starts to rise linearly.

Stage 2 (t1–t2): At t1, the active FET is turned off, while the sync FET stays off, and the inductor current starts to charge the Coss of the active FET and also discharge the Coss of the sync FET.

Stage 3 (t2–t3): At t2, the sync FET is fully discharged and remains off. The inductor current starts to freewheel through the sync FET, preparing for ZVS of the sync FET.

Stage 4 (t3–t4): At t3, ZVS of the sync FET is enabled. During this stage, the inductor current decreases linearly.

Stage 5 (t4–t5): At t4, the inductor current crosses zero. After a ZCD detection delay (not indicated in the diagram), the ZCD pin of the LMG3427 generates a ZCD pulse to indicate the inductor current zero crossing. The sync FET continues to be on for a period of time until t5, allowing the inductor to draw a certain negative current, creating conditions for ZVS of the active FET. This period between t4 and t5 can be referred to as the turn-off delay of the sync FET.

Stage 6 (t5–t6): At t5, the sync FET is turned off. The inductor current is negative at this point and therefore starts to charge the Coss of the sync FET and discharge the Coss of the active FET.

Stage 7 (t6–t7): At t6, the Coss of the active FET is fully discharged. Because the active FET remains off at this point, the inductor current starts to freewheel through the active FET, preparing for ZVS of the active FET. At t7, ZVS of the active FET is enabled.

# 2 ZCD Timing Issue Caused by Inter-phase Capacitance in TCM PFC

## 2.1 Inter-phase Parasitic Capacitance Caused by Poor Layout

The figure below shows the inter-phase parasitic capacitance caused by a poor layout in practice and its equivalent circuit. As shown in the figure, there is a large overlapping area between the switch-node planes of phases A and B, which introduces a relatively large parasitic capacitance between the switch nodes of phases A and B.

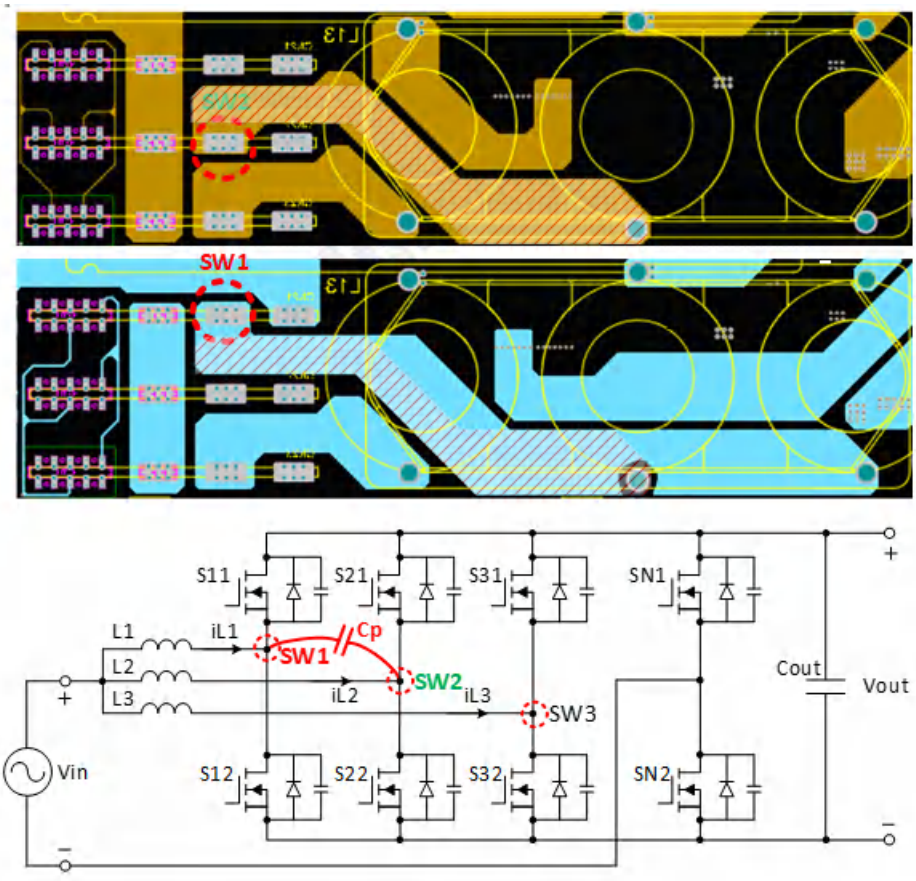


**Figure 2-1. Poor PCB Design with Large Overlap Between Adjacent SW Node Planes**

## 2.2 ZCD Timing Issue Caused by Inter-phase Parasitic Capacitance

Figure 2-2 shows the problematic ZCD waveform caused by the inter-phase capacitance. The LMG3427 generates the ZCD signal earlier than the inductor current crosses zero, which causes issues with the system's ZCD timing, leading to the disappearance of the system's ZVS characteristic.

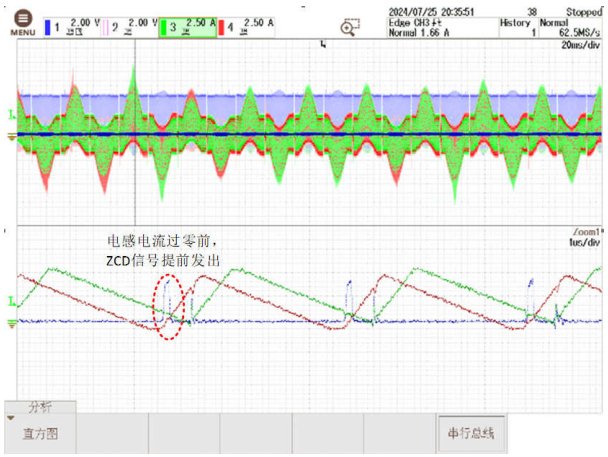


**Figure 2-2. ZCD Problematic Waveform Caused by Inter-phase Capacitance, with the Phase B ZCD Signal Generated Earlier Than the Phase B Current Crosses Zero**

By directly measuring the current flowing through the LMG3427, it is observed that the current through the LMG3427 oscillates significantly around the time the ZCD signal is generated. It is true that the LMG3427 generates the ZCD signal because of an actual zero crossing. It does not falsely generate the ZCD signal. Further analysis of the problematic timing reveals that the current flowing through phase B oscillates the moment the phase A active FET turns on, which effectively causes the current to cross zero, leading the LMG3427 to generate the ZCD signal. However, the negative inductor current is insufficient because the ZCD signal is generated prematurely, causing ZVS to disappear.


**Figure 2-3. Problematic Waveform, with the Oscillation of Current Flowing Through Phase B Causing Premature Generation of the Phase B ZCD Signal**

## 2.3 Analysis of ZCD Timing Issue Caused by Inter-phase Capacitance in TCM PFC

Figure 2-4 shows the ZCD timing issue caused by the inter-phase capacitance of the LMG3427.

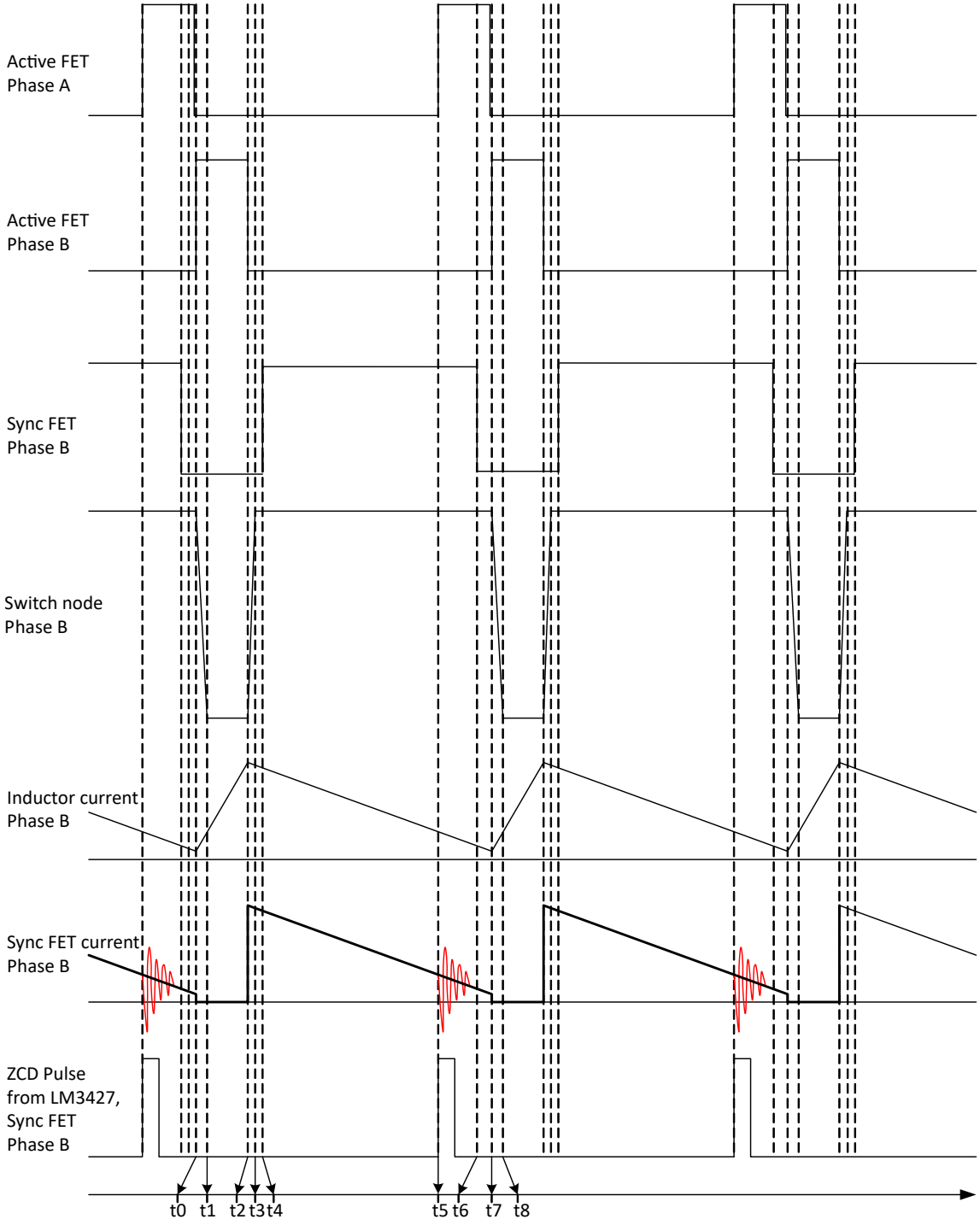


**Figure 2-4. ZCD Timing Issue**

Stage 1 (t0–t1): At t0, the phase B active FET starts conducting, and the phase B switch node voltage drops. The inductor current starts to rise linearly, and the phase B active FET begins hard commutation, at which point ZVS is lost, thereby increasing the turn-on loss.

Stage 2 (t1–t2): At t1, the hard commutation of the phase B active FET ends, at which point the phase B active FET remains on, and the inductor current continues to rise linearly.

Stage 3 (t2–t3): At t2, the phase B active FET is turned off, while the phase B sync FET stays off, and the inductor current starts to charge the Coss of the phase B active FET and also discharge the Coss of the phase B sync FET.

Stage 4 (t3–t4): At t3, the phase B sync FET is fully discharged and remains off. The inductor current starts to freewheel through the phase B sync FET, preparing for ZVS of the phase B sync FET.

Stage 5 (t4–t5): At t4, ZVS of the phase B sync FET is enabled, and the inductor current decreases linearly.

Stage 6 (t5–t6): At t5, the phase A active FET is turned on. Because there is a large inter-phase capacitance between phases A and B, at the moment the phase A active FET is turned on, a current flowing from the phase B switch node to the phase A switch node causes the current flowing through the phase B sync FET to actually cross zero, leading the LMG3427 to prematurely generate the ZCD signal to enable ZVS of phase B.

Stage 7 (t6–t7): At t6, the phase B sync FET is turned off, and the inductor current freewheels through the body diode of the sync FET. The inductor current decreases linearly, but because its direction is positive at this point, the energy stored in the Csw of the phase B active FET cannot be released, and therefore, no condition is created for ZVS of the phase B active FET.

Stage 8 (t7–t8): At t7, the phase B active FET is turned on. Due to the loss of ZVS of the phase B sync FET, the phase B switch node voltage drops, and the inductor current starts to rise linearly. The phase B active FET starts hard commutation, increasing the turn-on loss.

# 3 How to Avoid ZCD Timing Issue Caused by Inter-phase Capacitance During PCB Design

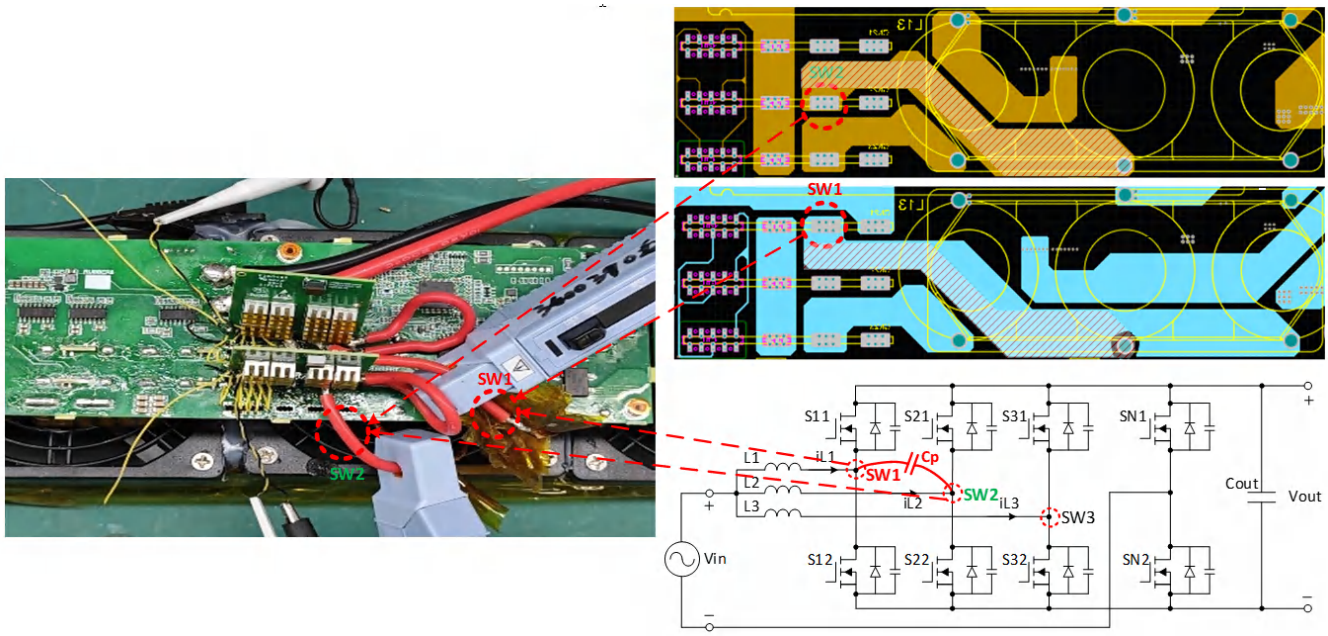


**Figure 3-1. Remove Overlap Between the First and Second Phases Using External Jumpers**

The previous analysis reveals that the oscillation in the current flowing through the phase B sync FET actually occurs at the moment phase A is turned on. Through careful analysis of the PCB, we found a large overlap between the switch nodes of phases A and B, which creates a large parasitic capacitance between them. Therefore, when the phase A active FET is turned on, the potential of the phase A switch node changes abruptly, and a large negative current charges this parasitic capacitance, causing the current flowing through the phase B sync FET to actually cross zero. This leads to the ZCD signal being generated prematurely, resulting in ZVS loss. Based on the above analysis, the problem can be solved by removing the overlap between the switch nodes of phases A and B using jumpers.

As shown in Figure 3-2, the ZCD timing issue caused by inter-phase capacitance is resolved when the overlap between phases A and B is removed using jumpers. Therefore, when using the LMG3427, PCB designers need to avoid large overlaps between the switch nodes of each phase.

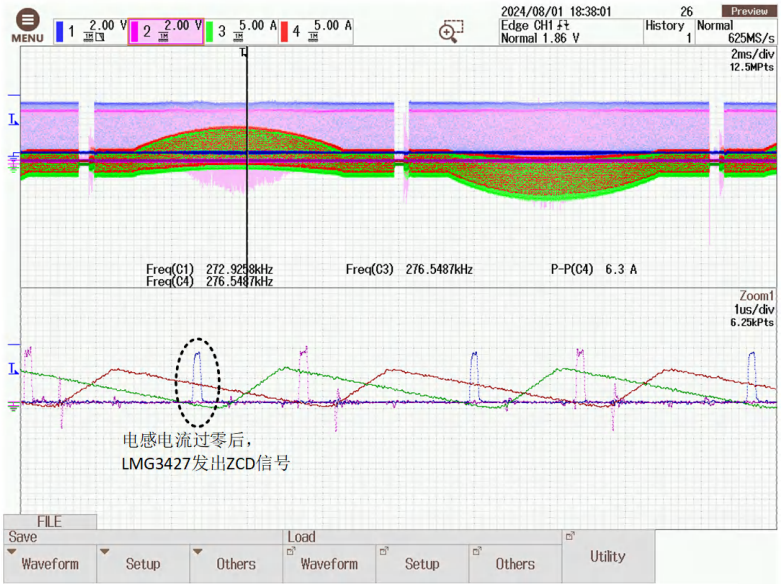


**Figure 3-2. Normal Waveform After the Overlap between Phases A and B Is Removed**

## 4 Summary

This article describes the ZCD implementation principle of the LMG3427 and its application in interleaved triangular current mode (TCM) PFCs. It presents the application timing for interleaved TCM PFCs based on the LMG3427. It also analyzes the problematic waveforms and timings of ZCD timing issues caused by inter-phase capacitance in applications. Finally, it provides related design recommendations to avoid LMG3427 ZCD timing issues caused by inter-phase capacitance in TCM PFC applications.

## 5 References

1. Ultraflat Interleaved Triangular Current Mode (TCM) Single-Phase PFC Rectifier
2. LMG3427 datasheet.

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