Application Note

Adaptive Current Control PFC Design With UCC28064A

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ABSTRACT

High-end TV and Monitor Switch-Mode Power Supplies (200-500W) commonly implement interleaved (two phase) critical conduction mode (CrCM, also called Transition mode-TM) PFC (Power Factor Correction) block, to improve efficiency and reduce design volume (height). This application note describes how to achieve higher efficiency to reduce power loss further and alleviate thermal challenge at low AC line condition without topology and power stage change. A simple external circuit is introduced here and the working principle is elaborated. Measurement shows 1-2% efficiency boost depending on the load conditions.

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Trademarks

1 Introduction

In the case of the PFC circuit block of the Switched Power supply that was designed and applied before writing this application note, the power loss difference due to FET conduction loss is large depending on the AC input voltage condition, That is, the low line voltage and the high line voltage, so the power loss in the low-voltage line is greater than that in the high-voltage line. In particular, the switching FET and the PFC inductor generate more losses than the other components. To improve this problem, the design was designed to modify the output current waveform of the AC low line by configuring an external circuit to reduce power loss to be equal to the high line and to stabilize the DC/DC operation connected to the PFC.

2 Interleaving PFC Principle of Operation

The UCC28064A device contains the control circuits for two parallel-connected boost pulse-width modulated (PWM) power converters. The boost PWM power converters ramp current in the boost inductors for a time period proportional to the voltage on the error amplifier output (COMP pin). Each power converter then turns off the power MOSFET until current in the boost inductor decays to zero (as sensed on the zero current detection inputs, ZCDA and ZCDB). After the inductor demagnetizes, the power converter starts another cycle. This cycle process produces a triangular waveform of current, with peak current set by the on-time and the instantaneous power mains input voltage, VIN(t) value, as shown in Equation 1.

$$I_{peak} = VIN \times Ton / L \tag{1}$$

The average line current is exactly equal to half of the peak line current, as shown in Equation 2.

$$I_{avg} = 1/2 \times (VIN \times Ton / L) \tag{2}$$

When the Ton and L values are essentially constant during an AC-line period, the resulting triangular current waveform during each switching cycle has an average value proportional to the instantaneous value of the rectified AC-line voltage. This architecture results in a resistive input impedance characteristic at the line frequency and a near-unity power factor

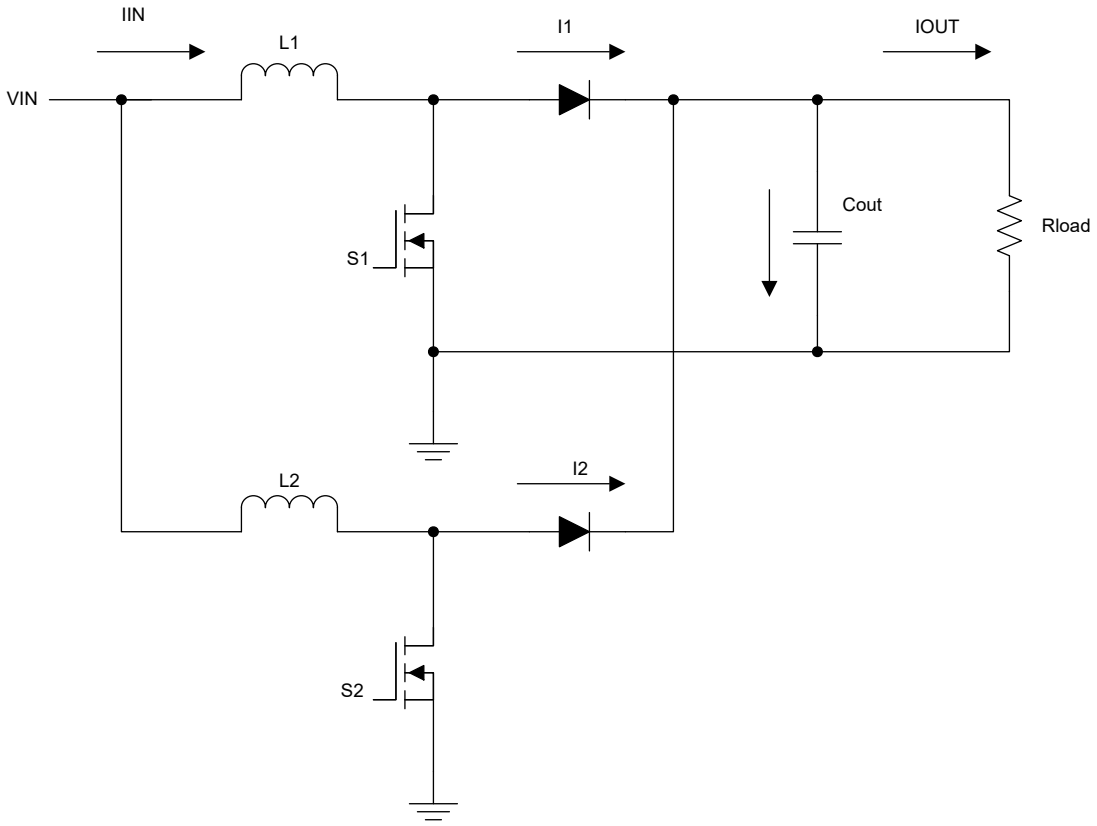


Figure 2-1. Interleaving PFC Block Introduction

3 Original PFC Design with Internal Line Feed-Forward block

Line voltage feed-forward compensation provides several benefits:

- Maintains constant bandwidth of the control loop versus line voltage variation
- Avoids high current in the MOSFET, inductors, and line filter when line increases from low to high
- Helps to keep simple phase management control

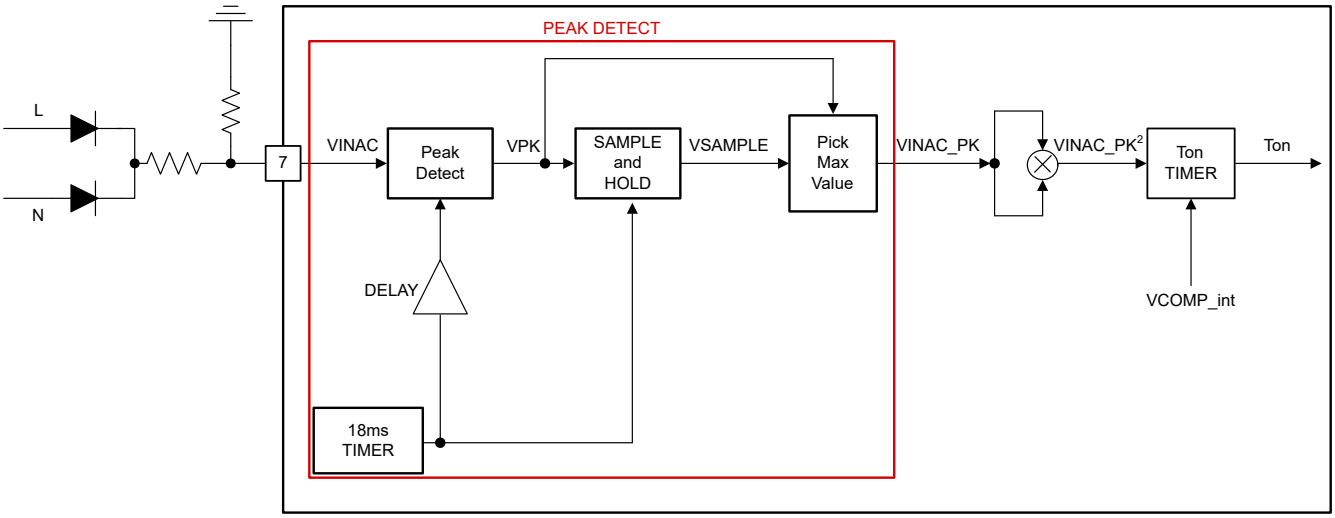


Figure 3-1. Voltage Feed Forward Function Block in UCC28064A

4 Current Phenomenon of Operating With UCC28064A Internal Line Feed Forward Function

Even though the line voltage feed-forward compensation is built-in, we wanted to implement an adaptive PFC design by configuring an external circuit to prevent the occurrence of a larger peak current than expected due to the slow response time of the PFC compensation block and the high current limit of the PFC block when line transitions from 90Vac to 264Vac and from 264Vac to 90Vac condition.

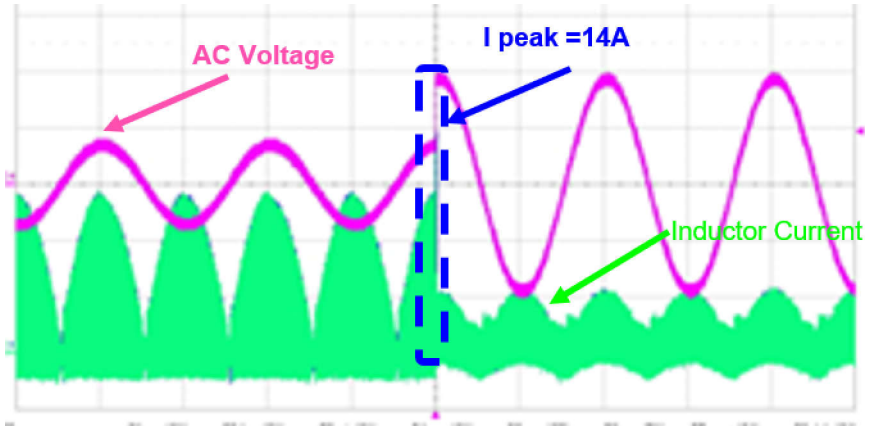


Figure 4-1. High Peak Current During 90Vac to 264Vac Line Transient

5 Achieving Adaptive Current Control PFC With UCC28064A

To implement it under AC low-line voltage and full-load, which are the conditions necessary to implement adaptive PFC performance, the apparent OCP level must be reduced. First, at low-line and max-load, set the apparent OCP level to limit peak current so that normal Vout cannot be maintained. Vout below the regulation set-point can drive VCOMP to maximum on-time but OCP level can prevent Vout regulation. When Vout falls to a target threshold (353V in this example) a comparator changes the apparent OCP level even lower and the OCP condition is locked in until either load is lighter or Vin rises.

Afterward, contrary to constant on-time control, when the switching frequency is lowered the current flows to the OCP level over the entire line cycle and the inductor current waveform changes from a sine wave envelope to a trapezoidal envelope.

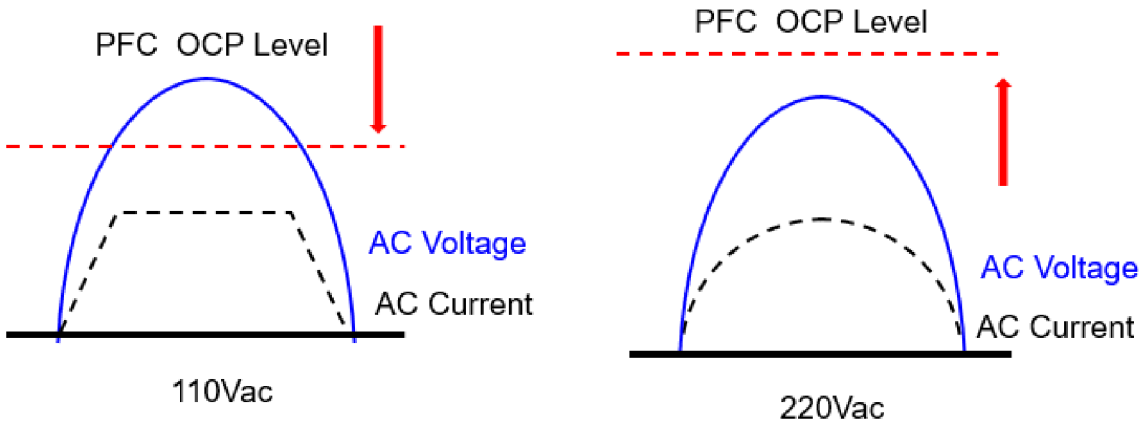


Figure 5-1. Concept to Achieving Adaptive PFC Design With OCP Level

Configure the adaptive current limit external circuit as shown in Figure 5-2 to adjust the current limit level according to the PFC output voltage.

The following list details the operating mechanism for external circuit with UCC28064A.

Using the CS pin parameter of UCC28064A, adjust the CS voltage level from -0.2V to -0.162V, limit the output power during OCP operation. For this purpose, the external circuit was configured as follows.

1. R6 and R7 set a reference voltage of 12V to the comparator (-) input. R8 and R9 form a divider to set the V_{PFCOUT} threshold to approximately 353V.
2. At higher input voltages or lower loads, the PFC output voltage can be regulated and the comparator output is high, keeping Q1 on
3. When Q1 is on, R5 is grounded and R2 and R4 form a 3kR/4kR divider across Rsense which reduces the current-sense voltage applied to the CS input by ¾. Internal CS threshold of -0.2V does not change so Rsense peak voltage must exceed -0.267V to trigger OCP
4. At low-line and max load, Rsense value is chosen so that the peak voltage triggers OCP and the peak inductor current is not high enough to sustain regulation. When V_{PFCOUT} falls below the 353V threshold, the comparator output goes low and turns Q1 off.
5. When Q1 is off, R5 is applied in series with R4 and the R2 and (R4+R5) divider forms 13kR/14kR divider across Rsense which reduces the current-sense voltage applied to the CS input by 13/14. Internal CS threshold of -0.2V does not change so Rsense peak voltage must exceed -0.215V to trigger OCP. This is a change of 0.215/0.267 = 0.808, which effectively changes the internal -0.2V OCP threshold to -0.162V. This becomes an effective hysteresis to reduce inductor peak current even more to make sure that V_{PFCOUT} stays below 353V.
6. When input voltage rises or load reduces, the OCP-limited current can allow V_{PFCOUT} to rise above 353V and the comparator drive Q1 on again and the apparent OCP limit is raised back to normal.
7. R1 and C1 are for noise filtering only and do not affect the OCP thresholds. No one knows what the purpose of R3 is, but the value is high enough that the value does not affect the OCP thresholds.

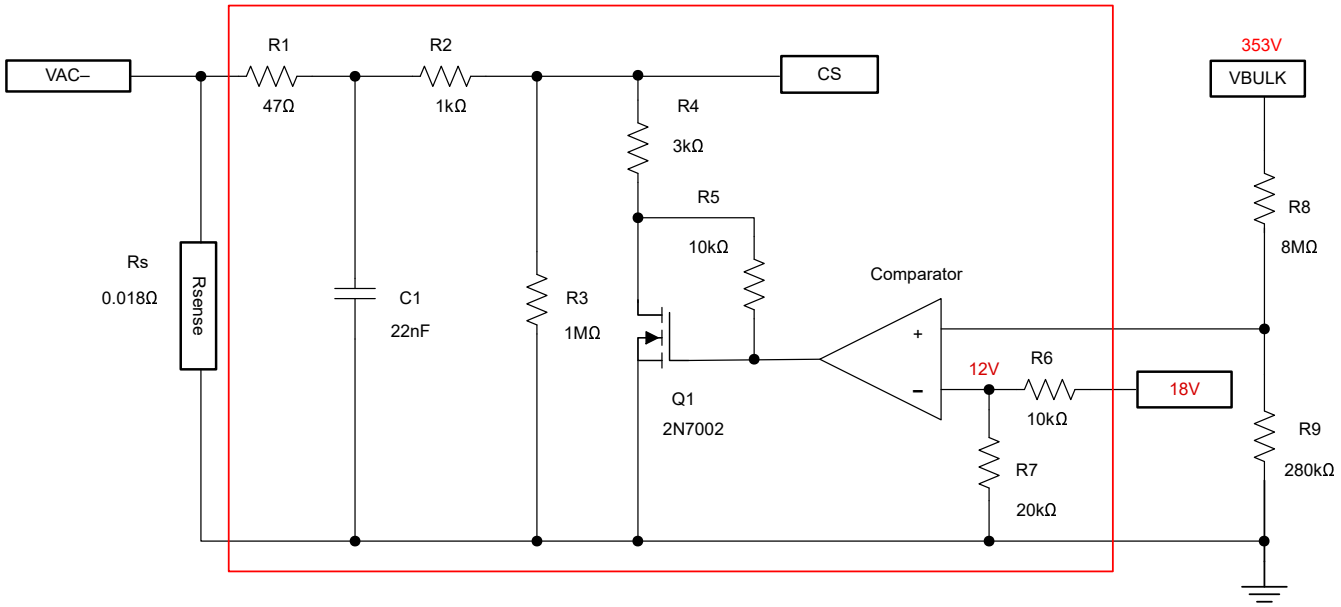


Figure 5-2. External Circuit for Adaptive Current Limit With UCC28064A

6 Test Results Comparing Original PFC Design to Adaptive PFC Design

Table 6-1 shows thermal test result with decrease temperature in PFC block components, especially PFC inductor with applying adaptive PFC external circuit design against original boost PFC design.

Table 6-1. Temperature Result Between Original PFC Design and Adaptive PFC Design

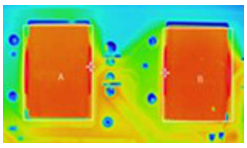
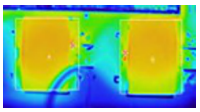
	Original Interleaved PFC	Interleaved Adaptive PFC	Remark
Inductor			
	EER3311 x 2EA	EER3311 x 2EA	
	140μH, 0.1Φx30P	140μH, 0.1Φx30P	
	71.5. °C	**62.1°C**	**10.4℃↓**
FET	56.8°C	52.7°C	**4.1℃↓**
Diode	56.5°C	52.6°C	**3.9℃↓**

Table 6-2 shows efficiency test result of increased efficiency value at total board condition when applying adaptive PFC external circuit design against original boost PFC design.

Table 6-2. Efficiency Increases With Adaptive PFC Design Over Original PFC Design

Input Voltage	**110Vac**	**230Vac**
Load	**Efficiency Improvement**	**Efficiency Improvement**
25%	1.96%	0.69%
50%	1.11%	0.61%
75%	0.88%	0.43%
100%	0.62%	0.33%

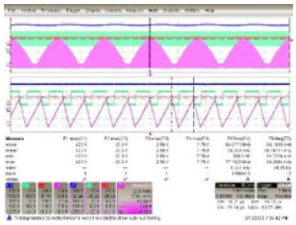
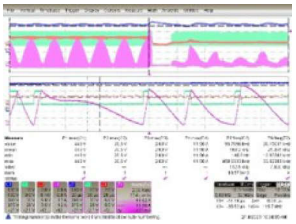
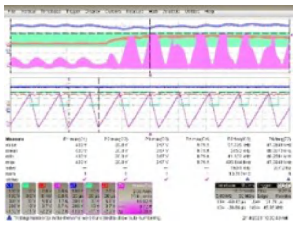
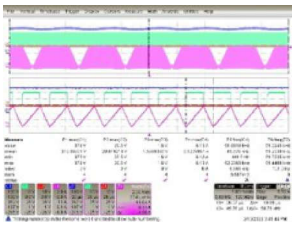
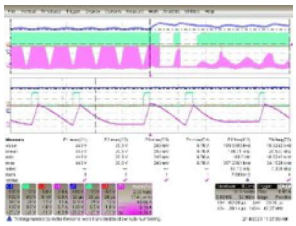
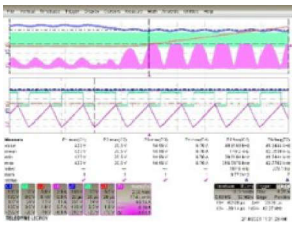
Table 6-3 shows PF(Power Factor) test result of decreased PF value at low AC input condition when applying adaptive PFC external circuit design against original boost PFC design. But the PF standard is 0.9 or higher and this standard is met even if an adaptive PFC design is applied.

Table 6-3. PF Test Result Between Original PFC Design and Adaptive PFC Design

Input Voltage	Original PFC	Adaptive PFC
90Vac	0.99	0.95
132Vac	0.99	0.95
230Vac	0.95	0.95
264Vac	0.94	0.94

Table 6-4 shows various comparison waveforms especially inductor current value with applying adaptive PFC external circuit design against original boost PFC design. As shown from the comparison waveforms, the board with adaptive PFC external circuitry has a significantly lower inductor current value than the existing circuit board.

Table 6-4. Waveforms Between Original PFC Design and Adaptive PFC Design

	Original PFC	Adaptive PFC
Max Load Operating		
	ILmax = 7.79A(Vin:90Vac,Vout:395V)	**ILmax = 6.13A(Vin:90Vac,Vout:353V)**
Normal Operating		
ILmax	**ILmax = 7.09A(Vin:90Vac,Vout:395V)**	**ILmax = 5.62A(Vin:90Vac,Vout:353V)**
Line Transient Operating (264Vac to 90Vac)		
ILmax	**ILmax = 9.71A**	**ILmax = 6.70A**

Note

CH1(Yellow) :VPFC OUT, CH2(Red): GDA, CH3(Blue): VCOMP, CH4(Green): IINDUCTOR

7 Summary

As a result of various tests and measurement of various waveforms after applying the adaptive current PFC design as above, problems such as excessive inductor current value increase and temperature rise of PFC block components during low voltage operation were improved, and we can see that the problem is solved even at 90Vac to 264Vac or 264Vac to 90Vac line transient conditions. In conclusion, the desired performance was achieved by applying adaptive current PFC external circuit.

8 References

- Texas Instruments, *UCC28064A Natural Interleaving™ Transition-Mode PFC Controller with High Light-Load Efficiency*, data sheet.

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