48-V_{IN}, 5-V_{OUT} Loadshare System Using the UCC39002 With Three PT4484 Excalibur DC/DC Modules (PR042A)

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ABSTRACT

This reference design features the UCC39002 BiCMOS 8-pin advanced load share controller and specifically illustrates equal current sharing between three PowerTrends PT4484 48 VDC to 5 VDC power modules, each rated for 20-A maximum output current, paralleled to supply a load of up to 60 A. The design uses high-side current sensing with the bias for the controllers supplied directly from the modules' output voltage. The complete list of materials, schematic, design performance curves, and Gerber file images are included.

Contents

1 Features

- High-side current sensing
- Enhanced reliability with redundancy
- Single wire load share bus
- External shut down switch for each module
- External or internal bias selection
- Less than 1% current share error at full load

2 Schematic

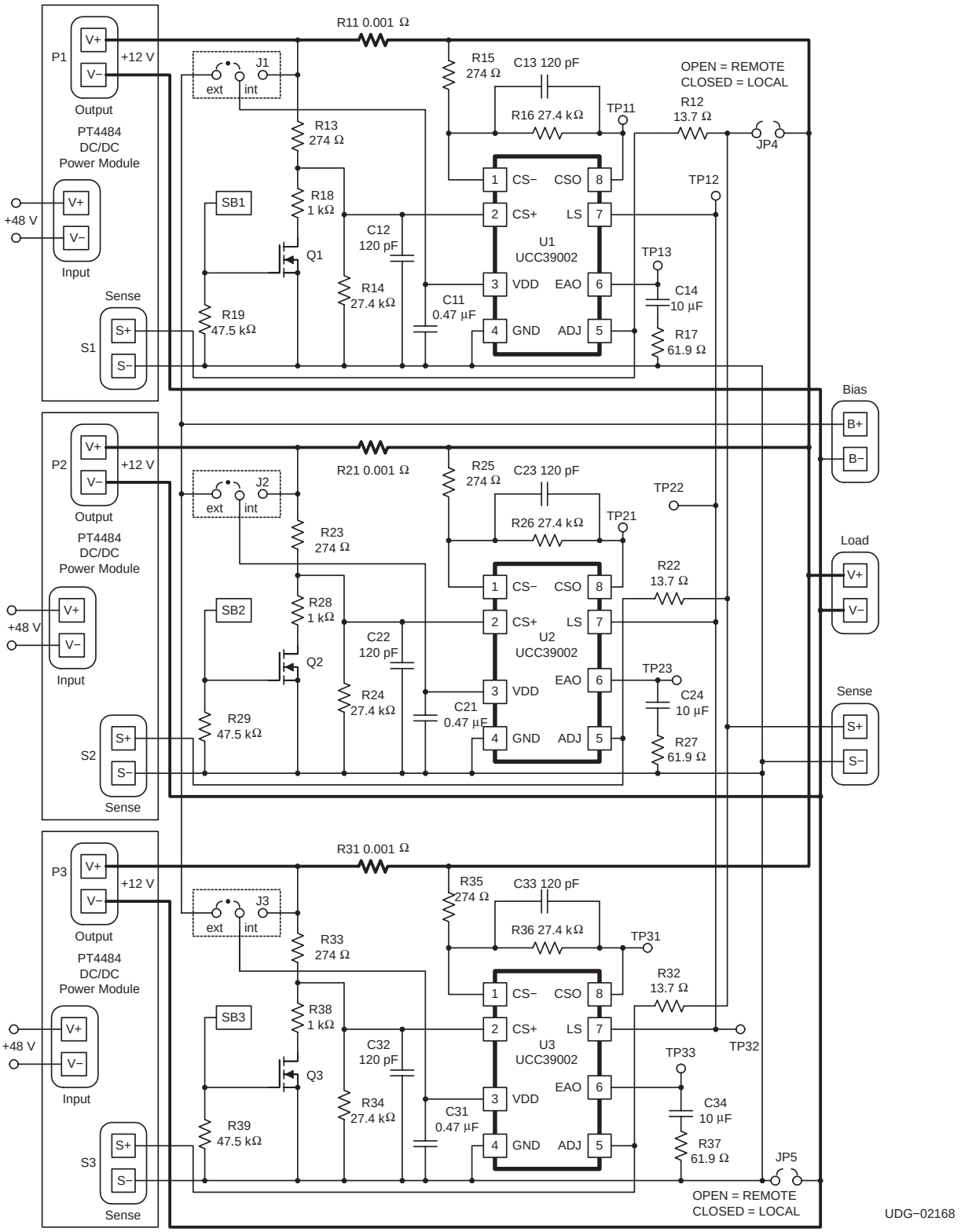

Figure 1. Three Module Load Share Application

3 Reference Design Layout

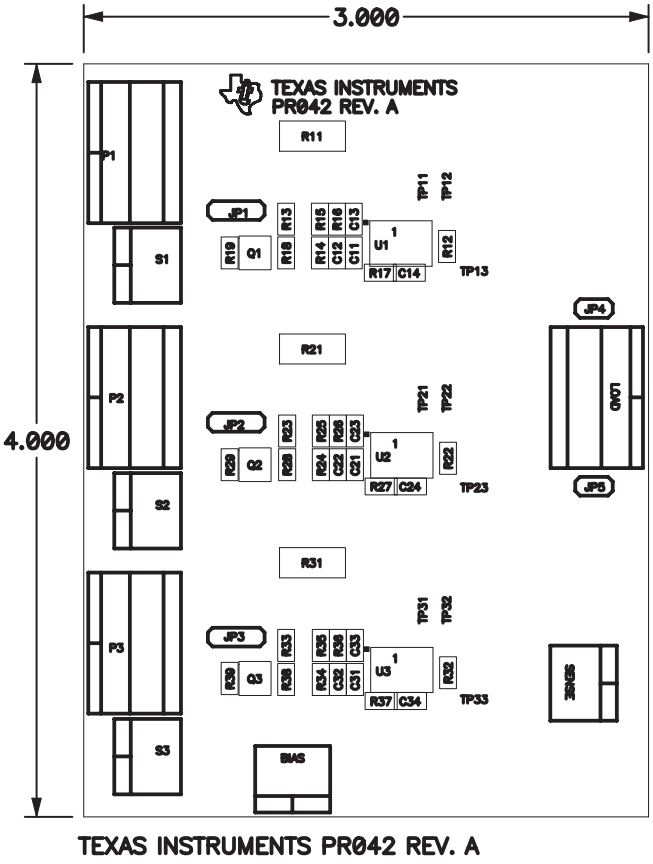

Figure 2. Top Layer Assembly

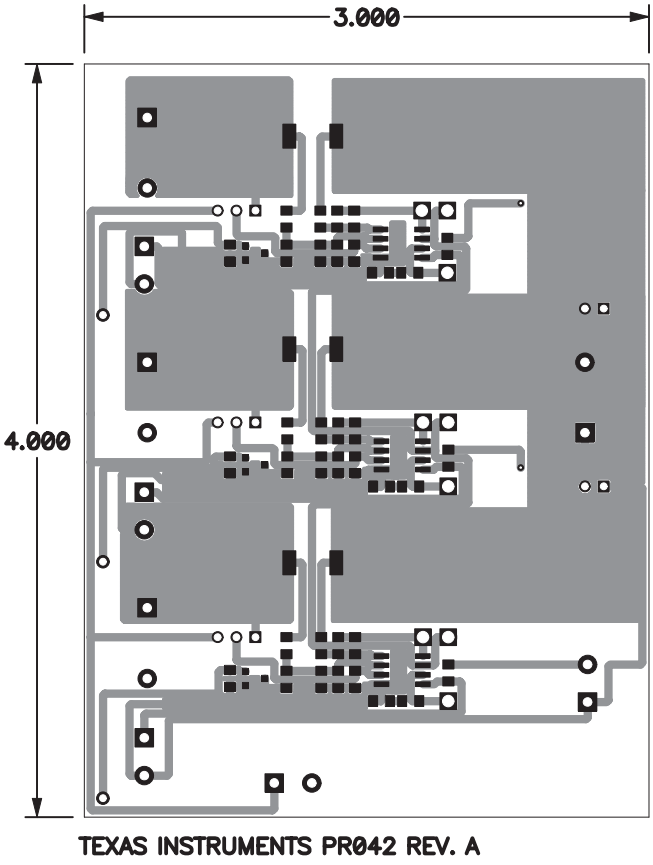

Figure 3. Top Layer

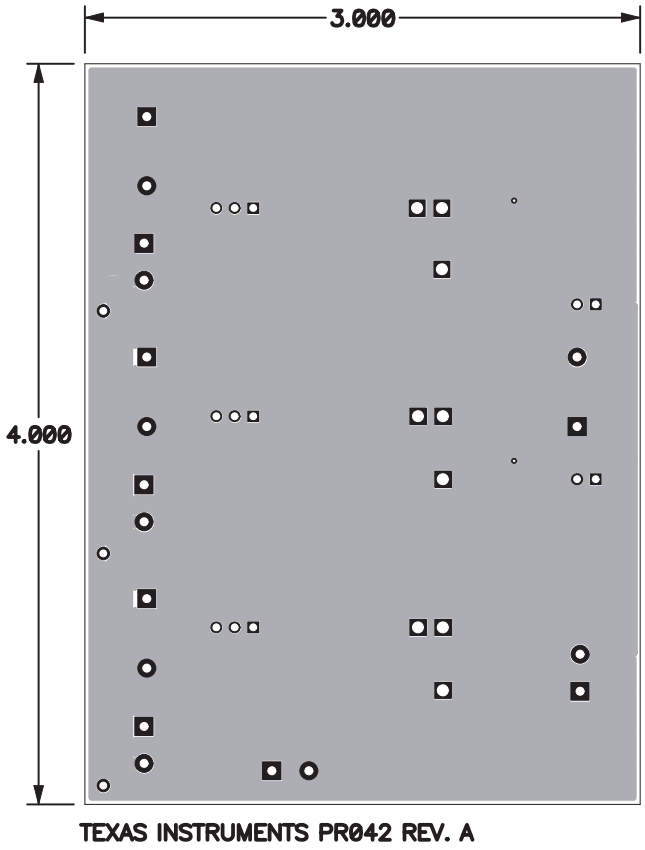

Figure 4. Bottom Layer

4 Setting Up the UCC39002 Load Share Controller

4.1 Measure the Modules

In order to accurately current share between power modules, specific parameters must be known. Among these parameters are the nominal output voltage of the modules (V_{OUT}), the maximum output current of each module ($I_{OUT(max)}$), the maximum voltage adjustment range of each module (V_{ADJ}), and the transfer function of the power modules between their positive voltage sense and power output terminals.

For this particular example:

- V_{OUT} = 5 V
- $I_{OUT(max)}$ = 20 A
- $\Delta V_{ADJ(max)}$ = 100 mV

The UCC39002 requires a bias voltage of 4.375 V to turn on, but the bias should not exceed 18 V. Due to the 5-V output of the modules, direct bias from the output voltage of the modules is possible.

- VDD = 5 V

Universal power modules have a very low bandwidth to ensure proper operation with a variety of loads. The transfer function is determined using a network analyzer and injecting a small signal across a 50-Ω resistor placed between the positive sense terminal and the positive voltage output terminal, much like measuring the control loop of a converter, as shown in Figure 5. The resultant Bode plot shows the dc gain and the unity gain crossover frequency of the module. Expect the module's crossover frequency to be within the range from 0.1 Hz to approximately 30 kHz. The desired crossover frequency for the load share loop is set at least one decade before the unity gain crossover frequency of the modules. This is accomplished by selecting the compensation components for the transconductance error amplifier as described in Section 4.5, *Error Amplifier Compensation*.

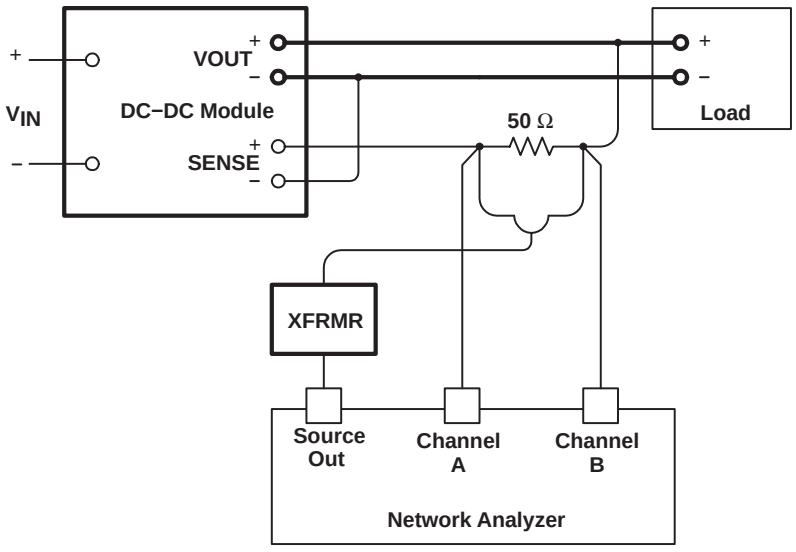

Figure 5. Measuring the Unity Gain Crossover Frequency

The unity gain crossover frequency, $f_{CO(module)}$, is measured from the power module's SENSE(+) terminal to the VOUT(+) terminal.

The resultant Bode plot of the loop gain yields a crossover frequency ($f_{CO(module)}$) of 25.6 Hz. The unity gain crossover frequency is unique to the module and must be specifically measured for each module type.

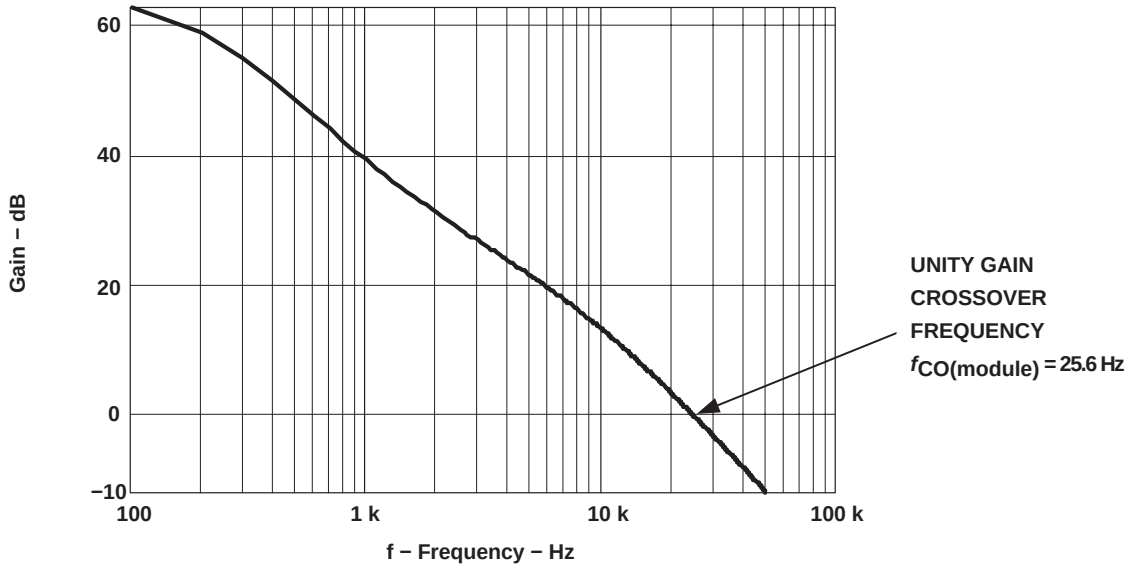

Figure 6. Power Module Bode Plot

4.2 Choosing the Sense Resistor

The primary concern in the selection of the sense resistor is to ensure that the sum of the voltage drops across the resistor and the parasitic wire impedances, at maximum module output current, is significantly less than the output voltage adjustment range of the modules, otherwise there would be no room for output voltage adjustment.

- $I_{OUT(max)} \times R_{SENSE} << \Delta V_{ADJ(max)}$

Other limitations for the sense resistor are the desired minimum power dissipation and available component ratings.

For this particular example, the power dissipation of each current sense resistor was desired to be less than 1 W:

- $R_{SENSE(max)} = P_{RSENSE} / I_{OUT(max)}^2 = 1\ W / 20\ A^2 = 2.5\ m\Omega$
- $R_{SENSE} = 1\ m\Omega$
- $P_{RSENSE} = 400\ mW$
- $I_{OUT(max)} \times R_{SENSE} = 20\ mV << \Delta V_{ADJ(max)}$

4.3 Setting the Current Sense Amplifier Gain

The gain of the current sense amplifier (CSA) is configured by adding compensation components between the inverting input to the amplifier, CS−, and the current sense amplifier output, CSO, of the load share device. The maximum voltage at the CSO pin is limited by the saturation voltage of the internal current sense amplifier and must be at least 2-V less than VDD. For this particular example, $V_{CSO(max)}$ must be less than 3 V.

- $V_{CSO(max)} < VDD - 2V$
- $V_{CSO(max)} < 5\ V - 2\ V$
- $V_{CSO\ (max)} < 3\ V$

Referring to Figure 1, the CSA gain, A_{CSA}, is equal to:

- $$A_{CSA} = \left(\frac{R16}{R15}\right) = \frac{V_{CSO}}{\left(R_{SENSE} \times I_{OUT(max)}\right)}$$

For this particular example, the A_{CSA} gain is set to 100, resulting in a voltage of 2 V at CSO. A high-frequency pole, configured with C13, is added for noise filtering. This impedance is mirrored at the non-inverting input, CS+, of the differential amplifier.

The CSA output voltage, V_{CSO}, serves as the input to the internal unity gain LS bus driver. The module with the highest output voltage forward biases the internal diode located at the output of the LS bus driver and determines the voltage on the load share bus on the LS pin, V_{LS}, making this module the master. This load share bus acts as a communication port between the paralleled modules. The LS pin is bi-directional. By forward biasing the internal diode, the master sets the LS bus voltage based upon the voltage across its current sense resistor. Because the internal diode is reverse biased on the other modules, referred to as the slaves, the LS voltage is used as the non-inverting input to the internal LS bus receiver. The master transmits the voltage signal to the slave modules so they can compare their voltages across their own current sense resistors with that of the master module. The slave modules represent a load on the bias current, I_{VDD}, of the master module due to the internal 100-kΩ resistor at the LS pin. This increase in supply current for the master module is equal to:

- $$\Delta I_{VDD} = n \times \left(\frac{V_{LS}}{100\ k\Omega}\right)$$

where *n* is equal to the number of paralleled modules.

4.4 Determining R_{ADJ}

The SENSE(+) terminal of the module is connected to the ADJ pin of the load share controller. Placing a resistor between this ADJ pin and the load, creates an artificial SENSE(+) voltage from the voltage drop across $R_{ADJ,}$ due to the current sunk by the internal NPN transistor. The voltage at the ADJ pin must be maintained at approximately 1 V above the voltage at the EAO pin. This is necessary in order to keep the transistor at the ouput of the internal adjust amplifier from saturating. To fulfil this requirement, R_{ADJ} is calculated using the following equation:

- $$R_{ADJ} \geq \frac{\left[\Delta V_{ADJ(max)} - \left(I_{OUT(max)} \times R_{SENSE}\right)\right] \times 500\ \Omega}{\left[V_{OUT} - \left(\Delta V_{ADJ(max)} - \left[I_{OUT(max)} \times R_{SENSE}\right]\right) - 1V\right]}$$

The maximum sink current for the ADJ pin, $I_{ADJ(max)}$ also limits the selection of the adjust resistor, R_{ADJ}. $I_{ADJ(max)}$ is equal to 6 mA as determined by the internal 500-Ω emitter resistor and 3-V clamp. The value of the adjust resistor, R_{ADJ}, is based upon the maximum adjustment range of the module $\Delta V_{ADJ(max)}$. This adjust resistor must be greater than or equal to the given voltage adjustment range divided by the maximum available current:

- $$R_{ADJ} \geq \frac{\left[\Delta V_{ADJ(max)} - \left(I_{OUT(max)} \times R_{SENSE}\right)\right]}{I_{ADJ(max)}}$$

By selecting a resistor that meets both of these requirements, the ADJ pin will be at least 1-V greater than the error amplifier output voltage (V_{EAO}) and the adjust pin sink current will not exceed it's 6-mA maximum.

4.5 Error Amplifier Compensation

For this design, the total load share loop is configured for a unity gain crossover frequency f_{CO} two decades before $f_{CO(module)}$. Compensation of the transconductance error amplifier is done by placing the compensation resistor, R_{EAO} shown as R17 in Figure 1, and capacitor, C_{EAO} shown as C14 in Figure 1, between EAO and GND. The values of these components is determined by the following loop gain equation.

- $$C_{EAO} = \left(\frac{g_M}{\pi f_{CO}}\right)\left(A_{CSA}\right)\left(A_V\right)\left(A_{ADJ}\right)\left(A_{PWR(fco)}\right)$$

Where:

- g_M is the transconductance of the error amplifier, typically 14 mS,
- f_{CO} is equal to the desired crossover frequency in Hz of the load share loop, equal to $f_{CO(module)}$/100,
- A_{CSA} equals R16/R15,
- A_V is the voltage gain, equal to R_{SENSE}/R_{LOAD},
- A_{ADJ} is the gain associated with the adjust amplifier, equal to R_{ADJ}/500 Ω, and
- $A_{PWR(fco)}$ is the measured gain of the power module at the desired load share crossover frequency, converted from dB to V/V

Once the C_{EAO} capacitor is determined, R_{EAO} is selected to achieve the desired loop response

$$R_{EAO} = \frac{1}{\left[2\pi\left(C_{EAO}\right)\left(f_{CO}\right)\right]} \quad (1)$$

4.6 Other Circuitry

Referring to Figure 1, R18, R19, and Q1 provide remote disconnect. By injecting a high signal onto SB2, Q1 is turned on, shorting CS+ to ground, disabling the load share controller for that module.

5 Test Results

Following the procedure described in this reference design, three dc-to-dc modules are paralleled. The list of materials and complete schematic, along with the board layout are included. Figure 7 shows the Bode plots for the dc-to-dc module, the open loop load share circuitry, and the total combined loop gain. Figure 8 displays the individual output currents measured from each module as a function of the total load current. Figure 9 shows the load share error is minimal at full load. At light load, internal offset voltages and small signal measurement error have a more pronounced effect, contributing to a larger current distribution error, as expected.

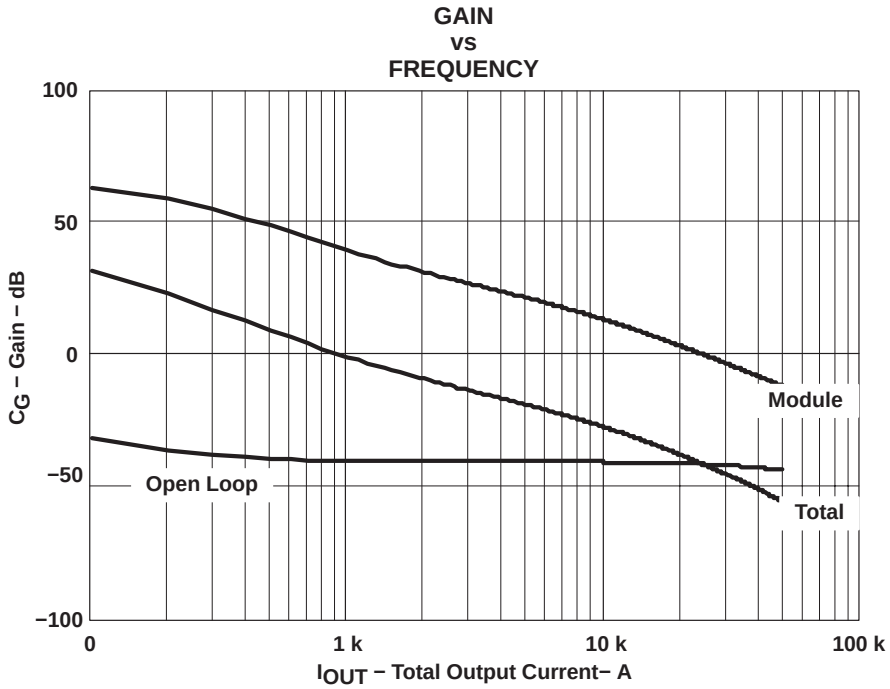

Figure 7.

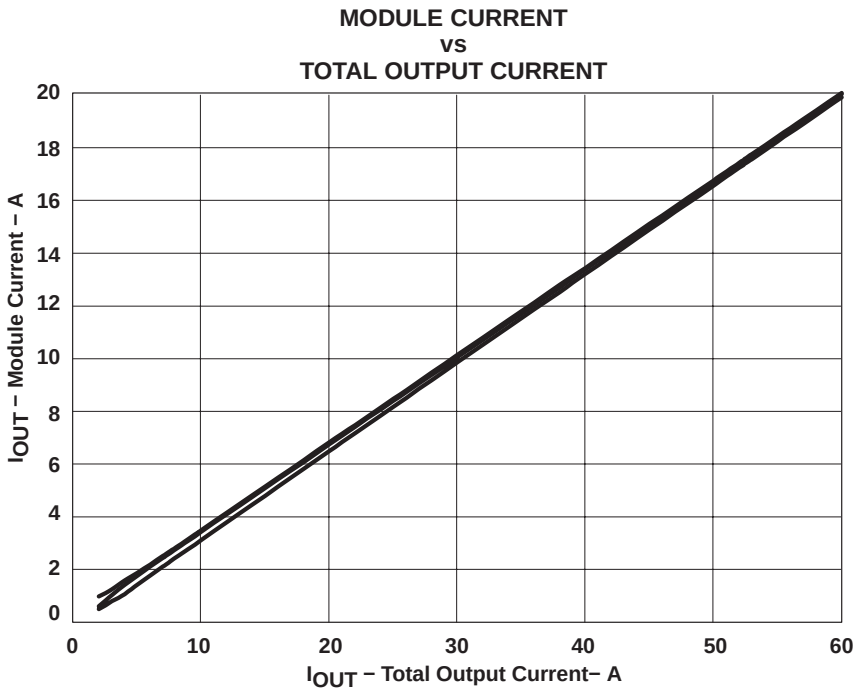

Figure 8.

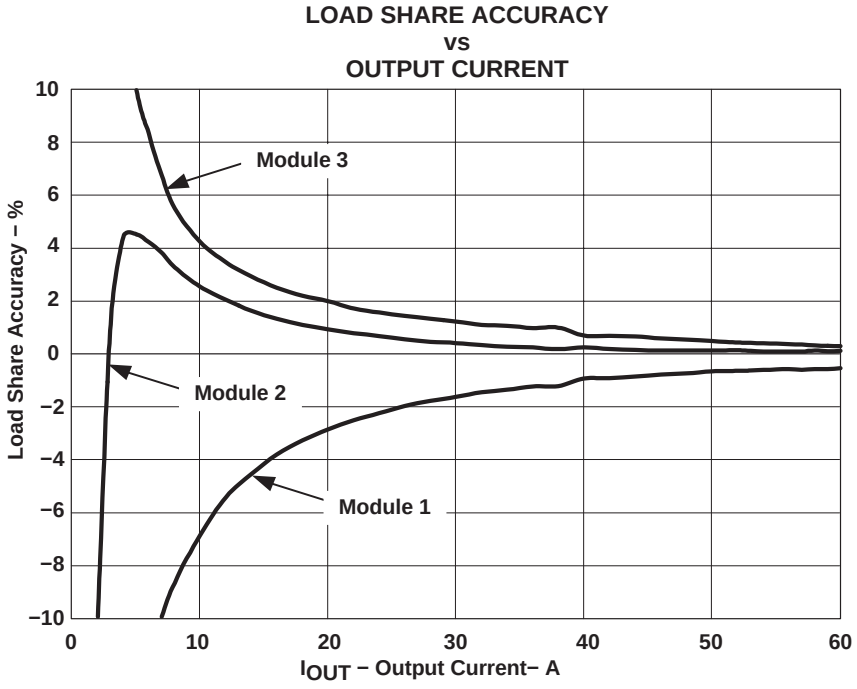

Figure 9.

6 List of Materials

Table 1 lists the board components and their values, used in the reference design.

Table 1. List of Materials

	QTY	REFERENCE	DESCRIPTION	MFG	PART NUMBER
Capacitor	3	C11, C21, C31	Ceramic, 0.47 µF, ±10%, 25 V, X7R	Kemet	C0805C474K3RAC
	6	C12, C22, C32, C13, C23, C33	Ceramic, 120 pF, ±5%, 50 V, NPO, 0805	Panasonic	ECJ−2VC1H121J
	3	C14, C24, C34	Ceramic, 10 µF, ±20%, 16 V, X7R, 1206	Panasonic	ECJ−3YB1C106M
Integrated Circuit	3	U1, U2, U3	Advanced load share controller, SO−8	Texas Instruments	UCC39002D
Resistor	3	R11, R21, R31	Thick film, 0.001 Ω, 1 W, ±1%, 2512	Vishay−Dale	WSL−2512−0.001
	3	R12, R22, R32	Thick film, 13.7 Ω, ±5%, 1/10 W, 0805	Panasonic	ERJ−6ENF13R7V
	6	R13, R23, R33, R15, R25, R35	Thick film, 274 Ω, ±1%, 1/10 W, 0805	Panasonic	ERJ−6ENF2740V
	6	R14, R24, R34, R16, R26, R36	Thick film, 27.4 kΩ, ±1%, 1/10 W, 0805	Panasonic	ERJ−6ENF2742V
	3	R17, R27, R37	Thick film, 61.9 Ω, ±1% , 1/10 W, 0805	Panasonic	ERJ−6ENF61R9V
	3	R18, R28, R38	Thick film, 1.0 kΩ, ±5%, 1/10 W, 0805	Panasonic	ERJ−6GEYJ102V
	3	R19, R29, R39	Thick film, 47.5 kΩ, ±1%, 1/10 W, 0805	Panasonic	ERJ−6ENF4752V
Terminal Block	3	P1, P2, P3	High-current (10 A) screw type terminal block (or similar)	Weidmuller	LM5.00/9.0
	3	S1, S2, S3	2 pos. 5.08 mm spacing, low current (signal) screw type (or similar)	Phoenix Contact	1730612
Transistor	3	Q1, Q2, Q3	N-channel, 60 V, 115 mA, SOT−23	ON Semiconductor	2N7002LT1
Terminals and Connectors	3	J1, J2, J3	64 pin strip, cut to 3 pins per assembly, gold plate, 0.024” tail, 0.030” pin (0.028” hole)	Mill−Max	800−10−064−10−001
	5	J1, J2, J3, J4, J5 mates	5 sockets per assembly, gold plate	Mill−Max	801−93−050−10−001
Test Point	9	TP11, TP12, TP13, TP21, TP22, TP23, TP31, TP32, TP33	White 0.063 inch diameter, 1.6 mm, 5012	Keystone	

7 References

1. Balogh, Laszlo, *The UCC3902 Load Share Controller and It’s Performance in Distributed Power*, TI Literature No. SLUA128
2. Dinwoodie, Lisa, *48-V_{IN}, 12-V_{OUT} Loadshare System Using the UCC39002 with Three DC/DC Modules*, TI Literature No. SLUA270.
3. *Advanced 8-Pin Load Share Controller*, TI Literature No. SLUS495B

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