Using the TPS40090EVM-001

User's Guide

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It is important to operate this EVM within the input voltage range of 0 Vdc to100 Vdc.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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TPS40090 Multi-Phase Buck Converter Steps-Down from 12-V to 1.5-V at 100 A

Systems Power

Contents

1 Introduction

The TPS40090EVM−001 multi-phase dc-to-dc converter utilizes the TPS40090 multi-phase controller and UCC27222 predictive gate driver to step down a 12-V input to 1.5-V at 420 kHz. The output current is 100 A. The TPS40090 provides fixed-frequency, peak current-mode control with forced-phase current balancing. Phase currents are sensed by the voltage drop across the DC resistance (DCR) of inductors. Other features include a single voltage operation, true differential output voltage sense, user programmable current limit, capacitor-programmable soft-start and a power good indicator. Device operation is specified in the TPS40090 datasheet[1].

2 Features

Table 1. TPS40090EVM−001 Performance Summary

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range		10.5	12.0	14.5	V
Output voltage set point		1.477	1.508	1.540	V
Output current range	V_{IN} = 12 V	0	100	120	A
Line regulation(1)	I_{OUT} rising from 10 A to 100 A, 8 V ≤ V_{IN} ≤ 14 V		±0.1%		
Load regulation	I_{OUT} rising from 10 A to 100 A		±0.3%		
Load transient response voltage change	I_{OUT} rising from 10 A to 100 A		−160		mV_{PK}
	I_{OUT} falling from 100 A to 10 A		200		mV_{PK}
Load transient response recovery time	I_{OUT} rising from 10 A to 100 A		< 10		µs
	I_{OUT} falling from 100 A to 10 A		< 15		µs
Loop bandwidth	I_{OUT} = 100 A, I_{OUT} = 10 A		89		kHz
Phase margin	I_{OUT} = 100 A		50		°
	I_{OUT} = 10 A		52		°
Input ripple voltage			80	200	mV_{PK}
Output ripple voltage			6	10	mV_{PK}
Output rise time					ms
Operating frequency		370	415	455	kHz
Full load efficiency	V_{IN} = 12 V, V_{OUT} = 1.5 V, I_{OUT} = 100 A		86.6%		
Current sharing tolerance	V_{IN} = 12 V, V_{OUT} = 1.5 V, I_{OUT} = 100 A		±5%	±10%	

3 Schematic

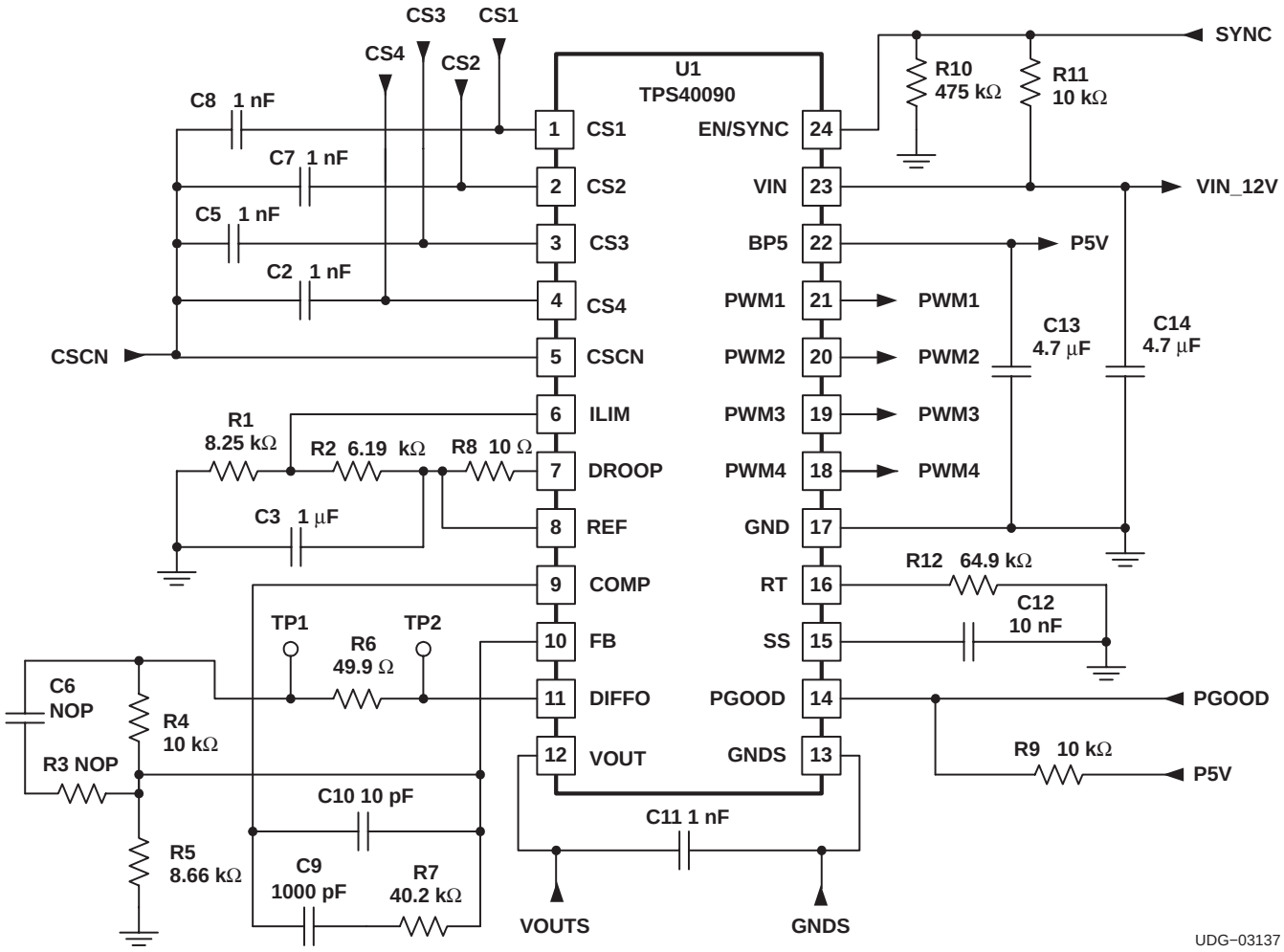


Figure 1. HPA026 Schematic Part 1 − TPS40090 Controller

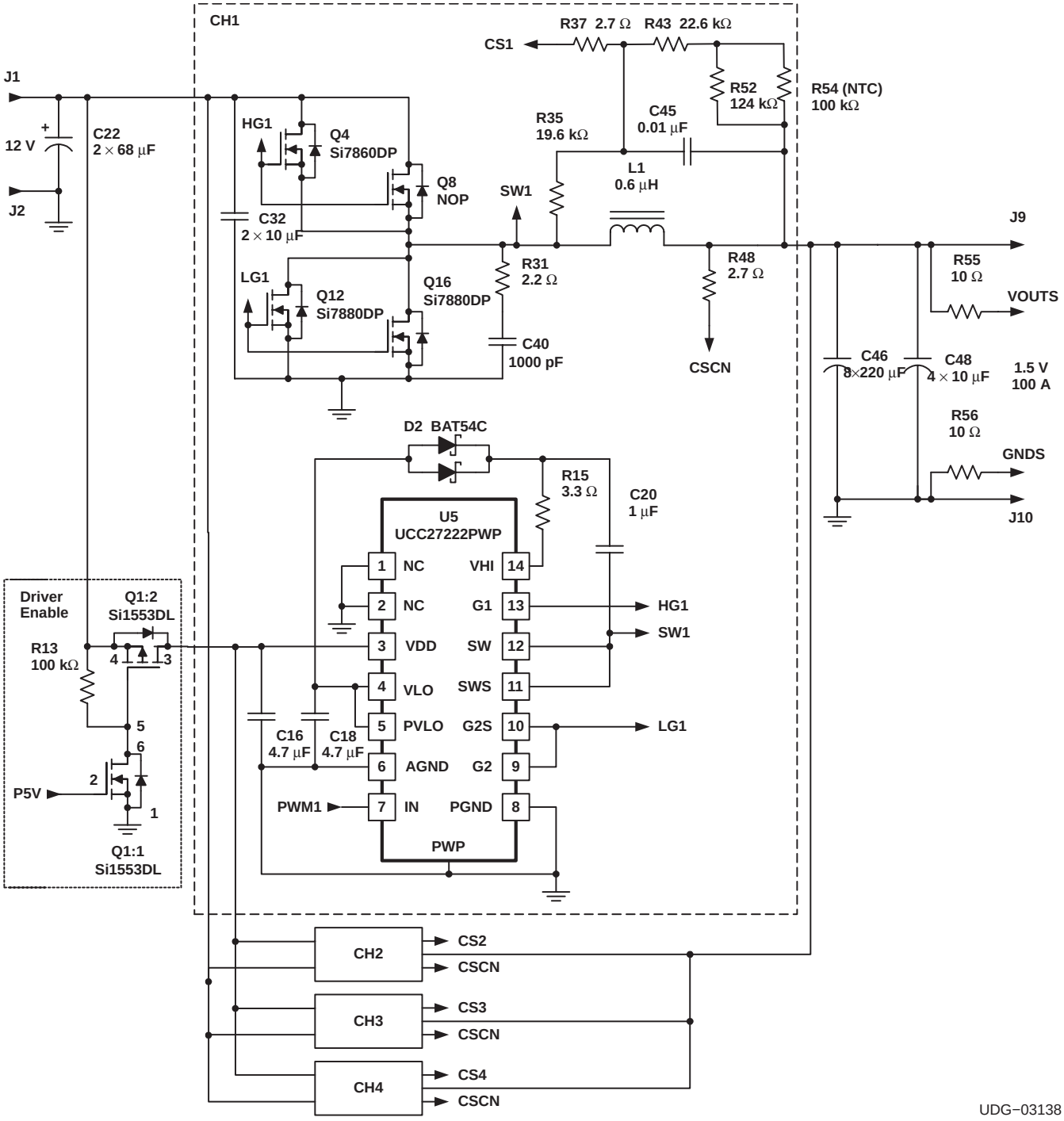


Figure 2. HPA026 Schematic Part 2 − Power Stage and Driver Circuit

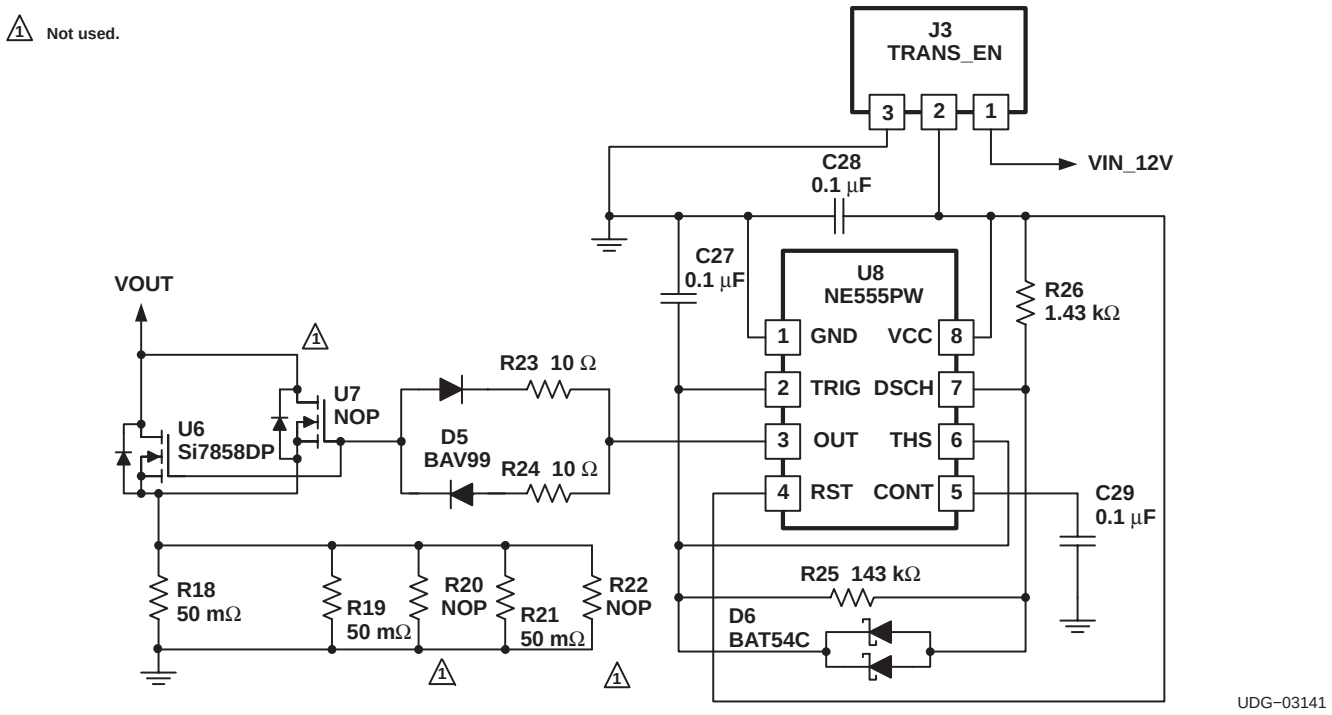


Figure 3. HPA026 Schematic Part 3 − Load Transient Generator

4 Component Selection

4.1 Frequency of Operation

The clock oscillator frequency for the TPS40090 is programmed with a single resistor from RT (pin 16) to signal ground. Equation (1) from the datasheet allows selection of the R_T capacitor in kΩ for a given switching frequency in kHz.

$$R_T = R12 = K_{PH} \times \left(39.2 \times 10^3 \times f_{PH}^{-1.041} - 7\right) (k\Omega) \quad (1)$$

where

- K_{PH} is the coefficient that depends on the number of active phases
- f_{PH} is the single phase frequency, in kHz
- for 2-phase and 3-phase configurations K_{PH}=1.333
- for 4-phase K_{PH}=1.0 is a single phase frequency, kHz.

The R_T resistor value is returned by the last expression in kΩ. For 420 kHz, R_T is calculated as 65.8 kΩ and a resistor with a 64.9-kΩ standard value is used.

4.2 Inductance Value

The output inductor value for each phase can be calculated from the volt-second during off time, shown in equation (2).

$$L = \frac{V_{OUT}}{f \times I_{RIPPLE}} \times \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) \quad (2)$$

where

- I_{RIPPLE} is usually chosen to be between 10% and 40% of maximum phase current $I_{PH(max)}$.

With I_{RIPPLE} = 20% of $I_{PH(max)}$, there is a ripple current of 5 A, and the inductance value is found to be 0.63 µH. Using SPM12550−R62M300 inductors from TDK, each had inductance of 0.6µH and resistance of 1.75-mΩ.

In multi-phase high current buck converter design, due to the ripple cancellation factor from interleaving, the inductor value could be smaller than that in a single phase operation. But from conduction loss point of view, the inductor value tends to be big to reduce the ripple current, thus losses. So there is a trade off.

4.3 Input Capacitor Selection

The bulk input capacitor selection is based on the input voltage ripple requirements. Due to the interleaving of multi phase, the input RMS current is reduced. The input ripple current RMS value over load current is calculated in equation (3).

$$\Delta I_{IN(nom)}\left(N_{PH}, D\right) = \quad (3)$$

$$\sqrt{\left[\left(D - \frac{k\left(N_{PH}, D\right)}{N_{PH}}\right) \times \left(\frac{k\left(N_{PH}, D\right) + 1}{N_{PH}} - D\right)\right] + \left(\frac{N_{PH}}{12 \times D^2}\right) \times \left[\frac{V_{OUT} \times (1 - D)}{L \times f \times \left(I_{OUT}\right)}\right]^2 \times \left[\left(k\left(N_{PH}, D\right) + 1\right)^2 \times \left(D - \frac{k\left(N_{PH}, D\right)}{N_{PH}}\right)^3 + k\left(N_{PH}, D\right)^2 \times \left(\frac{k\left(N_{PH}, D\right) + 1}{N_{PH}} - D\right)^3\right]}$$

where

- $k\left(N_{PH}, D\right) = \text{floor}\left(N_{PH} \times D\right)$
- floor(x) is the function to return the greatest integer less than or equal to x
- N_{PH} is the number of active phases

Figure 4 shows the input ripple current RMS value over the load current versus duty cycle with different number of active phases.

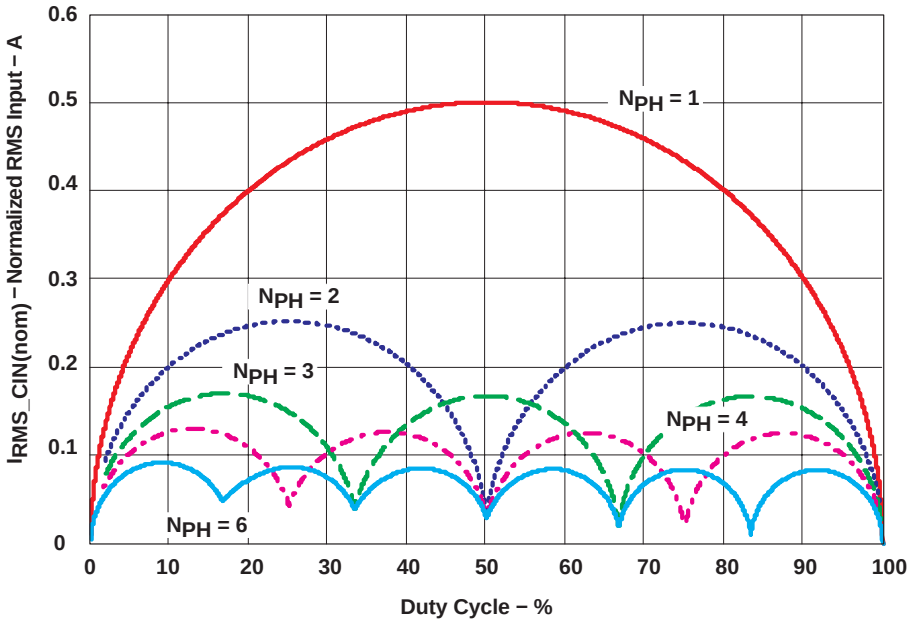


Figure 4. Input Ripple Current RMS Value Overload Current

The maximum input ripple RMS current can be estimated as shown in (4).

$$I \cong I_{OUT} \times \Delta I_{IN(nom)}\left(4,\ D_{min}\right) = 3.18\ A \tag{4}$$

It is also important to consider a minimum capacitance value which limits the voltage ripple to a specified value if all the current is supplied by the onboard capacitor. For a typical ripple voltage of 150 mV the maximum ESR is calculated in (5) as:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{150\ mV}{3.18\ A} = 47\ m\Omega \tag{5}$$

Two 68-µF, 20-V Oscon capacitors (20SVP68M) from Sanyo are placed on the input side of the board. The ESR is 40 mΩ for each capacitor.

4.4 Output Ripple Cancellation and Capacitor Selection

Due to the interleaving of channels, the total output ripple current is smaller than the ripple current from a single phase. The ripple cancellation factor is expressed in equation (6).

$$\Delta I_{OUT}\left(N_{PH}, D\right) = \frac{\left(\prod_{i=1}^{N_{PH}} \left|i - N_{PH} \times D\right|\right)}{\left[\prod_{i=1}^{N_{PH}-1} \left(\left|i - N_{PH} \times D\right| + 1\right)\right]} \tag{6}$$

$$k\left(N_{PH}, D\right) = \text{if}\left(N_{PH} \le 1,\ \Delta I_{OUT}(D),\ \Delta I_{OUT}\left(N_{PH},\ D\right)\right)$$

where

- D is the duty cycle for a single phase
- N_{PH} is the number of active phases
- K (N_{PH}) is the intermediate function for calculation

In this case, N_{PH}=4 and D_{min}=0.107 which yields k=0.573.

The actual output ripple is calculated in equation (7)

$$I_{RIPPLE} = \frac{V_{OUT}}{L \times f} \times K(N_{PH}, D) = \frac{1.5\ V}{0.6\mu\ H \times 420\ kHz} \times 0.573 = 3.41\ A \quad (7)$$

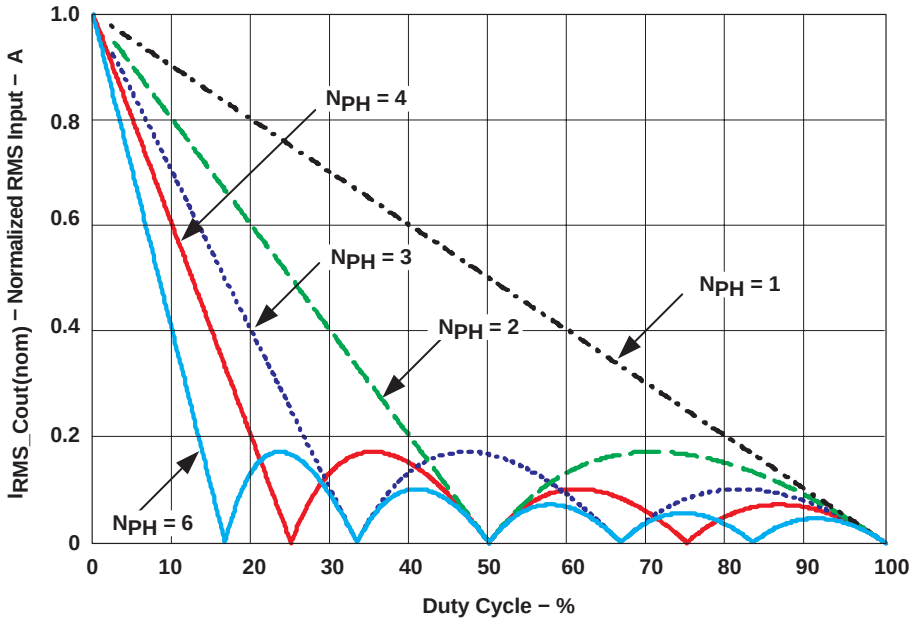


Figure 5. Input Ripple Current RMS Value Overload Current

Selection of the output capacitor is based on many application variables, including function, cost, size, and availability. There are three ways to calculate the output capacitance.

1. The minimum allowable output capacitance is determined by the amount of inductor ripple current and the allowable output ripple, as given in equation (8).

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} = \frac{3.41\ A}{8 \times 420\ kHz \times 10\ mV} = 101\ \mu F \quad (8)$$

   In this design, $C_{OUT(min)}$ is 101-µF with V_{RIPPLE}=10 mV. However, this affects only the capacitive component of the ripple voltage, and the final value of capacitance is generally influenced by ESR and transient considerations.

2. ESR limitation. (To limit the ripple voltage to 10 mV, the capacitor ESR should be less than the value calculated in equation (9)).

$$R_C <= \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{10\ mV}{3.41\ A} = 2.93\ m\Omega \quad (9)$$

3. Transient consideration. An additional consideration in the selection of the output inductor and capacitance value can be derived from examining the transient voltage overshoot which can be initiated with a load step from full load to no load. By equating the inductive energy with the capacitive energy the equation (10) can be derived.

$$C_{OUT} = \frac{L \times I^2}{V^2} = \frac{L_{EQ} \times \left(\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right)}{\left(V_{OUT2}\right)^2 - \left(V_{OUT1}\right)^2} = \frac{\frac{0.6\mu H}{4} \times (100\ A)^2}{\left((1.75\ V)^2 - (1.5\ V)^2\right)} = 1846\ \mu F \quad (10)$$

where

- I_{OH} is full load
- I_{OL} is no load,
- V_{OUT2} is the the allowed transient voltage rise
- V_{OUT1} is the initial voltage

In this 100-A design the capacitance required for limiting the transient is significantly larger than the capacitance required to keep the ripple acceptably low. Eight 220-µF POSCAP capacitors are in parallel with four 22-µF ceramic capacitors. The ESR of each POSCAP is 15mΩ.

4.5 MOSFET Selection

There are different requirements for switching FET(s) and rectifier FET(s) in the high-ratio step down application. The duty cycle is around 12%. So the rectifier FET(s) is on for most of the cycle. The conduction loss is dominant. Low-$R_{DS(on)}$ FET(s) are preferred. Also due to the dV/dt turn on of the rectifier FET(s) and cross conduction, choose a rectifier FET with Qgs > Qgd. When the switch node is falling, the Qgd can pull the gate of the lower FET below GND, which upsets the driver. Two Si7880DP from Siliconix are in parallel for the rectifier FET. The $R_{DS(on)}$ of this FET is 3 mΩ and Qgs=18nC, and Qgd=10.5nC.

The switching FET switches at high voltage and high current, the switching loss is dominant. One single Si7860DP is selected for its low total gate charge.

Both types of FET(s) are offered in the Powerpak SO−8 package.

The PCB is layed out for two FETs in parallel, for both switching FET(s) and rectifier FET(s), to give the feasibility to modify the board for different applications.

4.6 Current Sensing

TPS40090 supports both resistor current sensing and DCR current sensing approach. DCRs of the output inductors are used in this design as the current sensing components. The DCR current sensing circuit is shown in Figure 5. The idea is to parallel a R-C network to the inductor. If the two time constants are same (L/DCR=R × C), then V_C=V_{DCR}. Extra circuit, shown in (b), is used to compensate the positive temperature coefficient of copper specific resistance, which is 0.385%/°C. See detail explanation in the datasheet.

With the chosen inductor described in *Inductance Value*, (section 4.2, of this document) the following values are used.

- R=19.6 kΩ
- C=10 nF
- R_{NTC}=100 kΩ
- R1=124 kΩ
- R2=22.6 kΩ

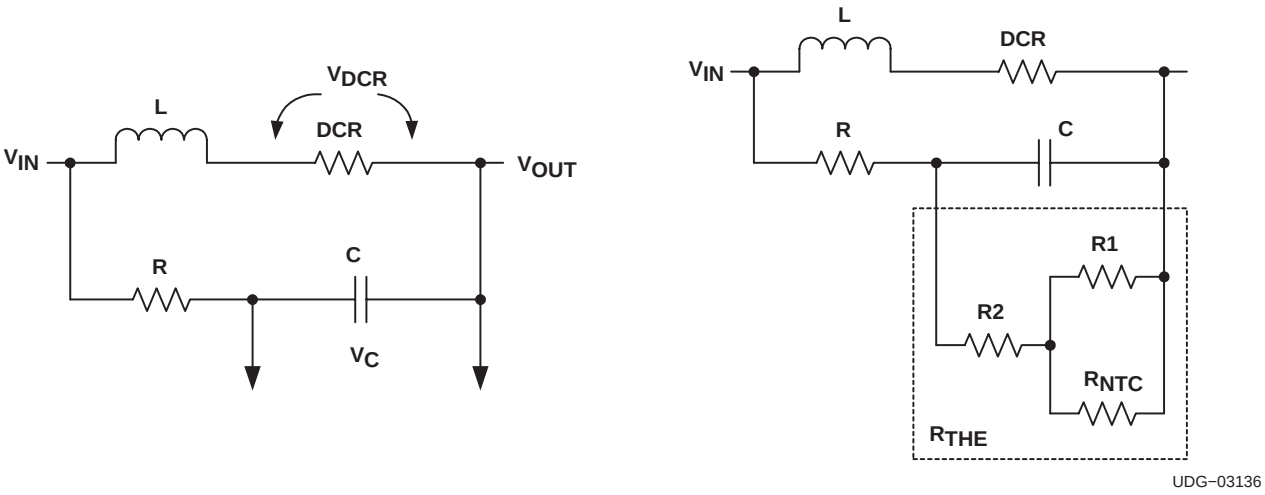


Figure 6. DCR Current Sensing Circuit with Copper Temperature Compensation

4.7 Overcurrent Limit Protection

The overcurrent function monitors the voltage level separately on each current sense input and compares it to the voltage on ILIM pin set by the divider from the controller's reference.

If the threshold of $V_{ILIM}/2.7$ is exceeded, the PWM cycle on the respected phase is terminated. Voltage level on the ILIM pin is determined by (11).

$$V_{ILIM} = 2.7 \times I_{PH(max)} \times R_{CS}; \quad I_{PH(max)} = I_{OUT} + \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{2 \times L_{OUT} \times f_{SW} \times V_{IN}} \tag{11}$$

where

- $I_{PH(max)}$ is the maximum allowable value of the phase current
- R_{CS} is the value of the current sense resistor

4.8 Compensation Components

The TPS40090 uses peak current mode control. Type II network is used here, which is implemented to provide one zero and two poles. The first pole is placed at the origin to improve DC regulation.

The ESR zero of the power stage is:

$$f_{ESRZ} = \frac{1}{2\pi \times R_C \times C_{OUT}} = 354 \text{ kHz} \quad (12)$$

The zero is placed near 3.96 kHz to produce a reasonable time constant.

$$f_Z = \frac{1}{2\pi \times R11 \times C11} \quad (13)$$

The second pole is placed at ESR zero (354 kHz).

$$f_{P1} = \frac{1}{2\pi \times R11 \times \left(\frac{(C11 \times C12)}{(C11 + C12)}\right)} \quad (14)$$

The resulting values selected for this design are:

- R11 = 40.2 kΩ
- C11 = 1000 pF
- C12 = 10 pF

4.9 Droop Function

Resistor R8, which is connected from DROOP (pin 7) to REF (pin 8), is used to program the droop function. See the datasheet for details. A 10-Ω resistor is used for R8 on the board. If droop function is required, R8 needs to be modified according to the required droop voltage. R8 can be calculated from the following equation.

$$R8 = \frac{2500\, N_{PH} \times V_{DROOP}}{I_{OUT} \times R_{CS}} \times \frac{V_{REF}}{V_{OUT}} = \frac{2500\, N_{PH} \times V_{DROOP}}{V_{CS1} + V_{CS2} + V_{CS3} + V_{CS4}} \times \frac{R2}{R1 + R2} \quad (15)$$

where

- V_{DROOP} is the allowed output voltage droop at full load output current
- R_{CS} is the current sensing resistor and
- N_{PH} is the number of active phases

5 Test Results/Performance Data

5.1 Efficiency and Power Loss

Figure 7 shows the efficiency as the load varies from 10 A to over 100 A. Efficiency curves with L_{OUT}=0.6-µH and L_{OUT}=0.3-µH are compared. The efficiency at full load is about 86.6% with L_{OUT}=0.6-µH and 86% with L_{OUT}=0.3-µH.

Figure 8 shows the total loss versus the load current, which is about 23.3 W and 24.1 W at 100 A with above mentioned inductor values.

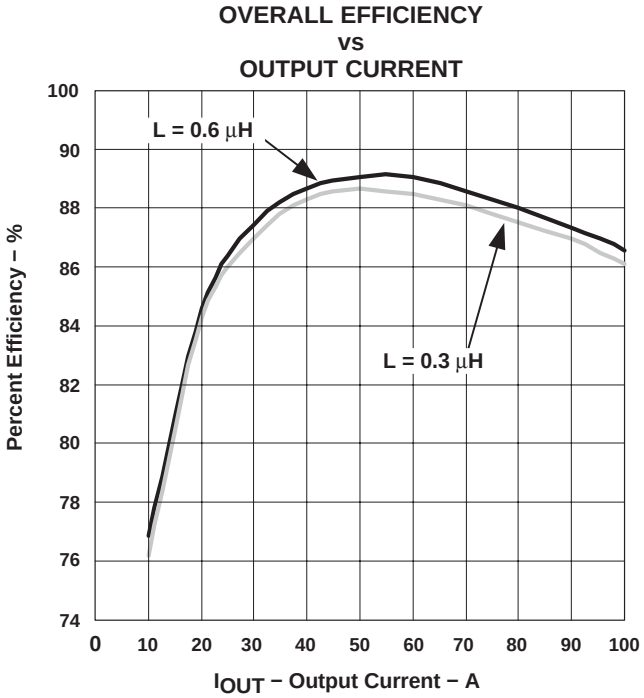


Figure 7.

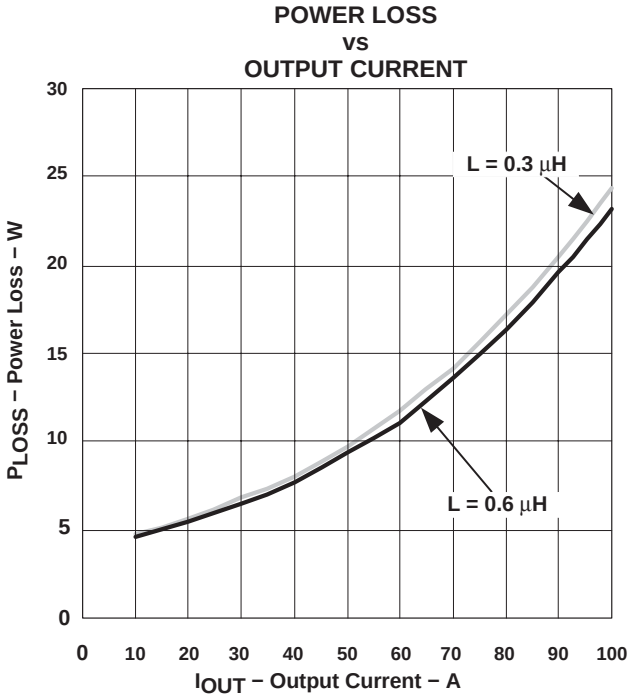


Figure 8.

5.2 Closed-Loop Performance

The TPS40090 uses peak current-mode control. Figure 9 shows the bode plots at 10 A and 100 A of load current respectively, where no droop function is implemented. The crossover frequency is at 89 kHz with phase margin of 59 degrees.

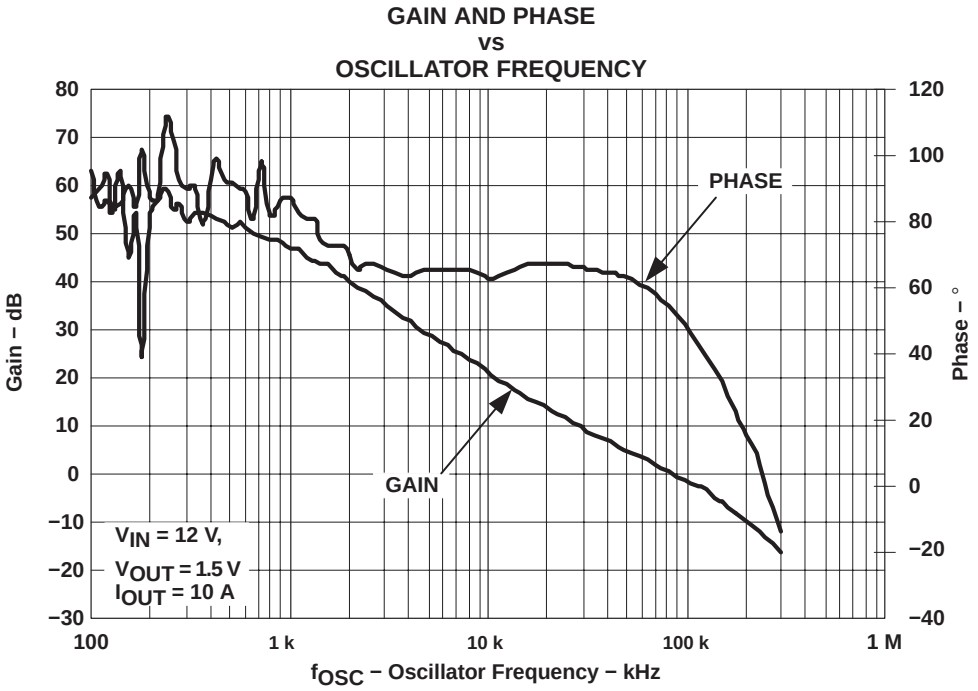


Figure 9.

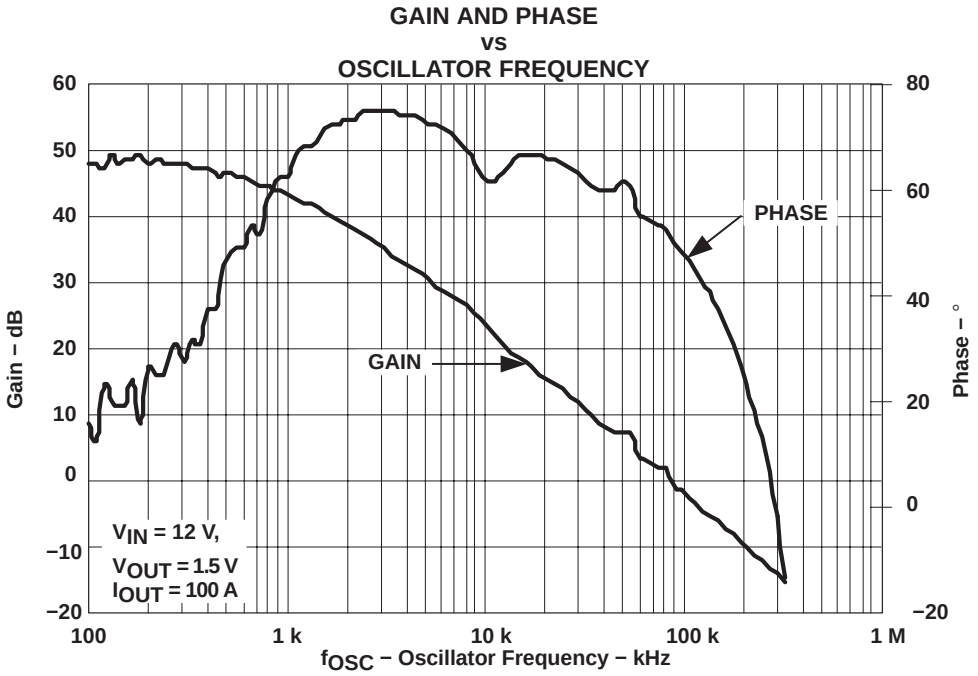


Figure 10.

5.3 Output Ripple and Noise

Figure 11 shows typical output noise where V_{IN}=12 V, and I_{OUT}=100A. The output ripple is less than 10 mV.

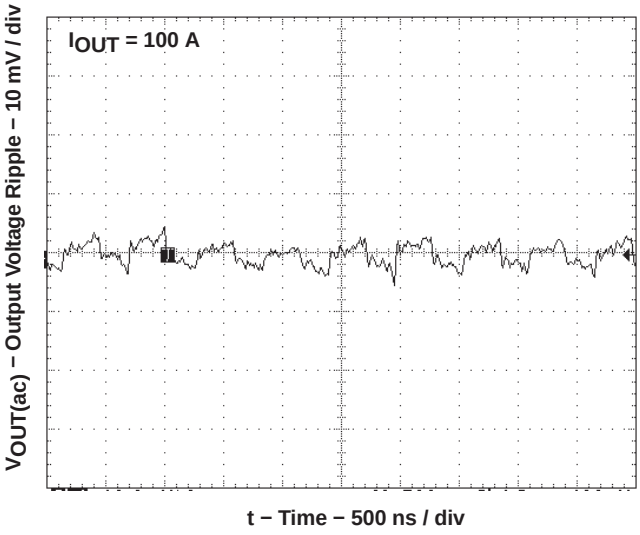


Figure 11. Output Noise

5.4 Transient Response

The on-board load transient circuit enables to check the step load transient response on the same board. By simply connecting pin1 and pin2 with a jumper on J3, the NE555PW generates a 100-Hz pulse signal with a 1% duty cycle to drive U6 (Si7858DP) which is in series with three 50-mΩ resistors, so a 90-A step load is created. The slew rates of the transient are 200 A/μs for the load step-down and 160 A/μs for the load step-up.

The transient response is shown in Figure 12 as the load is stepped from 10 A to 100 A. The output deviation is approximately 200 mV and the settling time is within 15 μs.

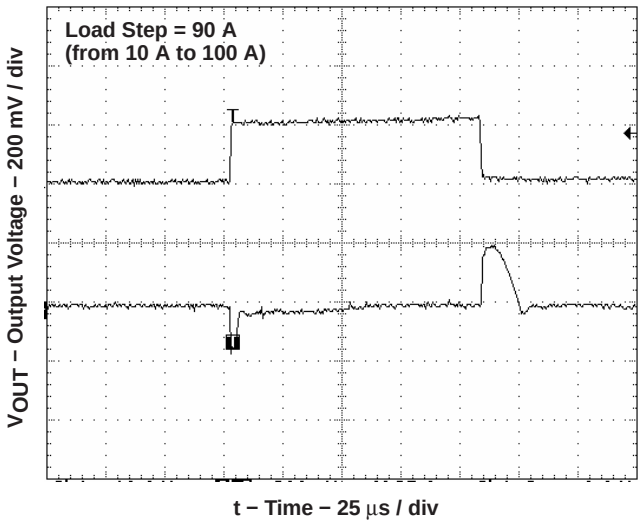


Figure 12. Transient Response Without Droop Function

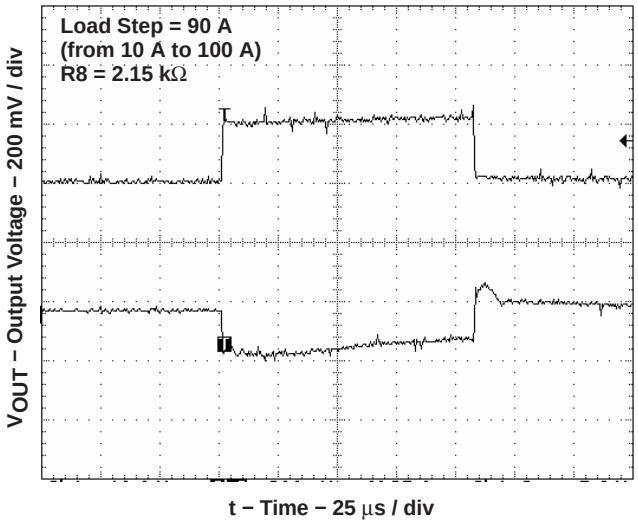


Figure 13. Transient Response With Droop Function

6 Layout Considerations

The PCB layout plays a critical role in the performance in a high frequency switching power supply design. Following the suggestions listed below will help to improve the performance and expedite the design.

- To take full advantage of the ripple cancellation factor from interleaving, place the input capacitors before the junction where the input voltage is distributed to each phase. Place the output capacitors after the junction where all the inductors are connected;
- Place the external drivers right next to the FETs and use at least 25 mil trace for gate drive signal to improve noise immunity
- Place some ceramic capacitors in the input of each channel to filter the current spikes
- Place the NTC resistor right next to its related inductor for better thermal coupling
- 2 oz. or thicker copper is recommended to reduce the trace impedance
- Place enough vias along pads of the power components to increase thermal conduction
- Keep the current sensing traces as short as possible to avoid excessive noise pick up
- Place the output inductors as symmetric as possible in relation to the output connectors to obtain similar voltage drop from the trace impedance

7 EVM Assembly Drawing and PCB Layout

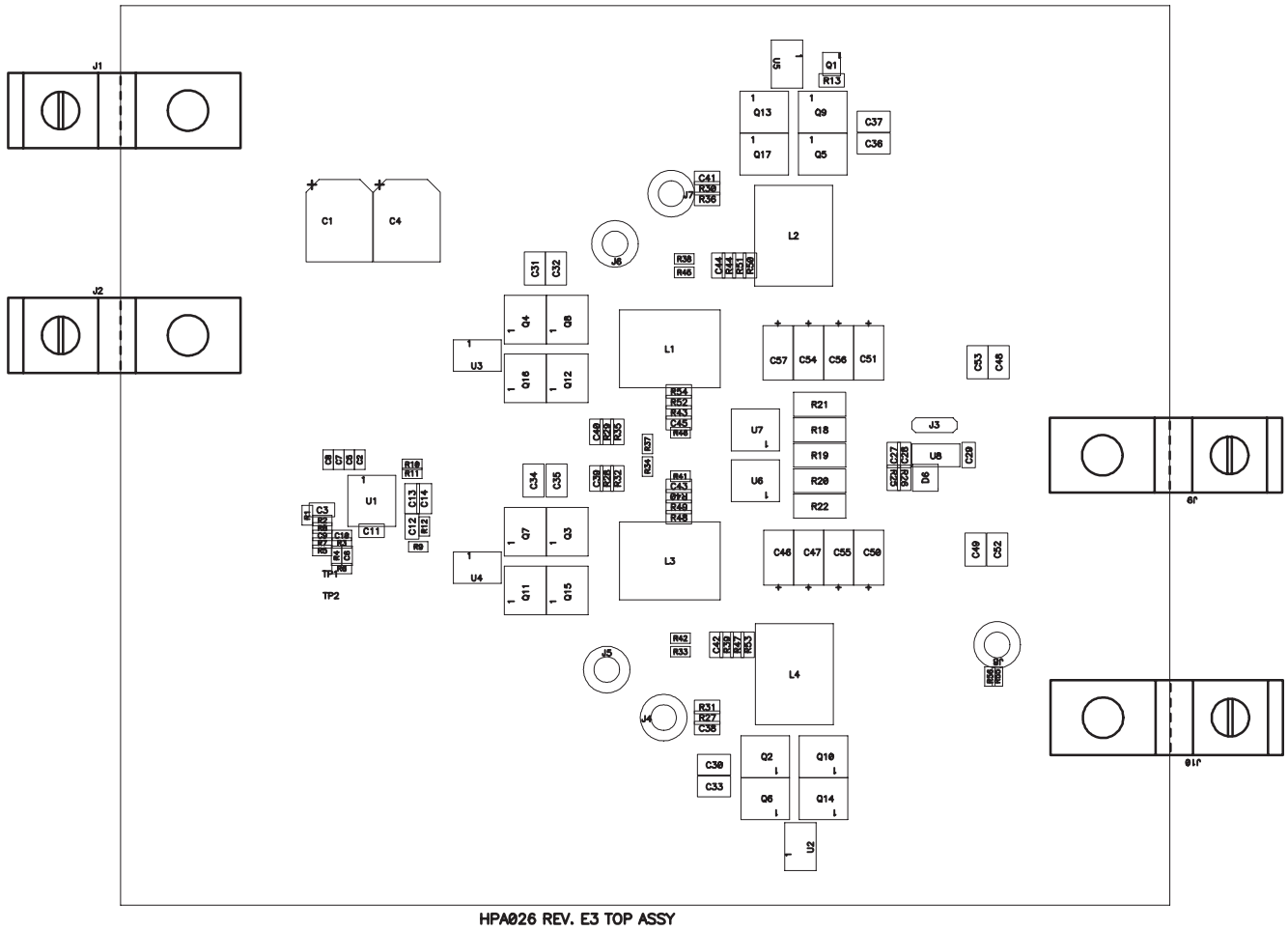
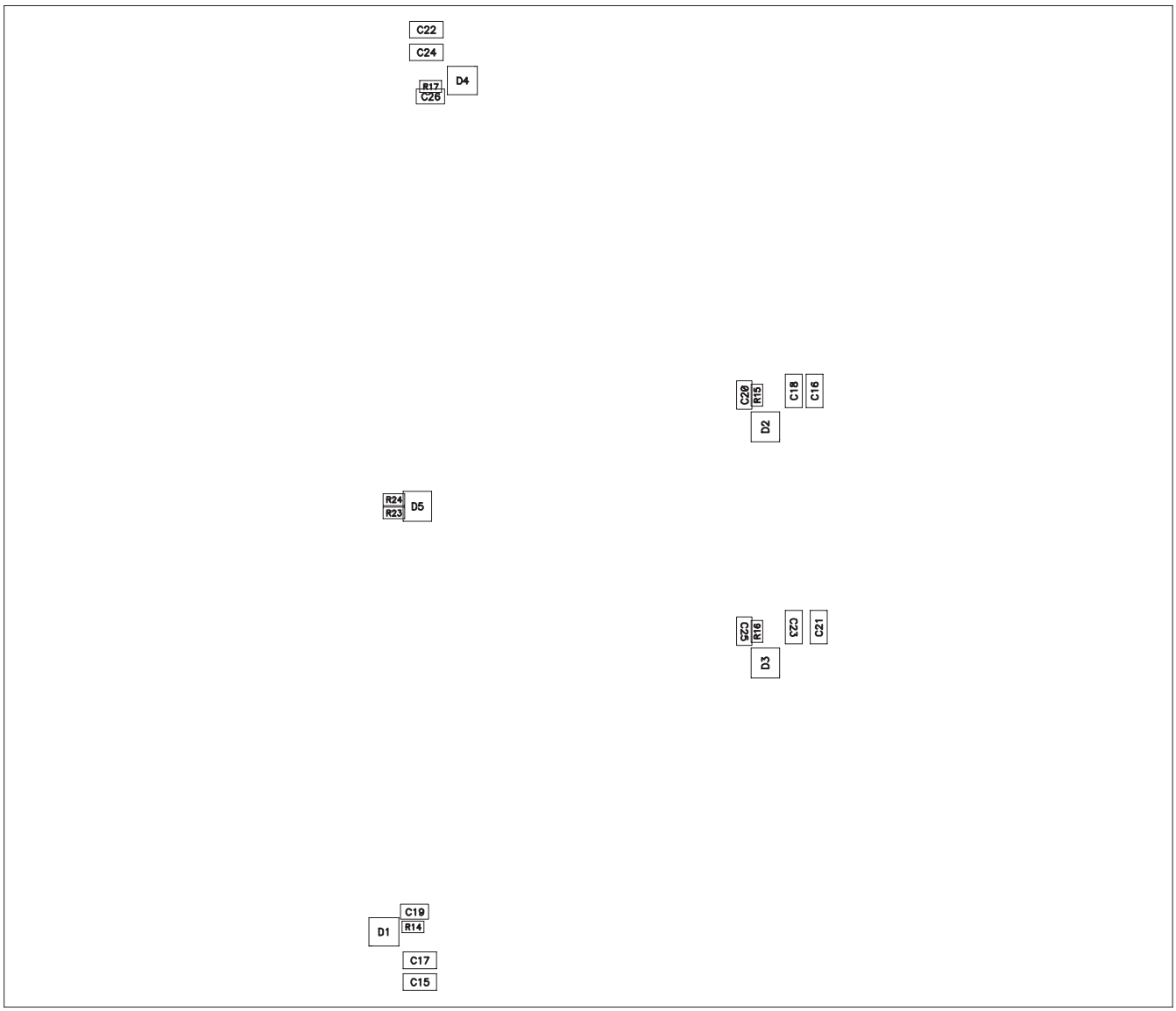


Figure 14. Top Side Component Assembly



HPA026 REV. E3 BOTTOM ASSY

Figure 15. Bottom Assembly

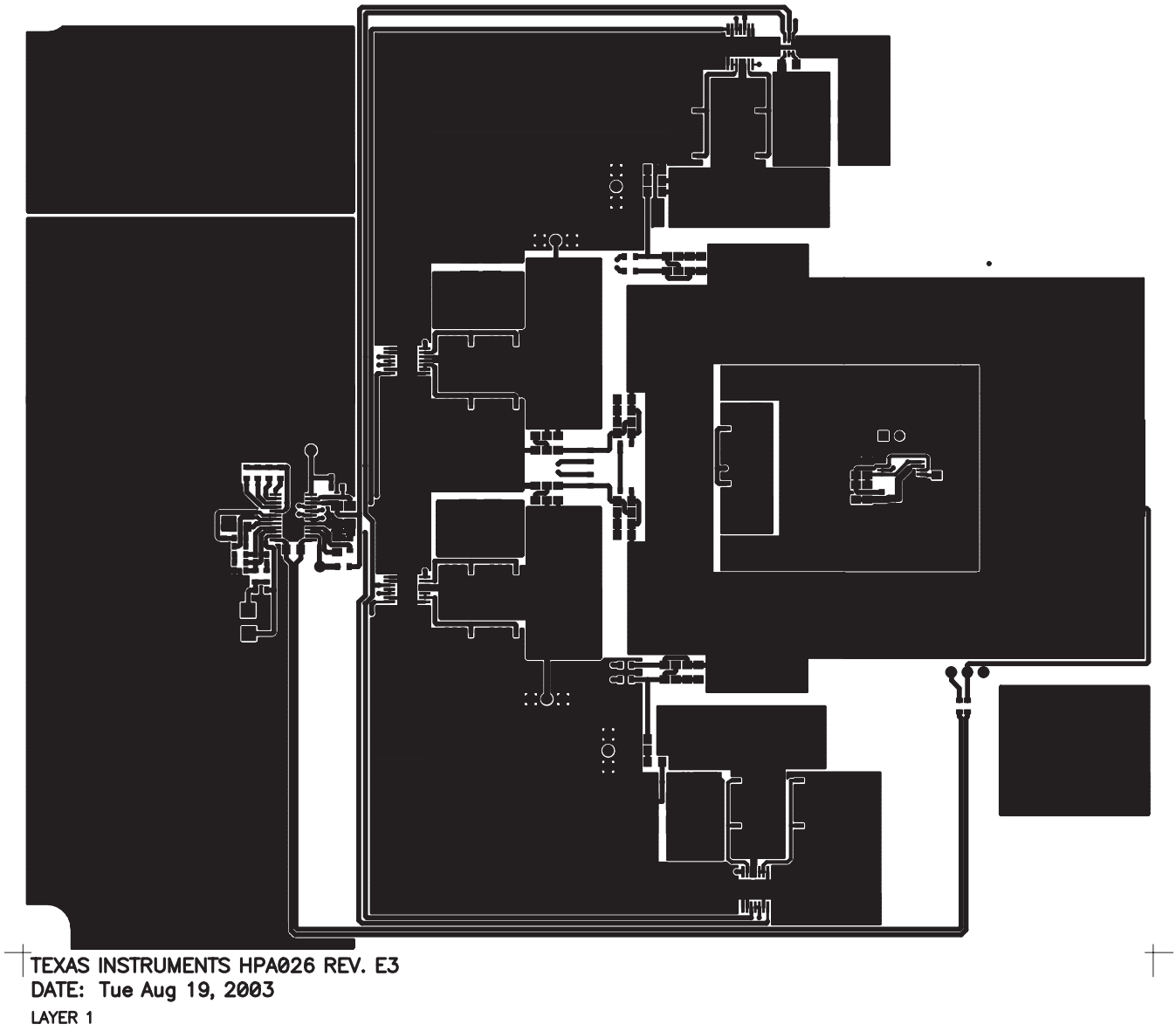


Figure 16. Top Side Copper

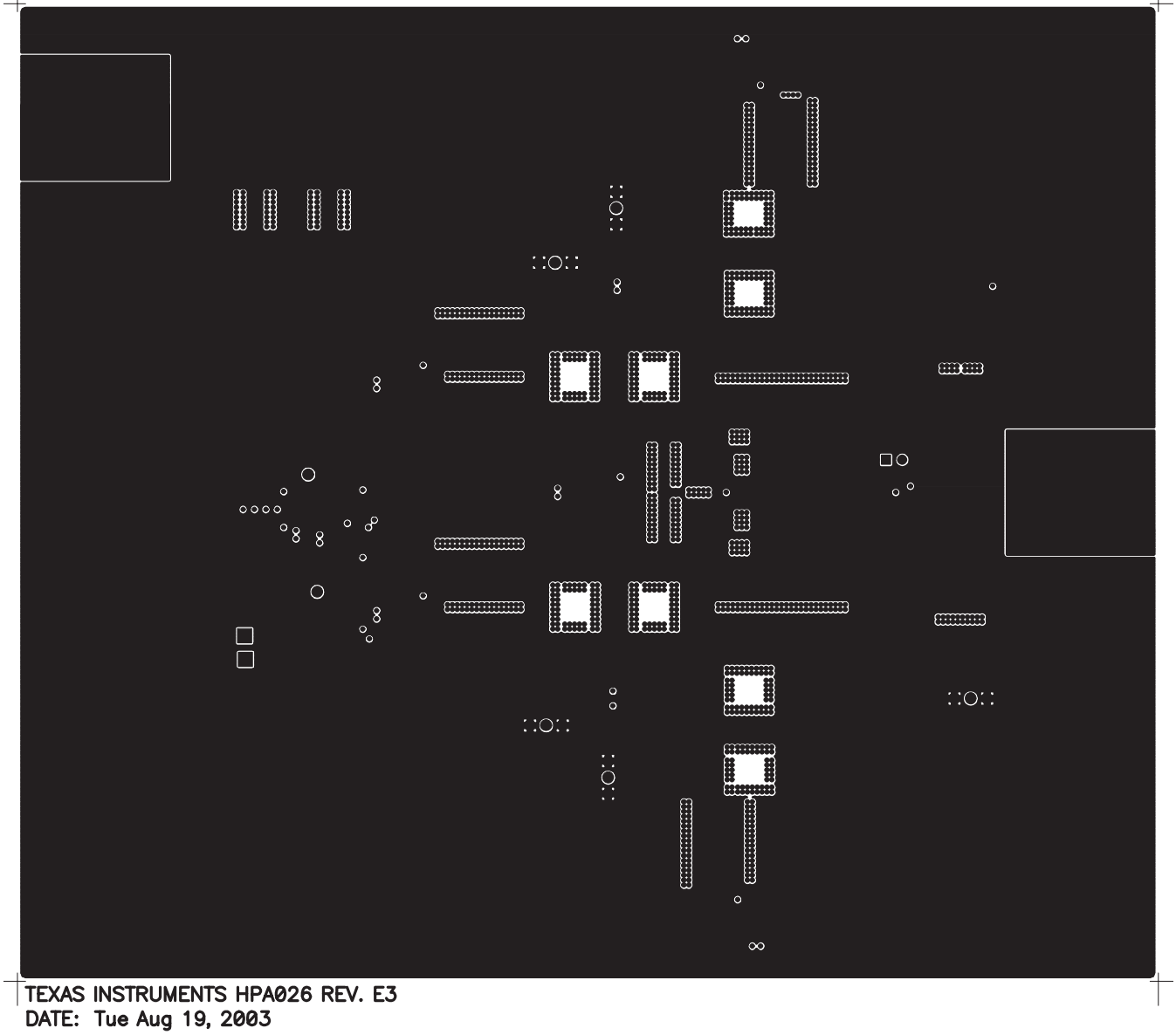


Figure 17. Internal 1 (Ground Plane)

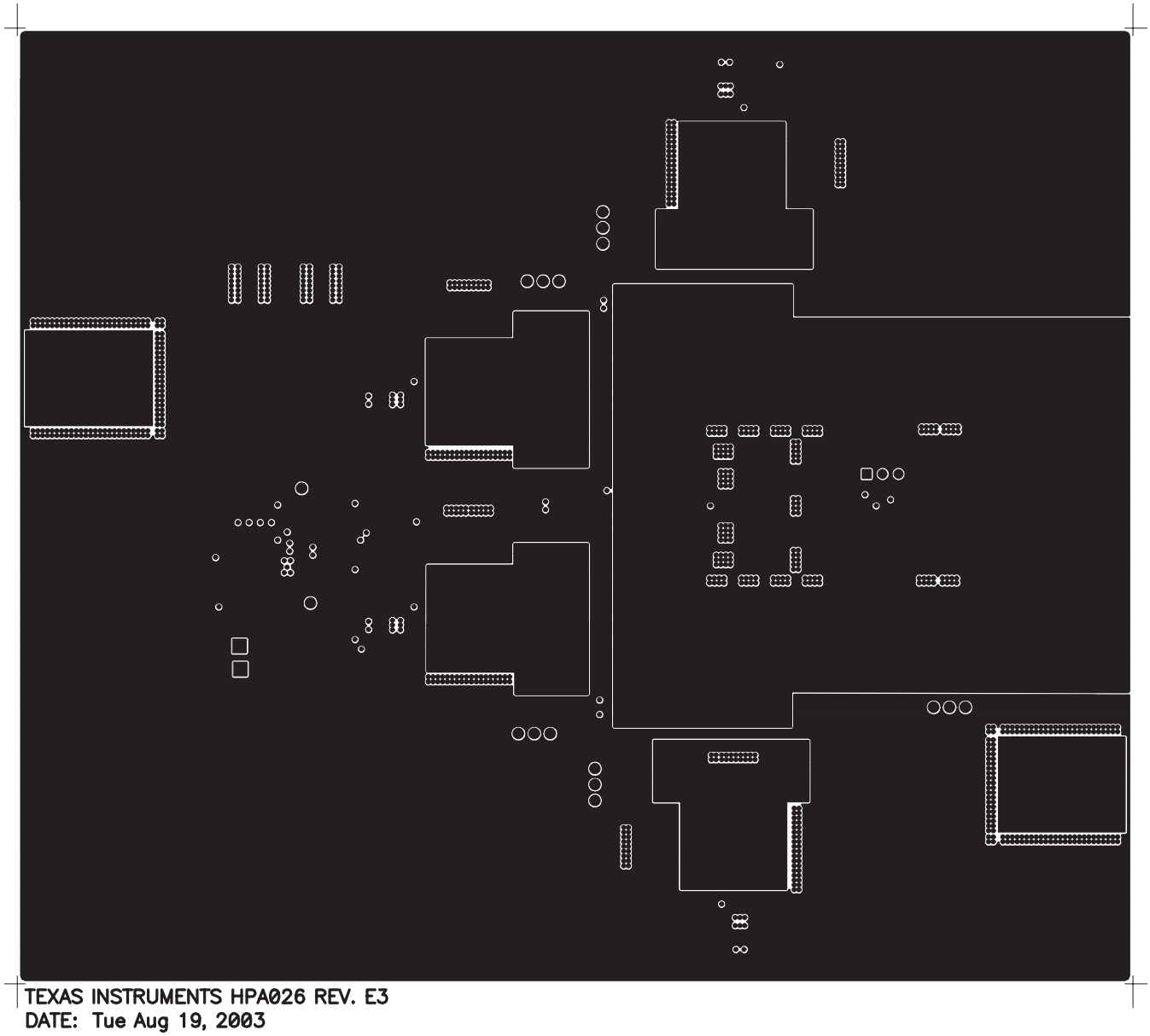


Figure 18. Internal 3 (Power Plane)

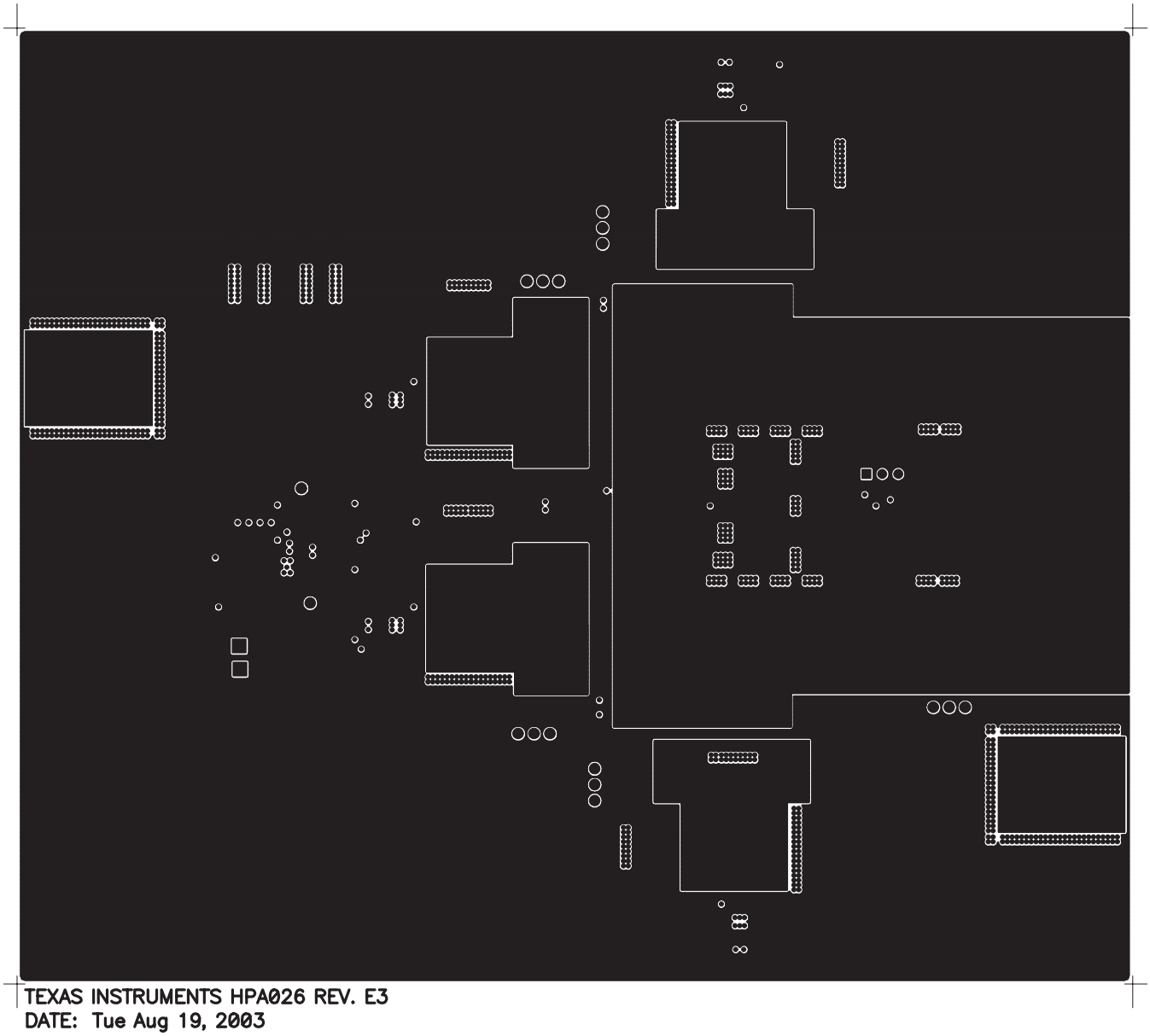


Figure 19. Internal 4 (Power Plane)

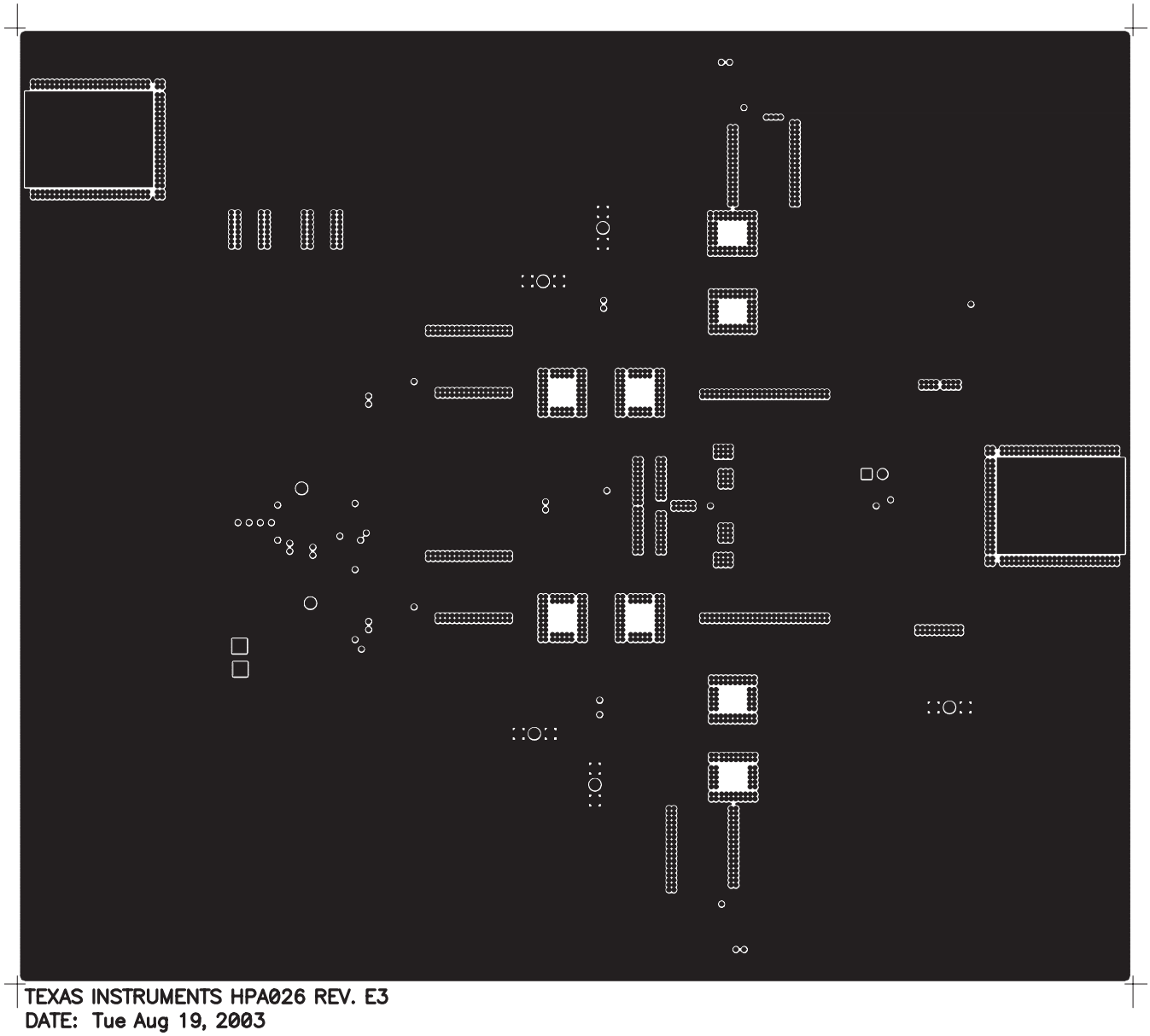


Figure 20. Internal 4 (Ground Plane)

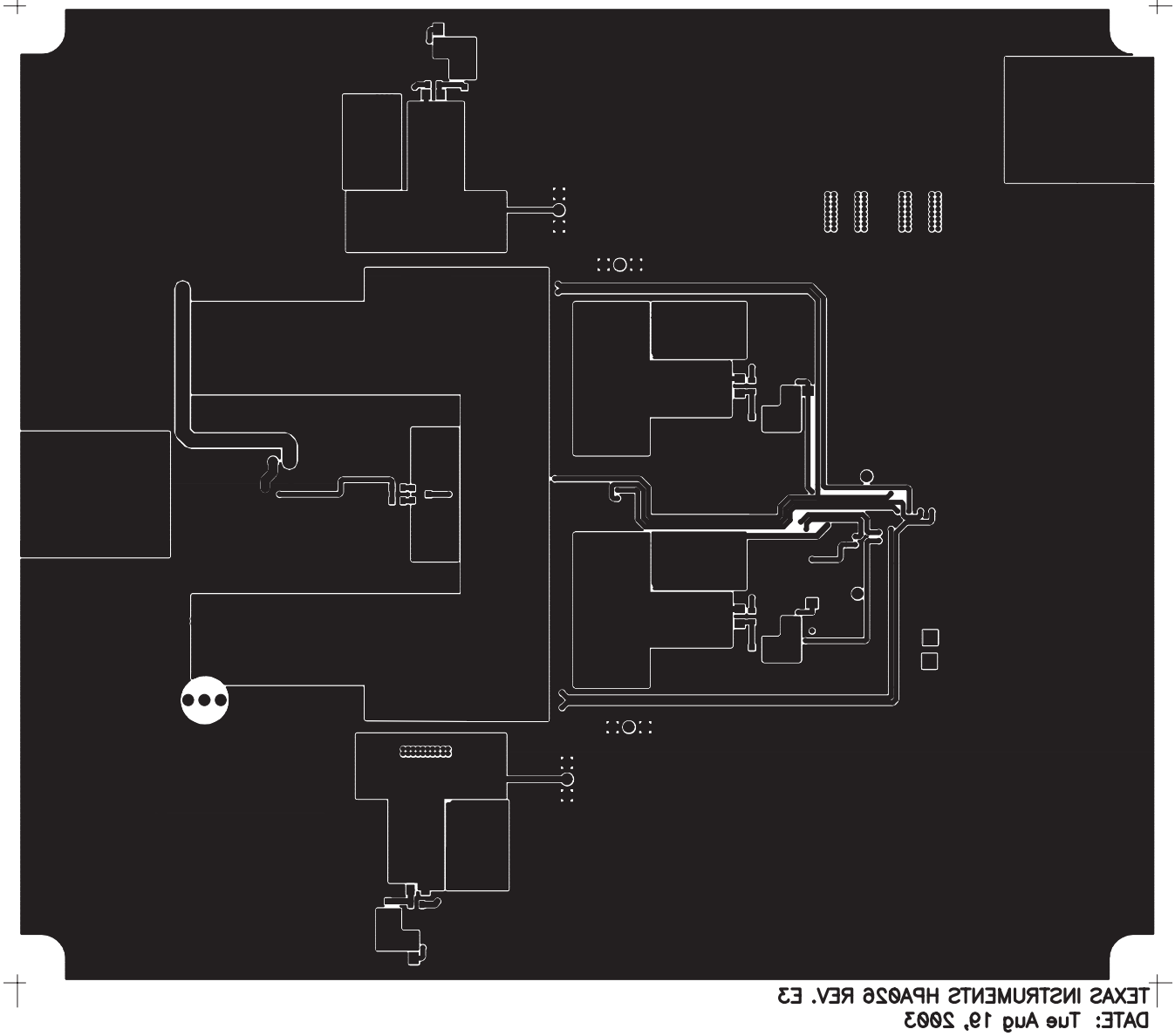


Figure 21. Bottom Layer Copper

8 List of Materials

The following table lists the TPS40090EVM−001 components corresponding to the schematic shown in Figure 1.

Table 2. List of Materials

REFERENCE DESIGNATOR		QTY	DESCRIPTION	SIZE	MFR	PART NUMBER
Capacitor	C1,C4	2	OS−CON, 68-µF, 20 V, 40−mΩ, 20%	10.3mm (F8)	Sanyo	20SVP68M
	C2, C5, C7, C8, C9, C11	6	Ceramic, 1−nF, 25 V, ±5%	603	muRata	GRM39SL102J25
	C3	1	Ceramic, 1.0-µF, 16 V, ±10%	805	muRata	GRM40B105K16
	C6	0		603	muRata	GRM39yyyxxxKvvvA
	C10	1	Ceramic, 10−pF, 50-V, COG, ±2.5%	603	muRata	GRQ706C0G100C50
	C12	1	Ceramic, 10−nF, 50-V, ±5%	805	muRata	GRM40UJ103J50
	C13,C14, C15, C16, C17, C18, C21, C22, C23, C24	10	Ceramic, 4.7-µF, 16-V, ±10%, X5R	1206	muRata	GRM42−65X5R475K16
	C19,C20,C25, C26	4	Ceramic, 1.0-µF, 16-V, ±10%, X5R	805	muRata	GRM40B105K16
	C27,C28	2	Ceramic, 0.1-µF, 25-V, ±10%, X5R	805	muRata	GRM40R104K25
	C29, C42, C43, C44, C45	5	Ceramic, 10−nF, 50-V, ±5%, X5R	805	muRata	GRM40UJ103J50
	C30, C31, C32, C33, C34, C35, C36, C37	8	Ceramic, 10-µF, 25-V, X5R	1210	TDK	C3225X5R1E106M
	C38, C39, C40, C41	4	Ceramic, 1000-pF, 50-V, ±5%, X5R	805	muRata	GRM40TH102J50
	C42, C43, C44, C45	4	Ceramic, 10−nF, 50-V, COG	805	TDK	C2012COG1H103JT
	C46,C47,C50, C51, C54, C55, C56, C57	8	POSCAP, 220-µF, 2.5-V, 15-mΩ, 20%	7343 (D)	Sanyo	2R5TPE220M
	C48, C49, C52, C53	4	Ceramic, 10-µF, 6.3-V, X5R	1206	TDK	C3216X5R0J106M
Diode	D1, D2, D3, D4, D6	5	Dual Schottky, 200-mA, 30-V	SOT23	Vishay−Liteon	BAT54C
	D5	1	Dual ultra-fast, series, 200-mA, 70-V	SOT23	Fairchild	BAV99
Test Points	E1, E2	2	Black, 1-mm	0.038	Farnell	240−333
	TP1	1	0.062 hole, red		None	Void
	TP2	1	0.062 hole, black			
Jumper	J1, J2, J9, J10	4	Lug, solderless, #2 − #8 AWG, 1/4	Copper	524600	ILSCO
	J3	1	Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 x 3	Sullins	PTC36SAAN
	J4, J5, J6, J7, J8	5	Connector, shielded, test jack vertical	.0125 DIA	Johnson	129−0701−202
Inductor	L1, L2. L3. L4	4	SMT, 0.62-µH, 30-A, 1.75-mΩ	0.524 x 0.492	TDK	SPM12550−R62M300

(1) Cannot be substituted.

REFERENCE DESIGNATOR		QTY	DESCRIPTION	SIZE	MFR	PART NUMBER
MOSFET	Q1	1	N−channel, 20-V, 0.7-A, 385-mΩ, P−channel,−20-V, 0.440-A, 995-mΩ	SC−70	Vishay	Si1553DL
	Q2, Q3, Q4, Q5(1)	4	N−channel, 30-V, 18-A, 8.0-mΩ,	PWRPAK S0−8	Vishay−Siliconix	Si7860DP
	Q6, Q7, Q8, Q9	0	N−channel, 30-V, 18-A, 8.0-mΩ,	PWRPAK S0−8	Vishay−Siliconix	Si7860DP
	Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17	8	N−channel, 30-V, 29-A, 3-mΩ,	PWRPAK S0−8	Vishay−Siliconix	Si7880DP
Resistor	R1	1	Chip, 8.25-kΩ, 1/16-W, 1%	603	Std	Std
	R2	1	Chip, 6.19-kΩ, 1/16-W, 1%	603	Std	Std
	R3	0		603	Std	Std
	R4	1	Chip, 10-kΩ, 1/16-W, 1%	603	Std	Std
	R5	1	Chip, 8.75-kΩ, 1/16-W, 1%	603	Std	Std
	R6	1	Chip, 49.9−Ohms, 1/16-W, 1%	603	Std	Std
	R7	1	Chip, 40.2-kΩ, 1/16-W, 1%	603	Std	Std
	R8	1	Chip, 10-Ω, 1/16-W, 1%	603	Std	Std
	R9, R11	2	Chip, 10-kΩ, 1/16-W, 1%	603	Std	Std
	R10	1	Chip, 475-kΩ, 1/16-W, 5%	603	Std	Std
	R12	1	Chip, 64.9-kΩ, 1/16-W, 1%	603	Std	Std
	R13	1	Chip, 100-kΩ, 1/16-W, 5%	805	Std	Std
	R14, R15, R16, R17	4	Chip, 3.3-Ω, 1/16-W, 1%	603	Std	Std
	R18, R19, R21	3	Chip, 0.050-Ω, 1-W, 1%	2512	Vishay	WSL−2512−R050 R86
	R20, R22	0		2512	Vishay	WSL−2512−xx 1% R86
	R23, R24, R55, R56	4	Chip, 10-Ω, 1/16-W, 1%	603	Std	Std
	R25	1	Chip, 143-kΩ, 1/10-W, 1%	805	Std	Std
	R26	1	Chip, 1.43-kΩ, 1/10-W, 1%	805	Std	Std
	R27, R28, R29, R30	4	Chip, 2.2-Ω, 1/10-W, 1%	805	Std	Std
	R31, R32, R35, R36	4	Chip, 19.6-kΩ, 1/10-W, 1%	805	Std	Std
	R33, R34, R37, R38, R41, R42, R45, R46,	8	Chip, 2.7-Ω, 1/10-W, 1%	603	Std	Std
	R39, R40, R43, R44,	4	Chip, 22.6-kΩ, 1/10-W, 1%	805	Std	Std
	R47, R49, R51, R52	4	Chip, 124-kΩ, 1/10-W, 1%	805	Std	Std
	R48, R50, R53, R54	4	NTC chip, 100-kΩ, 1/10-W, 1%	805	Vishay	NTHS0603N01N1003J

(1) Cannot be substituted.

REFERENCE DESIGNATOR		QTY	DESCRIPTION	SIZE	MFR	PART NUMBER
Integrated Circuit	U1(1)	1	Multi-phase synchronous buck controller	TSSOP-24	TI	TPS40090PW
	U2,U3,U4,U5(1)	4	High-efficiency predictive synchronous buck driver	PWP-14	TI	UCC27222PWP
	U6	1	N-channel, MOSFET, 12-V, 29-A, 3-mΩ	PWRPAK S0−8	Vishay	Si7858DP
	U7	0	N-channel, MOSFET, 12-V, 29-A, 3-mΩ	PWRPAK S0−8	Vishay	Si7858DP
	U8	1	Precision timer	TSSOP−8	TI	NE555PW

(1) Cannot be substituted.

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