



UCC28950 Dual-Channel Isolated Full-Bridge Converter

TI reference design number: PMP6712 Rev C

**Input: 38V – 60V
Output: 54V @ 30A**

DC – DC Test Results

PMP6712 Rev C Test Results

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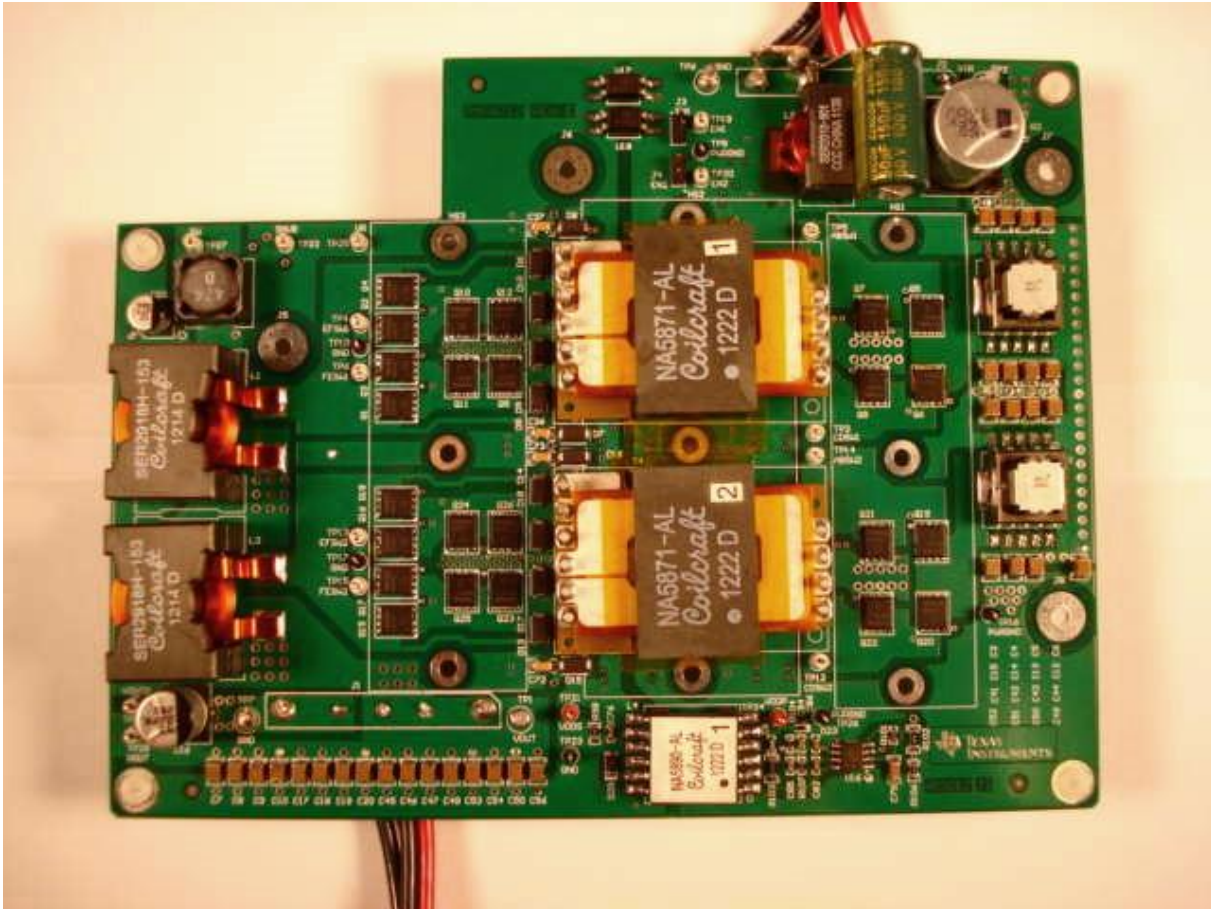
Note: *The circuit was built and tested on PMP6712 Rev C printed circuit board. Documentation for Rev D is provided, which fixes some minor connection and spacing issues.*

1 Circuit Description

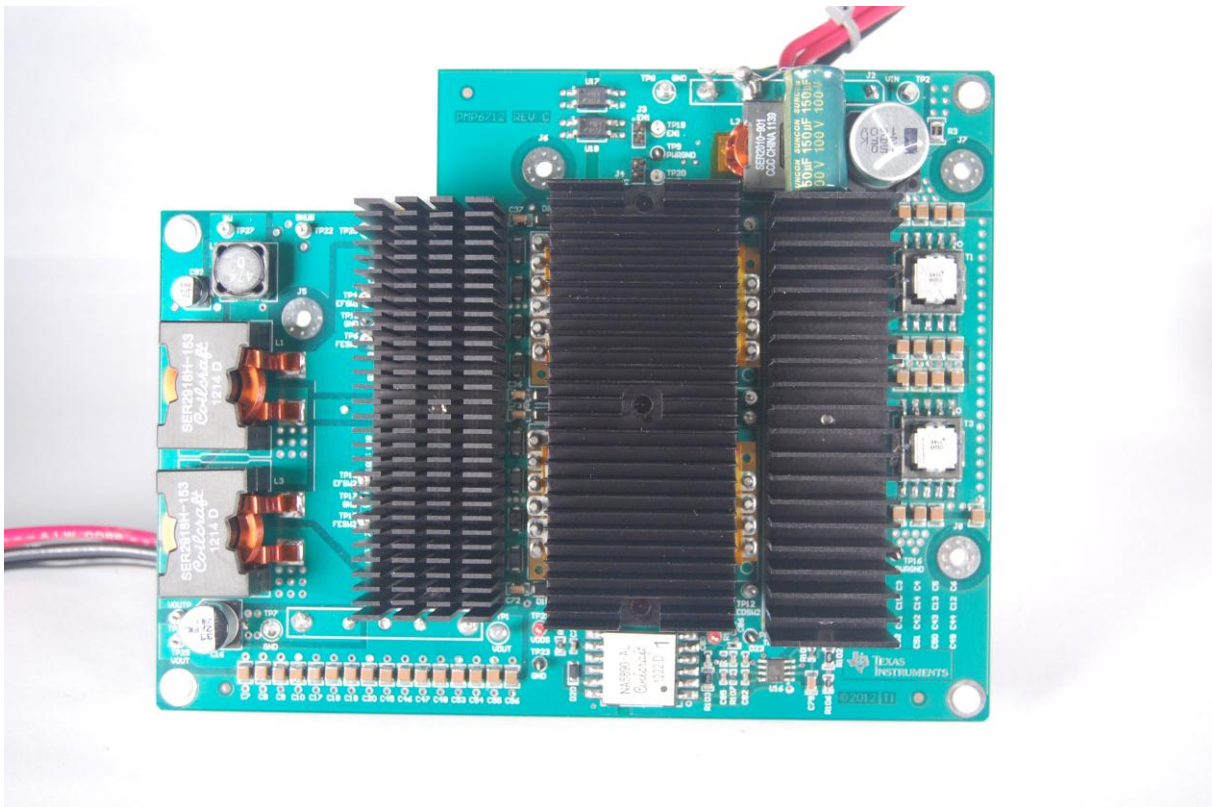
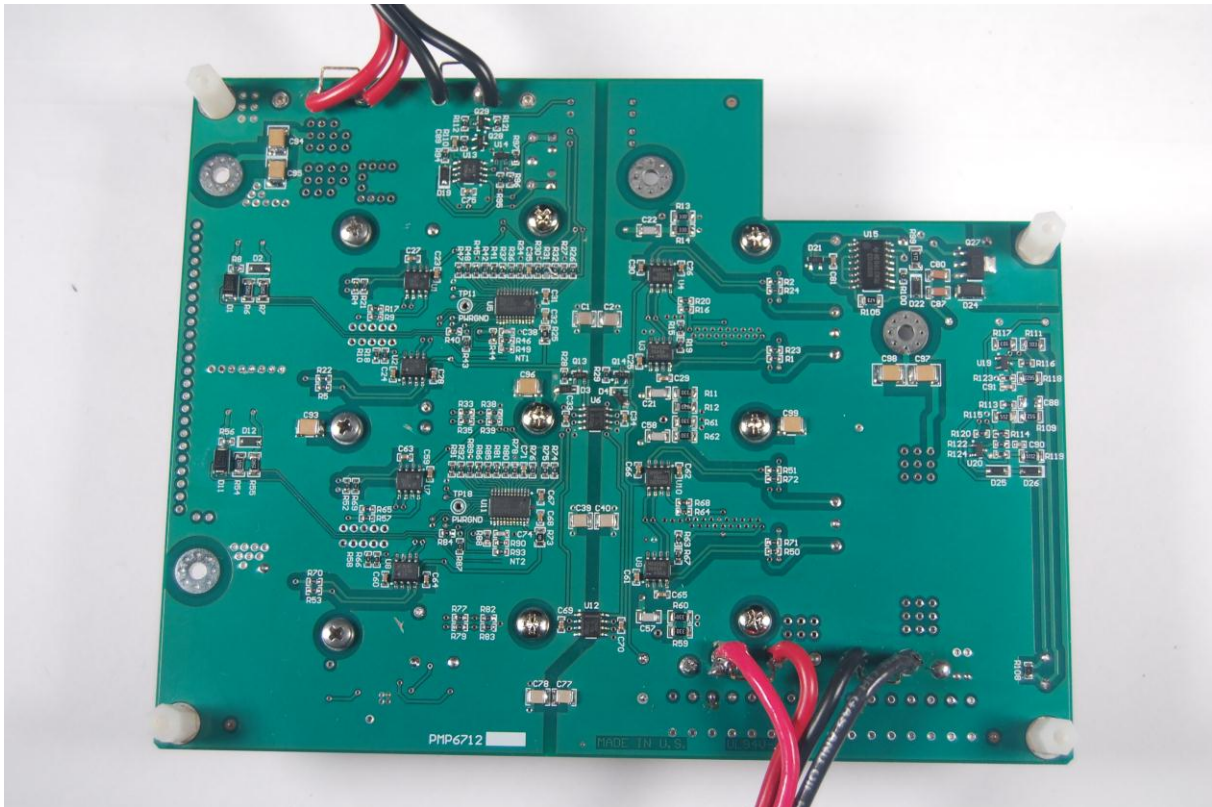
PMP6712 is a phase-shifted full-bridge converter capable of delivering 1600W of isolated output power. This design uses the UCC28950 controller in a dual phase master-slave configuration. An LM5017 constant on-time synchronous buck regulator provides bias power to primary and secondary-side circuits using a coupled inductor with isolated flyback winding. ISO7420FED digital isolators couple gate drive signals from the primary-side control to the secondary side drivers. Primary side MOSFETs are Infineon BSC057N08NS3 G driven by LM5100 gate drivers. Secondary-side MOSFETs are Infineon BSC190N15NS3 G driven by MAX15013 gate drivers. These best in class MOSFETs and drivers allow this design to reach greater than 96% efficiency. A unique hysteretic active buck snubber clamps the secondary switching spikes to a safe level and returns the stored energy to the output. Features include peak current-mode control for inherent current limit and current-sharing of master and slave phases. Input and VDD bias supply under-voltage lockout are provided for robust control of power-up and power-down events. Opto-coupler feedback is implemented using a TL431 shunt regulator for accurate output voltage control. A separate output over-voltage protection opto-coupler and shunt regulator limits the output voltage during a fault event.

2 Photos

The photographs below show the PMP6712 Rev C board assembly. This circuit was built on a 10 layer board to simulate a typical system board. See the associated printed circuit board documentation for board layer assignment and stack-up. A minimum layer implementation may be done on a four layer board using the four active signal layers. Power components are mounted on the top side of the board, with control circuits on the bottom. The overall board dimensions are 6.995" x 5.405". With heat sinks, the top side component height is 1.1" allowing the board to fit into a 1RU (rack unit) slot.



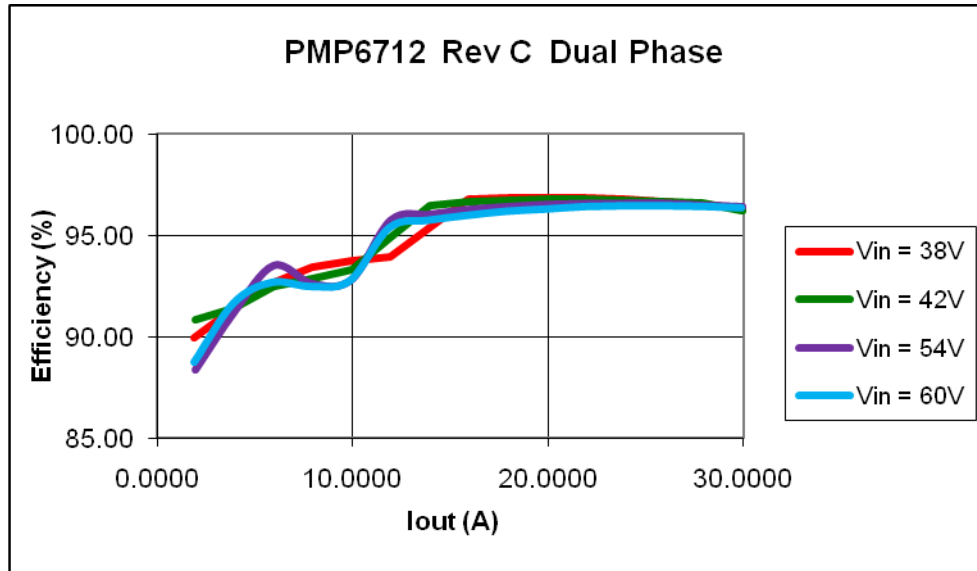
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3 Efficiency

The efficiency data is shown in the tables and graph below. Peak efficiency in excess of 96% is recorded at all input voltage conditions. Good light load efficiency above 91% is exhibited at a load of 4A.



Vin (V)	Iin (A)	Vout (V)	Iout (A)	Efficiency (%)	Pin (W)	Pout (W)	Losses (W)
38.0028	3.0632	54.2558	1.9306	89.98	116.41	104.75	11.66
38.0022	6.1862	54.2445	3.9630	91.44	235.09	214.97	20.12
38.0024	9.1730	54.2445	5.9580	92.71	348.60	323.19	25.41
38.0028	12.1572	54.2445	7.9572	93.43	462.01	431.63	30.37
38.0028	15.1516	54.2445	9.9534	93.77	575.80	539.92	35.89
38.0030	18.1538	54.2445	11.9498	93.96	689.90	648.21	41.69
38.0029	20.8670	54.2445	13.9468	95.40	793.01	756.54	36.47
38.0028	23.5288	54.2445	15.9586	96.81	894.16	865.67	28.49
38.0030	26.4584	54.2445	17.9554	96.87	1005.50	973.98	31.52
38.0032	29.4078	54.2445	19.9564	96.86	1117.59	1082.52	35.07
38.0032	32.3726	54.2445	21.9604	96.83	1230.26	1191.23	39.03
38.0033	35.3412	54.2445	23.9600	96.77	1343.08	1299.70	43.38
38.0039	38.3208	54.2445	25.9548	96.67	1456.34	1407.91	48.43
38.0036	41.3196	54.2445	27.9436	96.53	1570.29	1515.79	54.51
38.0037	44.3544	54.2445	29.9456	96.37	1685.63	1624.38	61.25

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Efficiency (%)	Pin (W)	Pout (W)	Losses (W)
42.0022	2.7824	54.2617	1.9560	90.82	116.87	106.14	10.73
42.0020	5.5700	54.2435	3.9436	91.44	233.95	213.91	20.04
42.0022	8.3162	54.2435	5.9538	92.46	349.30	322.95	26.34
42.0025	11.0430	54.2435	7.9424	92.88	463.83	430.82	33.01
42.0023	13.7578	54.2435	9.9410	93.32	577.86	539.23	38.62
42.0022	16.2504	54.2435	11.9392	94.88	682.55	647.62	34.93
42.0027	18.6618	54.2435	13.9424	96.48	783.85	756.28	27.56

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42.0029	21.2972	54.2435	15.9448	96.69	894.54	864.90	29.64
42.0029	23.9426	54.2435	17.9390	96.76	1005.66	973.07	32.58
42.0035	26.6048	54.2435	19.9426	96.80	1117.49	1081.76	35.74
42.0025	29.2784	54.2435	21.9466	96.80	1229.77	1190.46	39.31
42.0031	31.9568	54.2435	23.9446	96.76	1342.28	1298.84	43.45
42.0038	34.6484	54.2435	25.9414	96.69	1455.36	1407.15	48.21
42.0034	37.3544	54.2435	27.9376	96.59	1569.01	1515.43	53.58
42.0035	40.1924	54.2435	29.9416	96.20	1688.22	1624.14	64.08

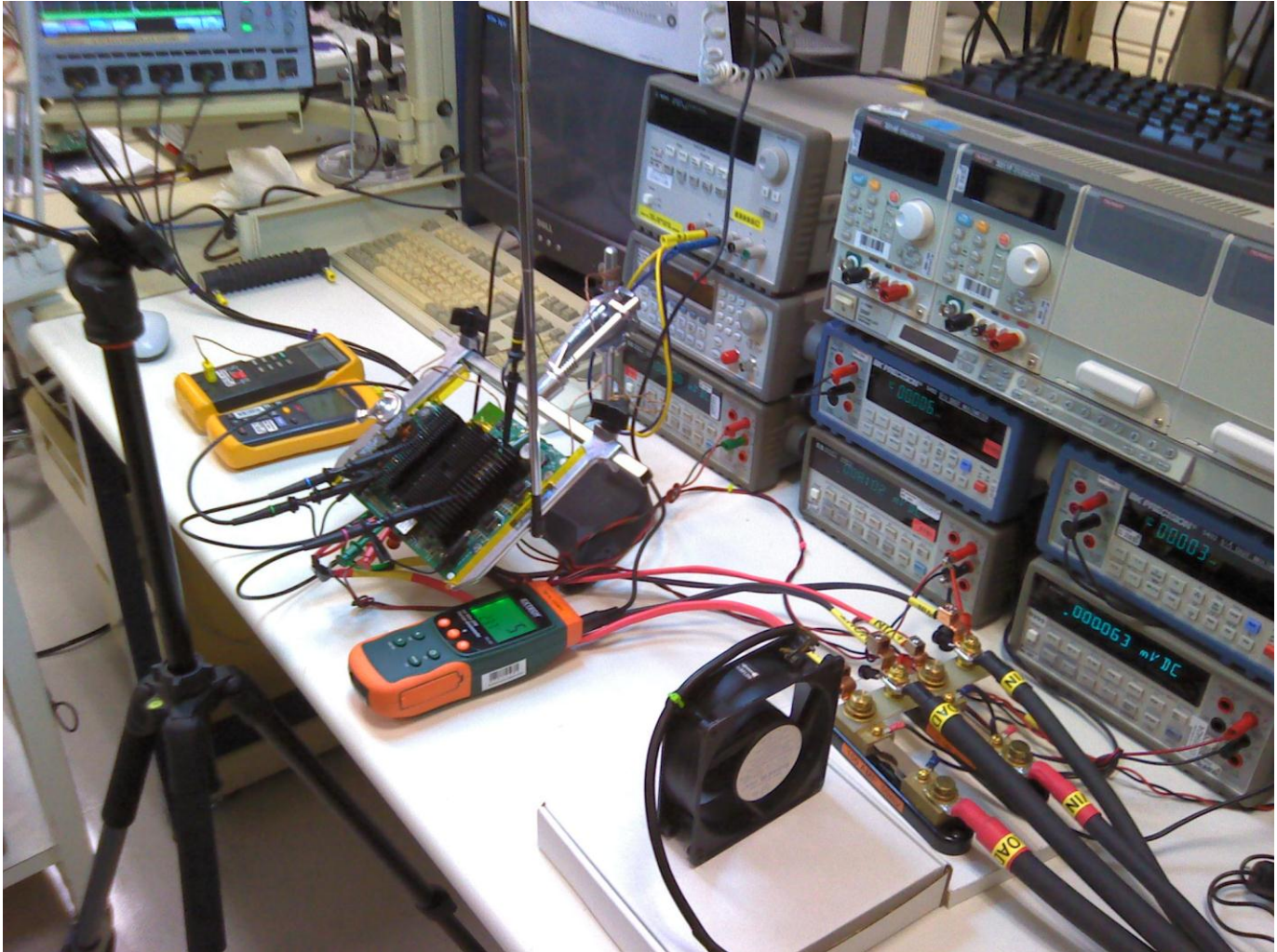
Vin (V)	Iin (A)	Vout (V)	Iout (A)	Efficiency (%)	Pin (W)	Pout (W)	Losses (W)
54.0031	2.2000	54.2642	1.9354	88.40	118.81	105.02	13.78
54.0031	4.3478	54.2536	3.9506	91.29	234.79	214.33	20.46
54.0035	6.3816	54.2536	5.9418	93.54	344.63	322.36	22.26
54.0031	8.6020	54.2536	7.9324	92.64	464.53	430.36	34.17
54.0031	10.7444	54.2536	9.9302	92.85	580.23	538.75	41.48
54.0035	12.5232	54.2536	11.9400	95.78	676.30	647.79	28.51
54.0031	14.5744	54.2536	13.9358	96.06	787.06	756.07	31.00
54.0036	16.6296	54.2536	15.9410	96.30	898.06	864.86	33.20
54.0036	18.6844	54.2536	17.9362	96.44	1009.02	973.10	35.92
54.0036	20.7506	54.2536	19.9426	96.55	1120.61	1081.96	38.65
54.0039	22.8262	54.2536	21.9472	96.59	1232.70	1190.71	41.99
54.0034	24.9024	54.2536	23.9458	96.60	1344.81	1299.15	45.67
54.0039	26.9842	54.2536	25.9466	96.60	1457.25	1407.70	49.56
54.0044	29.0814	54.2536	27.9370	96.51	1570.52	1515.68	54.84
54.0043	31.1880	54.2536	29.9382	96.44	1684.29	1624.26	60.03

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Efficiency (%)	Pin (W)	Pout (W)	Losses (W)
60.0058	1.9594	54.2640	1.9234	88.77	117.58	104.37	13.20
60.0060	3.8810	54.2539	3.9356	91.69	232.88	213.52	19.36
60.0060	5.7608	54.2539	5.9068	92.71	345.68	320.47	25.22
60.0062	7.7264	54.2539	7.9054	92.51	463.63	428.90	34.73
60.0062	9.6476	54.2539	9.9024	92.80	578.92	537.24	41.67
60.0061	11.2826	54.2539	11.9058	95.41	677.02	645.94	31.09
60.0064	13.1258	54.2539	13.9042	95.78	787.63	754.36	33.27
60.0062	14.9764	54.2539	15.9046	96.02	898.68	862.89	35.79
60.0061	16.8230	54.2539	17.9024	96.22	1009.48	971.28	38.21
60.0070	18.6804	54.2539	19.9038	96.33	1120.95	1079.86	41.10
60.0068	20.5420	54.2539	21.9132	96.45	1232.66	1188.88	43.78
60.0069	22.4040	54.2539	23.9090	96.49	1344.39	1297.16	47.24
60.0070	24.2758	54.2539	25.9082	96.49	1456.72	1405.62	51.10
60.0070	26.1544	54.2539	27.9052	96.46	1569.45	1513.97	55.48
0.0069	28.0520	54.2539	29.9076	96.39	1683.31	1622.60	60.71

4 Thermal Tests

All tests were performed at room temperature on an open bench. The worst case input voltage of 60V was used for all thermal tests.

4.1 Test Setup



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4.2 Thermal Test Summary

PMP6712 Rev C Board #2, without heat sinks, no airflow, 800W thermal test - measured temperature at 24°C ambient											
Vin @ 60V, Vout @ 54V. All temperatures in Celsius. Monitor input FETs @ Q5, Q6, output FETs @ Q11, Q1. Board mounted at a 45 degree angle.											
	Airflow (LFM)	Ambient Temp.	Load Current	Temp Probe @ Output FETs	Temp Probe @ Input FETs	Output Inductor Area 1	Output FETs Area 2	Transformer Heat Sink Area 3	Input FETs Area 4	Current Sense Transformer Area 5	Transformer Winding Side View
Top up	0	23.7	15.0	72.2	84.0	80.2	81.5	110.8	87.1	78.2	111.0
Bottom up	0	24.6	15.0	76.4	84.8						

Efficiency without heat sinks @ Vin = 60V & no airflow								
No Airflow	Vin (V)	Iin (A)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Pdis (W)	Efficiency
50% Load	60	14.414	864.84	54	15.380	830.52	34.32	0.960

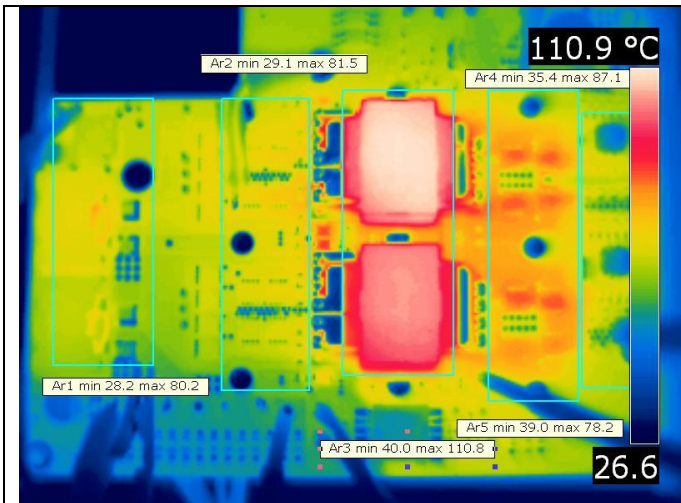
PMP6712 Rev C Board #2 with heat sinks, 1600 watt thermal test - measured temperature at 24°C ambient											
Vin @ 60V, Vout @ 54V. All temperatures in Celsius. Monitor input FETs @ Q5, Q6, output FETs @ Q11, Q1. Board mounted at a 45 degree angle.											
	Airflow (LFM)	Ambient Temp.	Load Current	Temp Probe @ Output FETs	Temp Probe @ Input FETs	Output Inductor Area 1	Output FETs Area 2	Transformer Heat Sink Area 3	Input FETs Area 4	Current Sense Transformer Area 5	Transformer Winding Side View
20 min*	0	24.2	30	87.4	107.5	94.7	76.0	114.6	109.3	104.5	116.0
45 min**	200	24.3	30	66.2	55.3	69.7	65.8	79.6	60.9	58.4	77.2
* NOTE: Temperature still climbing about 1°C per minute											
** NOTE: Temperature stable at 200 LFM											

Efficiency with heat sinks @ Vin = 60V & no airflow								
No Airflow	Vin (V)	Iin (A)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Pdis (W)	Efficiency
100% Load	60.132	28.192	1695.24	54.097	29.994	1622.59	72.656	0.957
50% Load	60.023	14.421	865.59	54.138	14.970	810.45	55.146	0.936
20% Load	60.024	5.799	348.08	54.712	5.962	326.19	21.886	0.937
No Load	60.025	0.018	1.08	45.254	0			

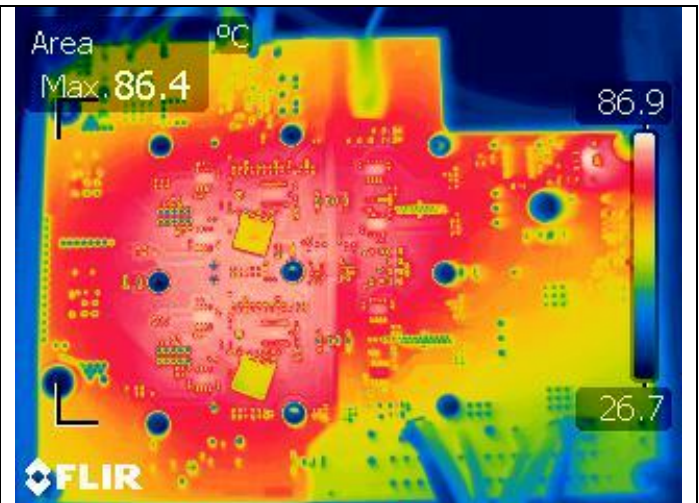
4.3 15A Load, No Heat Sinks, No Airflow

At 50% load with no heat sinks or airflow, the transformer exhibited the highest temperature rise of $111^{\circ}\text{C} - 23.7^{\circ}\text{C} = 87.3^{\circ}\text{C}$.

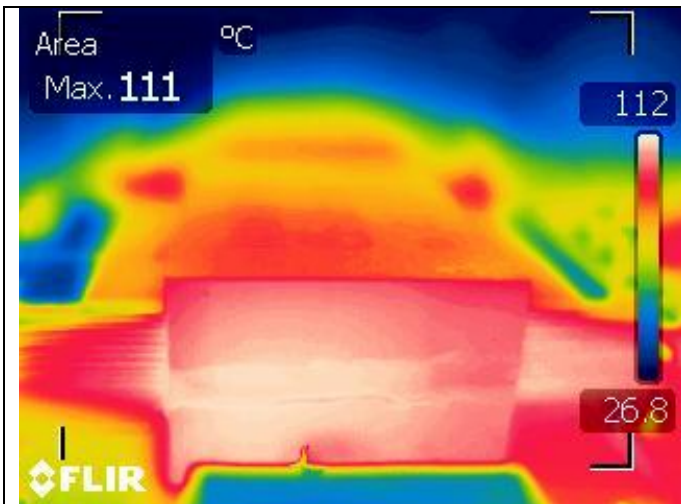
Adjustment pots on the bottom of the board were used to set the delay time, showing up as cooler square areas in the thermal image. Optimum component values are listed in the bill of material.



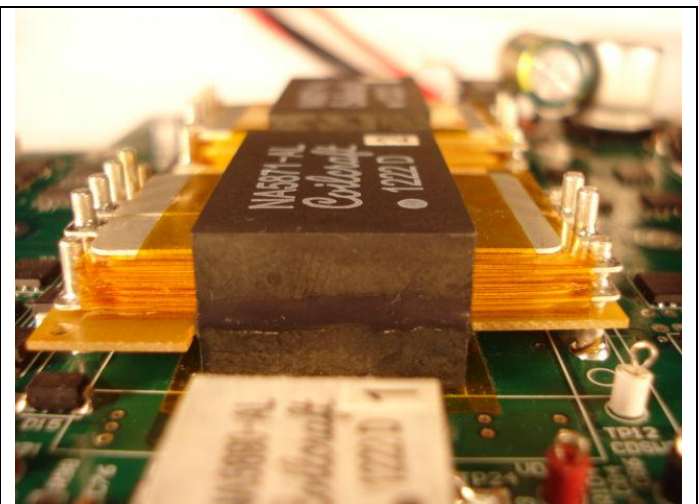
Top View, 60Vin, 15A Load



Bottom View, 60Vin, 15A Load



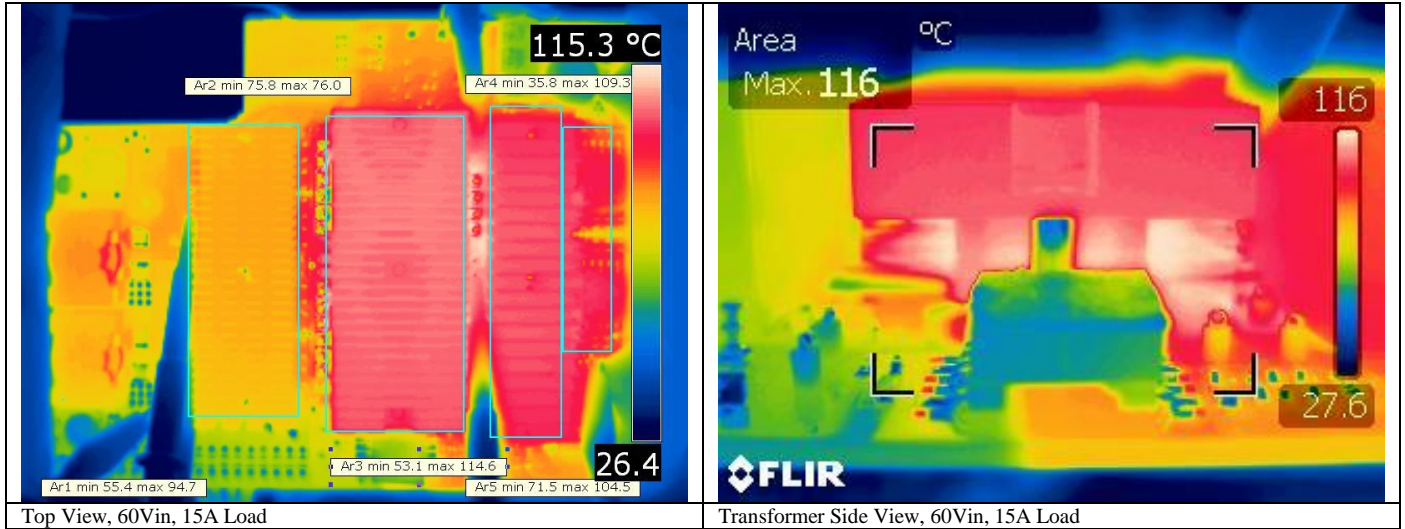
Transformer Side View, 60Vin, 15A Load



Transformer Side View, No Heat Sink

4.4 30A Load, with Heat Sinks, No Airflow

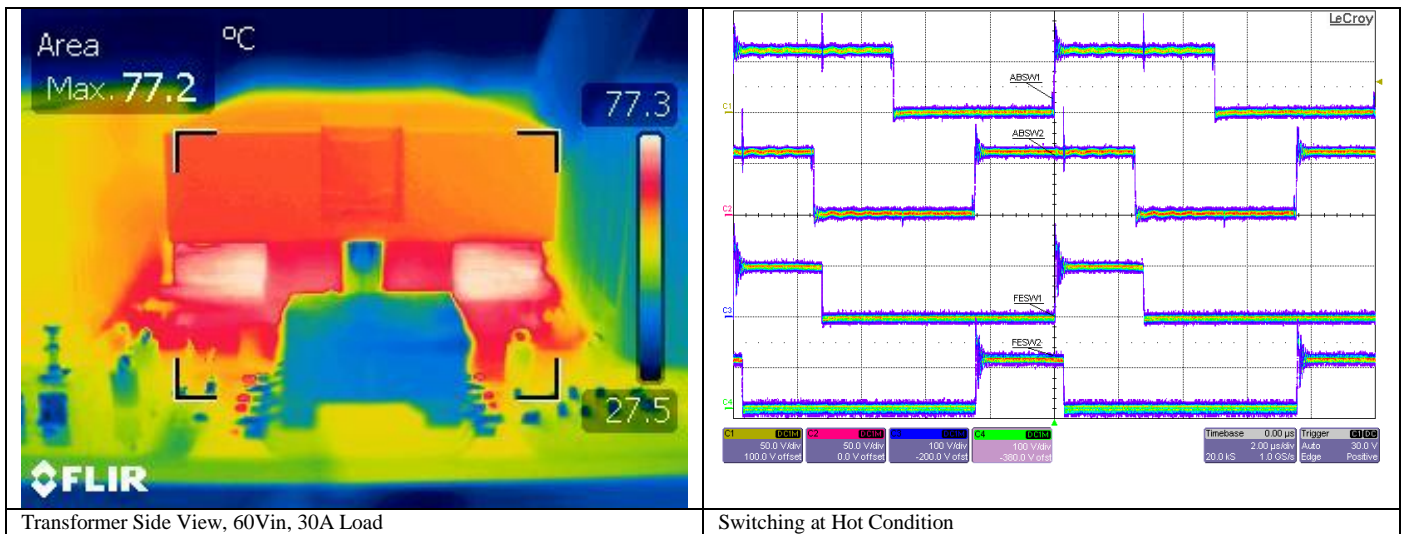
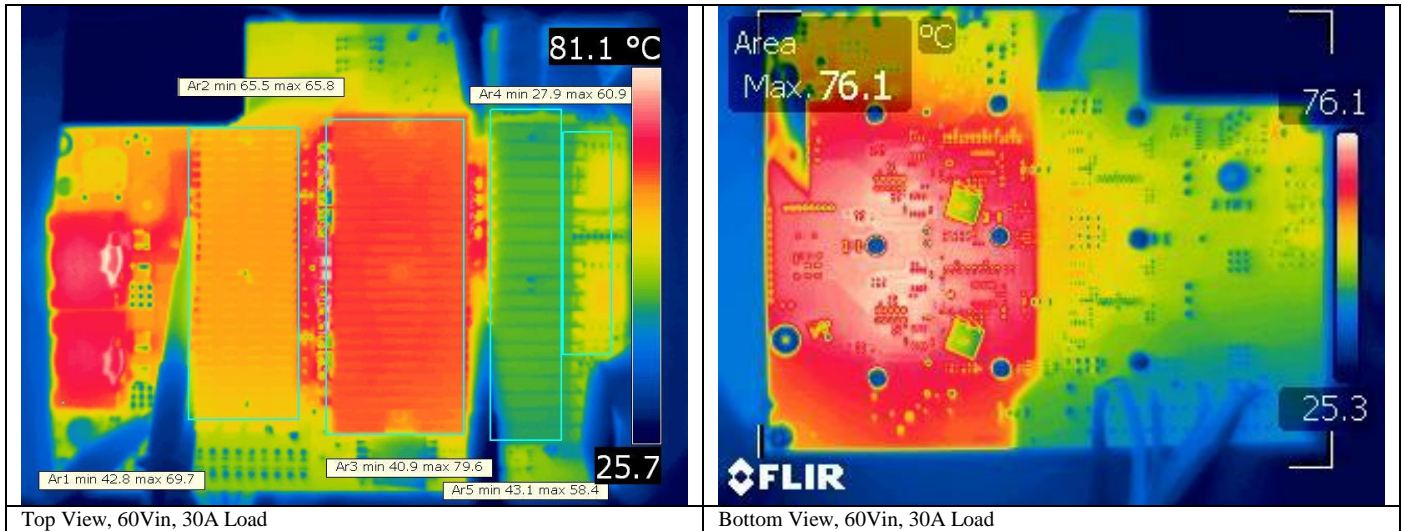
At 100% load with heat sinks and no airflow, the transformer exhibited the highest temperature rise of $116^{\circ}\text{C} - 24.2^{\circ}\text{C} = 91.8^{\circ}\text{C}$.



4.5 30A Load, with Heat Sinks, 200 LFM Airflow

At 100% load with heat sinks and airflow, the transformer exhibited the highest temperature rise of $77.2^{\circ}\text{C} - 24.3^{\circ}\text{C} = 52.9^{\circ}\text{C}$. The hot spot of 79.6°C in Area 3 is between the transformers at the snubber diodes. Switching is stable at elevated temperature, showing no evidence of jitter at the maximum input and full load condition.

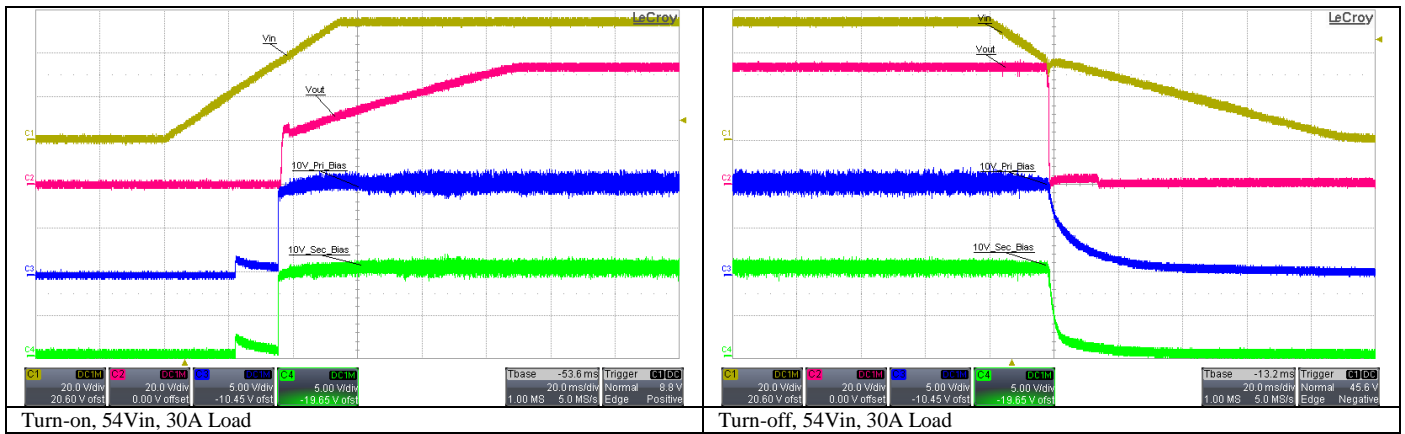
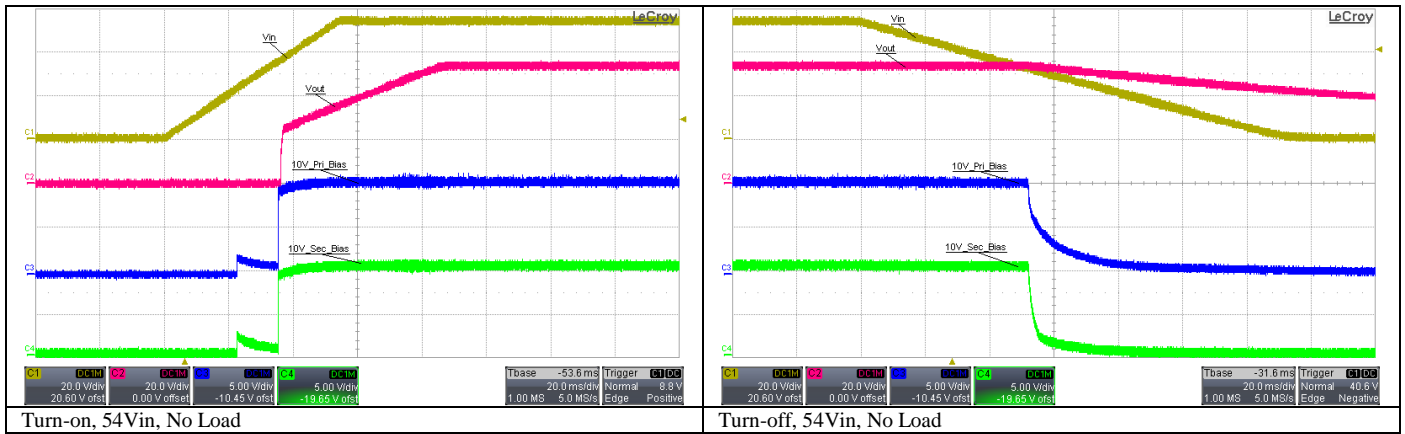
Adjustment pots on the bottom of the board were used to set the delay time, showing up as cooler square areas in the thermal image. Optimum component values are listed in the bill of material.



5 Startup and Shutdown Behavior

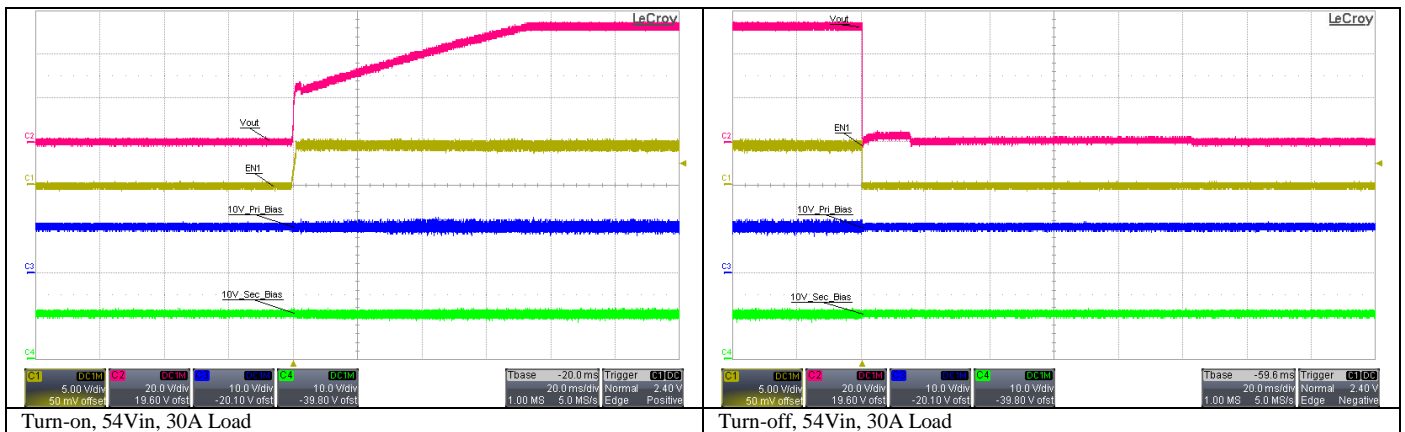
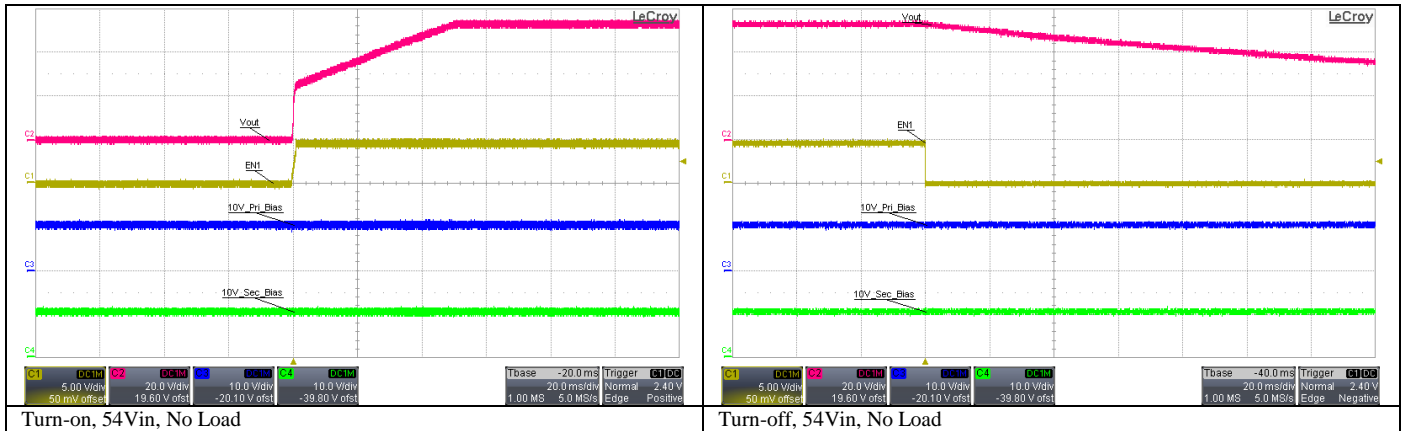
5.1 Turn-on and Turn-off from Vin

Typical turn-on is at 35V input, with turn-off at 32V. The 10V primary bias supply under-voltage lockout is set for 9.2V nominal. The output voltage is well controlled at turn-on, showing no evidence of over-shoot.



5.2 Turn-on and Turn-off from EN1

The master enable line EN1 is used to check turn-on and turn-off, showing similar output voltage characteristic as the previous tests using Vin. Note that the bias supply keeps running under this condition.

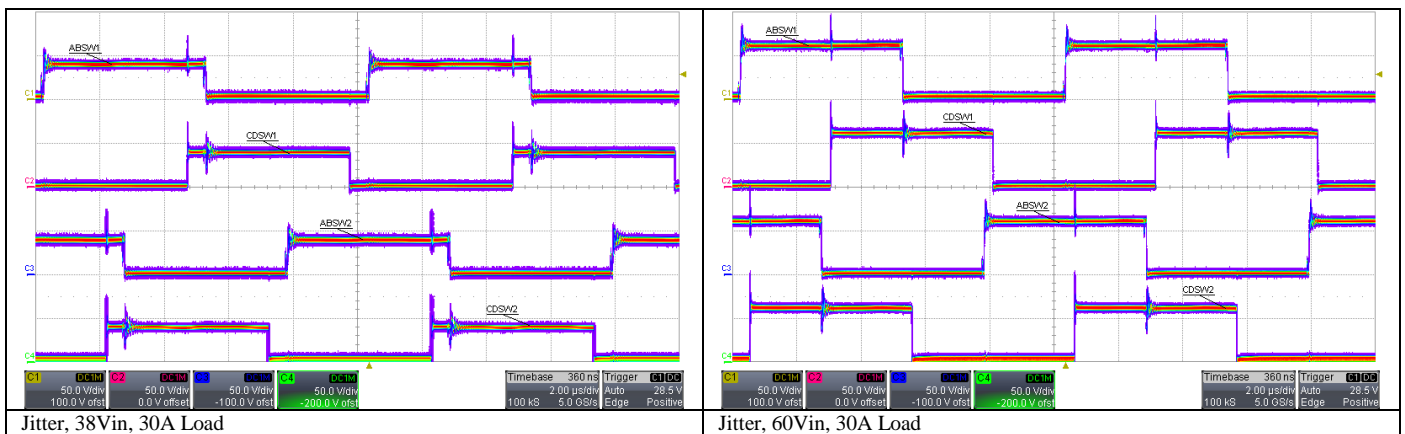
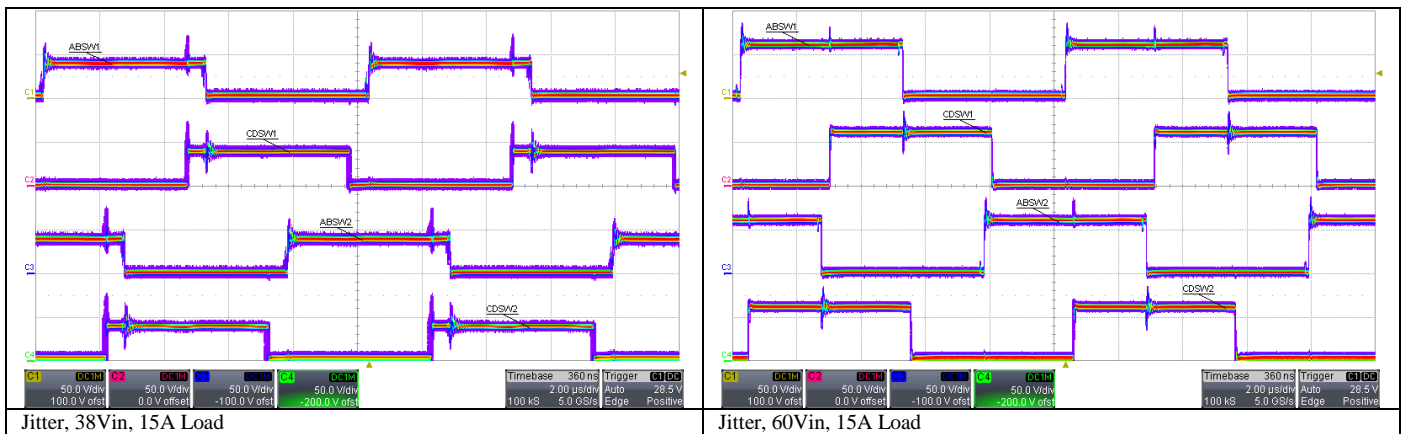


6 Switching Behavior

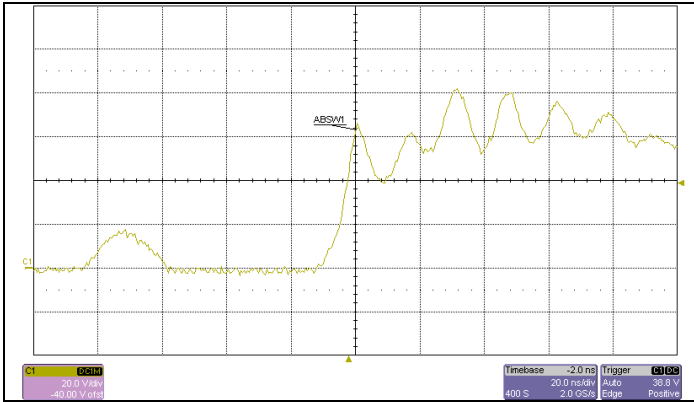
6.1 Primary Switching

The oscilloscope persistence setting is used to capture primary switching. Jitter is minimal at 38V input, with virtually none at 60V input. The nominal switching frequency is 100 kHz, with two power pulses per cycle per phase.

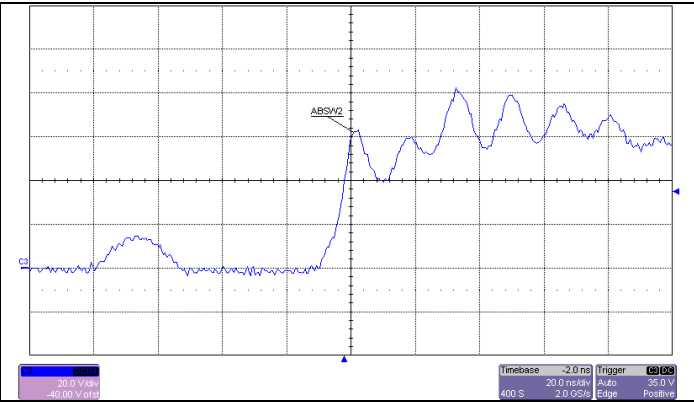
The Infineon BSC057N08NS3 G MOSFETs have a good avalanche rating of 216 mJ single pulse. Brief spikes exceeding their 80V rating are not hazardous to the proper operation of the MOSFETs. The duration of 5 ns over the 80V rating showed no evidence of avalanche during the test. Of greater concern is the LM5100 gate driver rating of 100V. Using 80V MOSFETs with avalanche rating will clamp any spikes and protect the LM5100. See the Infineon application note “The Selection of MOSFETs for DC-DC-Converters” for further information on MOSFET avalanche capability.



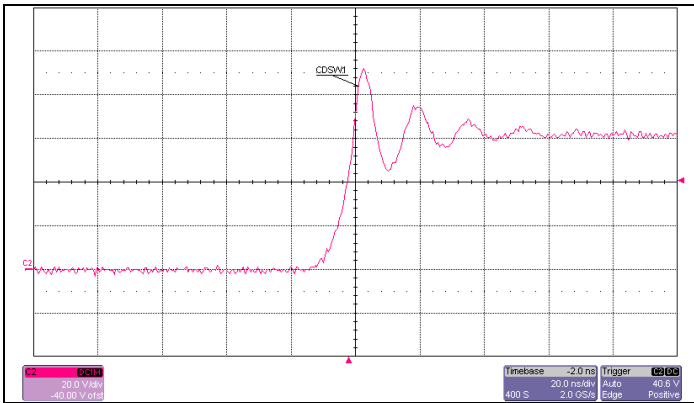
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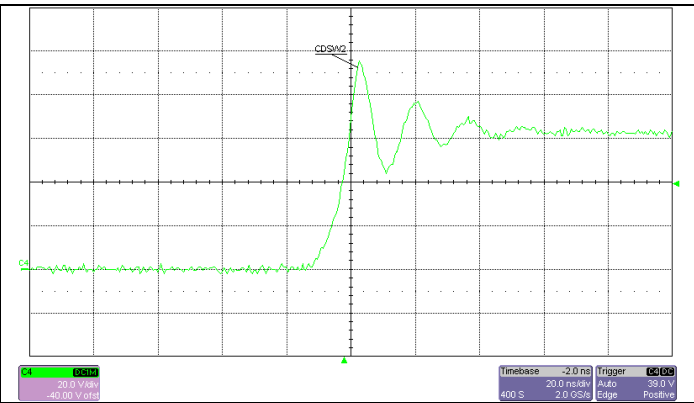
Transition and Spike, 60Vin, 30A Load



Transition and Spike, 60Vin, 30A Load



Transition and Spike, 60Vin, 30A Load



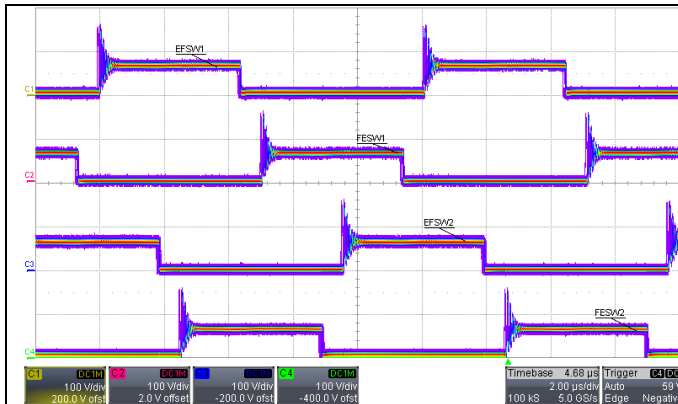
Transition and Spike, 60Vin, 30A Load

PMP6712 Rev C Test Results

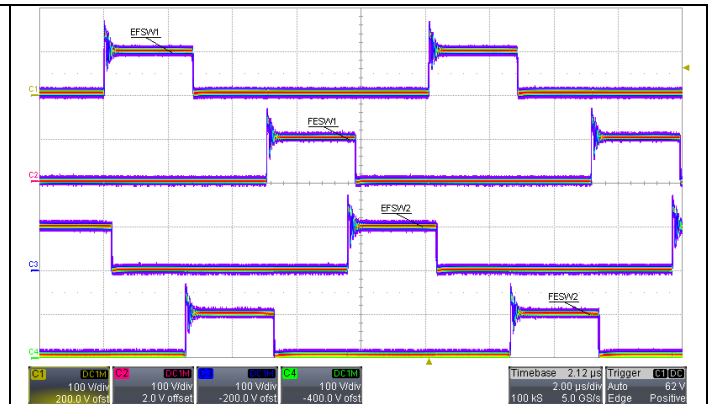
6.2 Secondary Switching

The oscilloscope persistence setting is used to capture secondary switching. Jitter is minimal at 38V input, with virtually none at 60V input. The nominal switching frequency is 100 kHz, with two power pulses per cycle per phase.

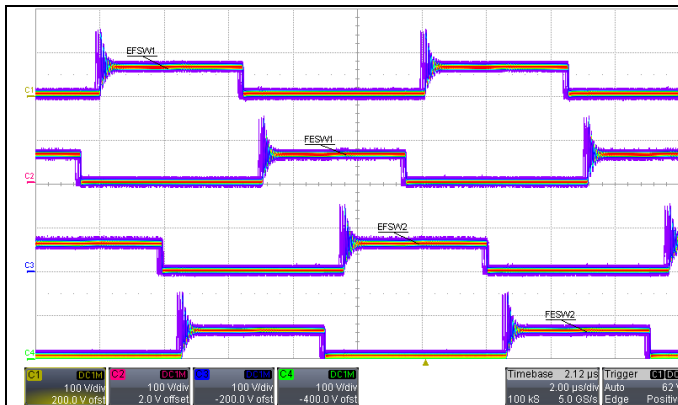
The Infineon BSC190N15NS3 G MOSFETs have a good avalanche rating of 170 mJ single pulse. Brief spikes exceeding their 150V rating are not hazardous to the proper operation of the MOSFETs. The duration of 2 ns over the 150V rating showed no evidence of avalanche during the test. Of greater concern is the MAX15013 gate driver rating of 175V. Using 150V MOSFETs with avalanche rating will clamp any spikes and protect the MAX15013. See the Infineon application note “The Selection of MOSFETs for DC-DC-Converters” for further information on MOSFET avalanche capability.



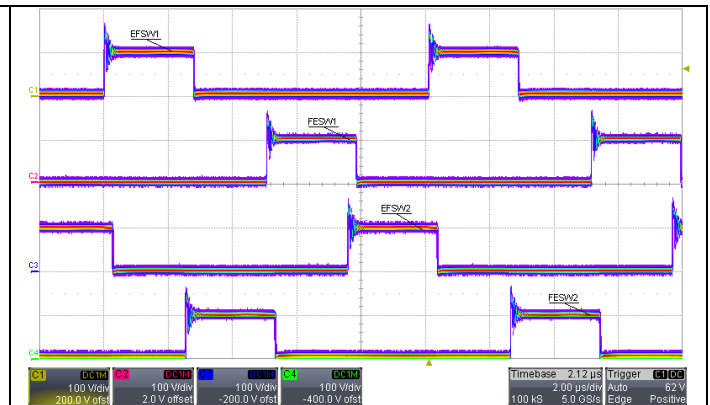
Jitter, 38Vin, 15A Load



Jitter, 60Vin, 15A Load

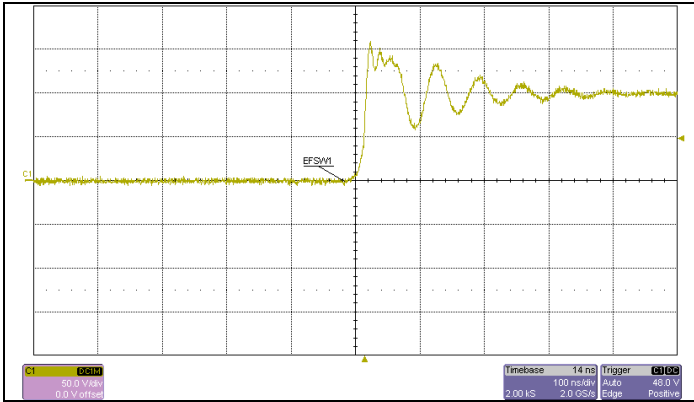


Jitter, 38Vin, 30A Load

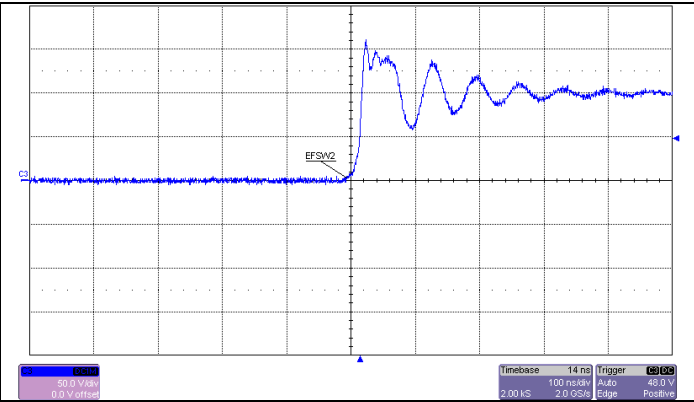


Jitter, 60Vin, 30A Load

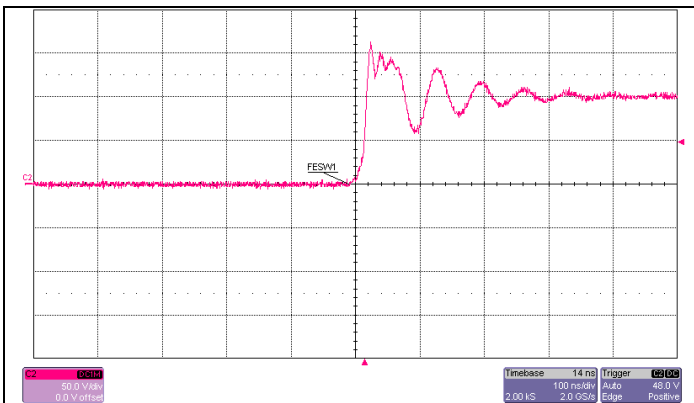
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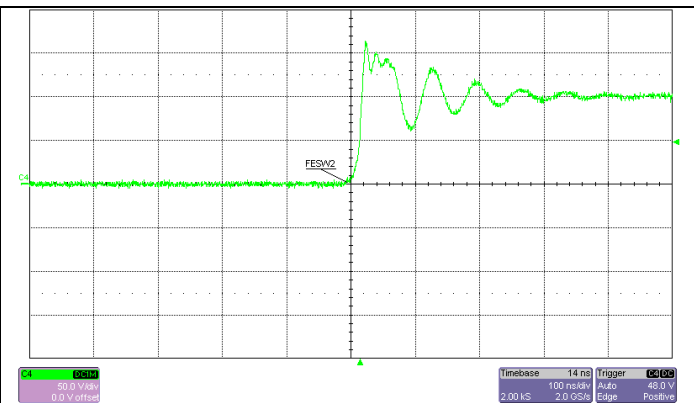
Transition and Spike, 60Vin, 30A Load



Transition and Spike, 60Vin, 30A Load



Transition and Spike, 60Vin, 30A Load

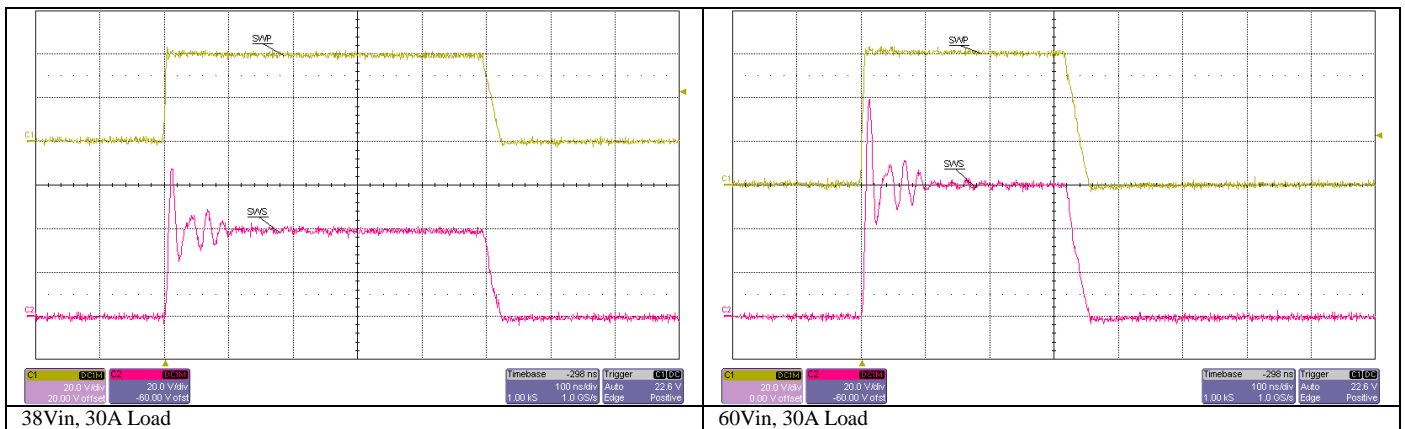
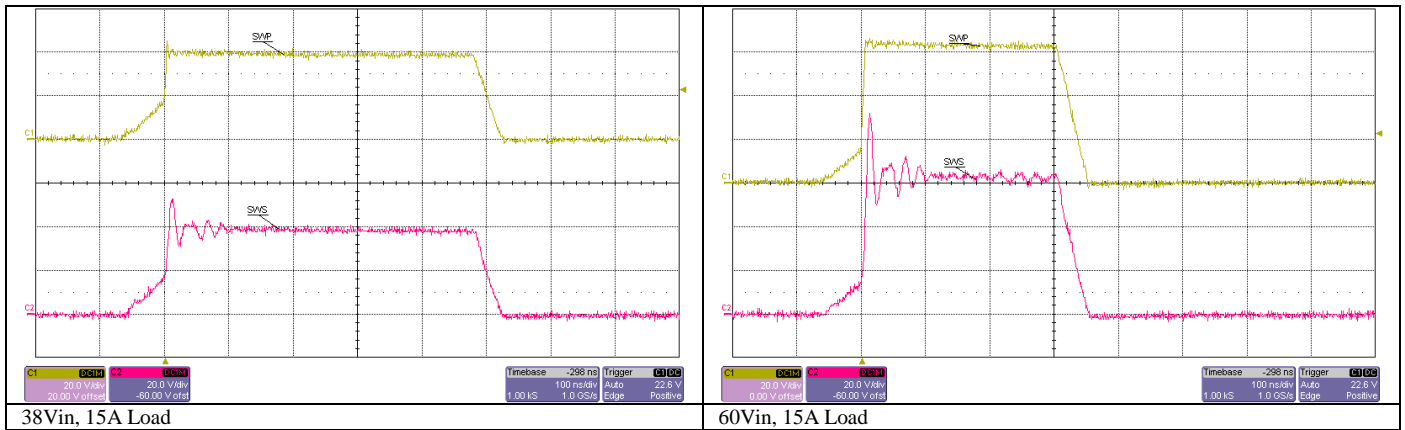


Transition and Spike, 60Vin, 30A Load

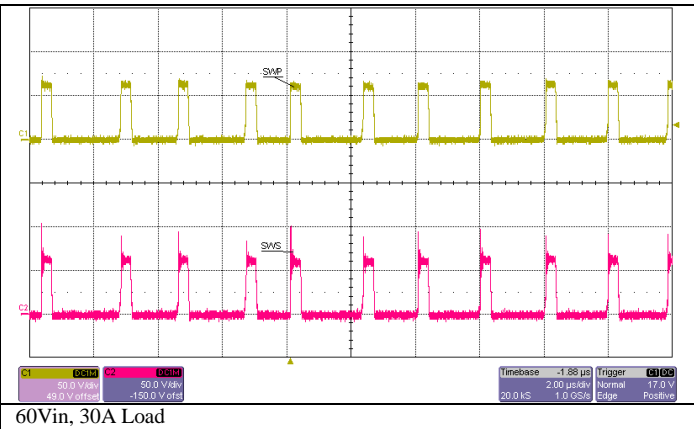
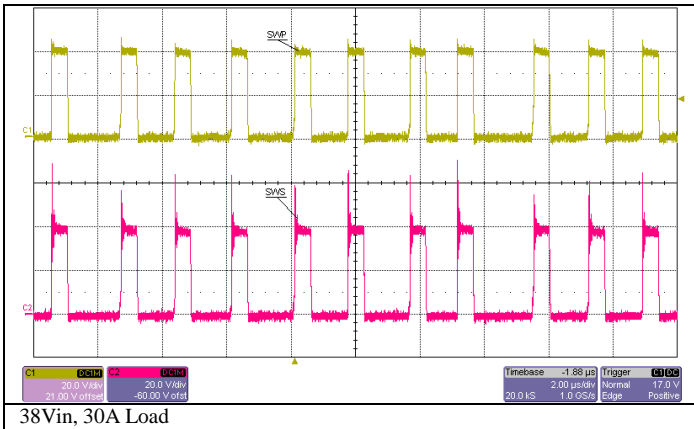
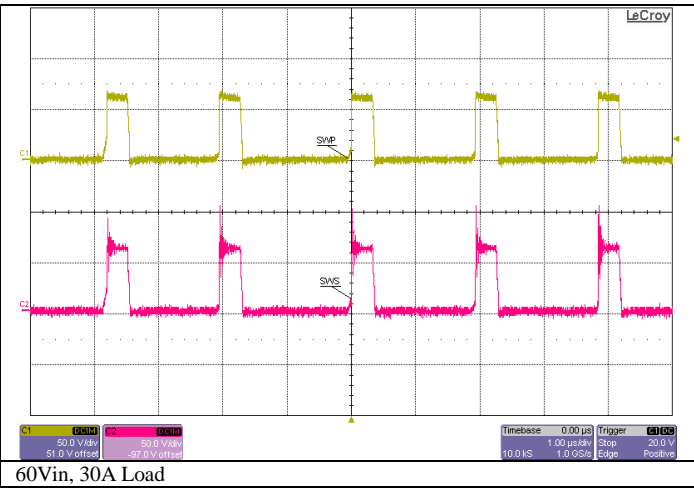
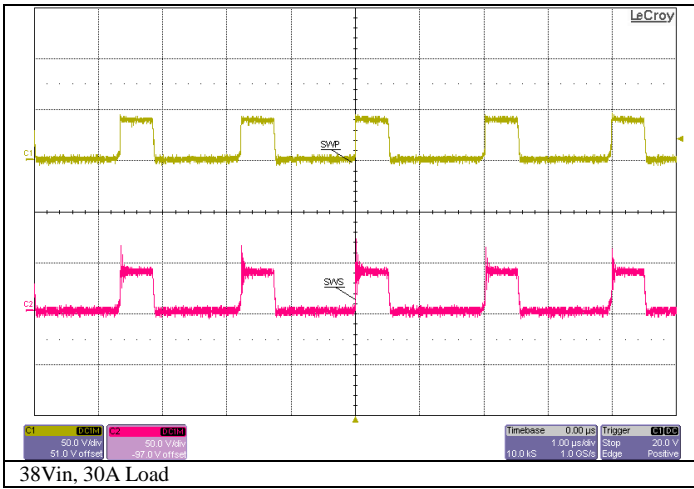
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6.3 Bias Switching

The LM5017 switching regulator sets the on-time to be proportional to the input voltage by the selection of R_{on} . Using $R_{on} = 200\text{ k}\Omega$ results in a constant switching frequency of 500 kHz. Since the feedback control is hysteretic in nature, switching is perturbed by the gate driver currents at the primary switching frequency of 100 kHz. In the event that perturbation of the bias supply switching frequency is deemed objectionable, a small inductor may be placed between the 10V primary bias supply output and the gate driver VDD supply line.



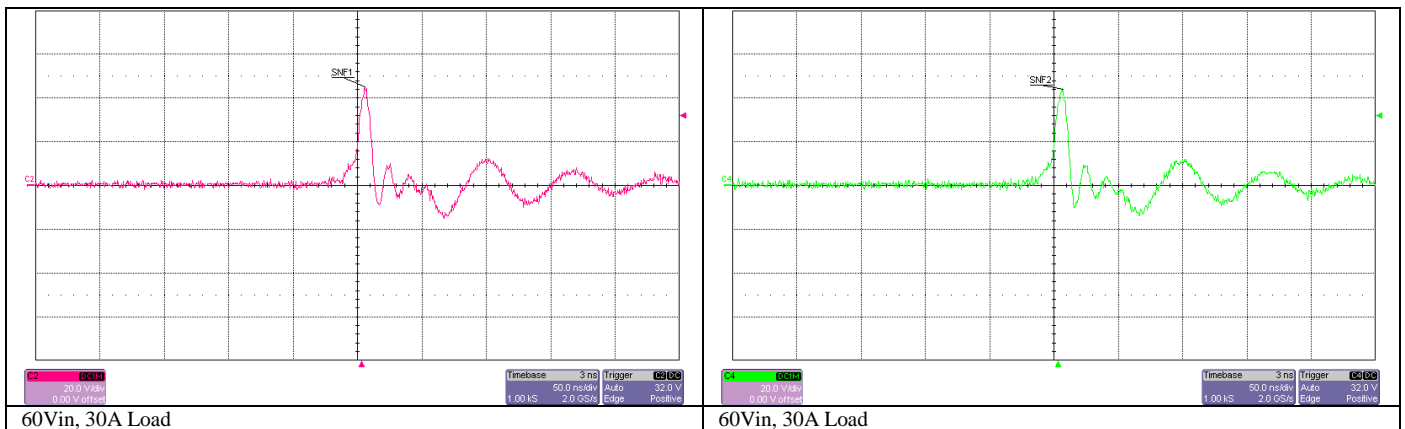
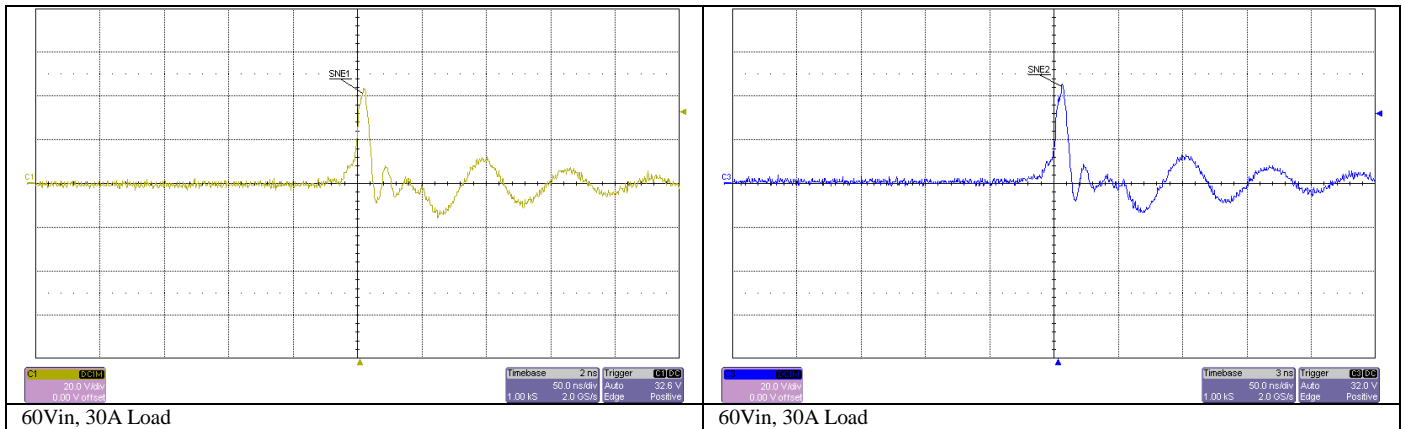
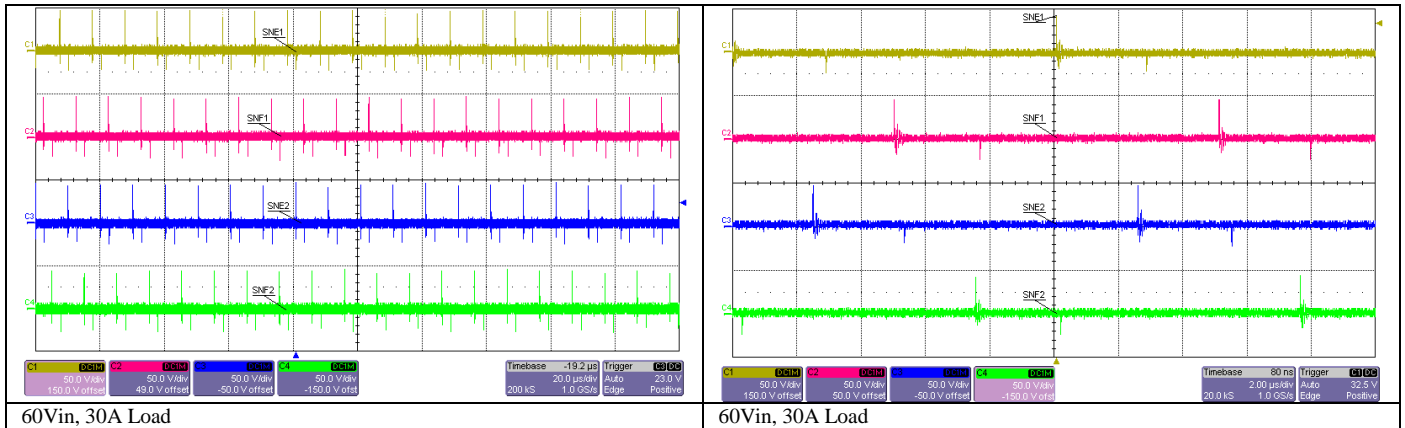
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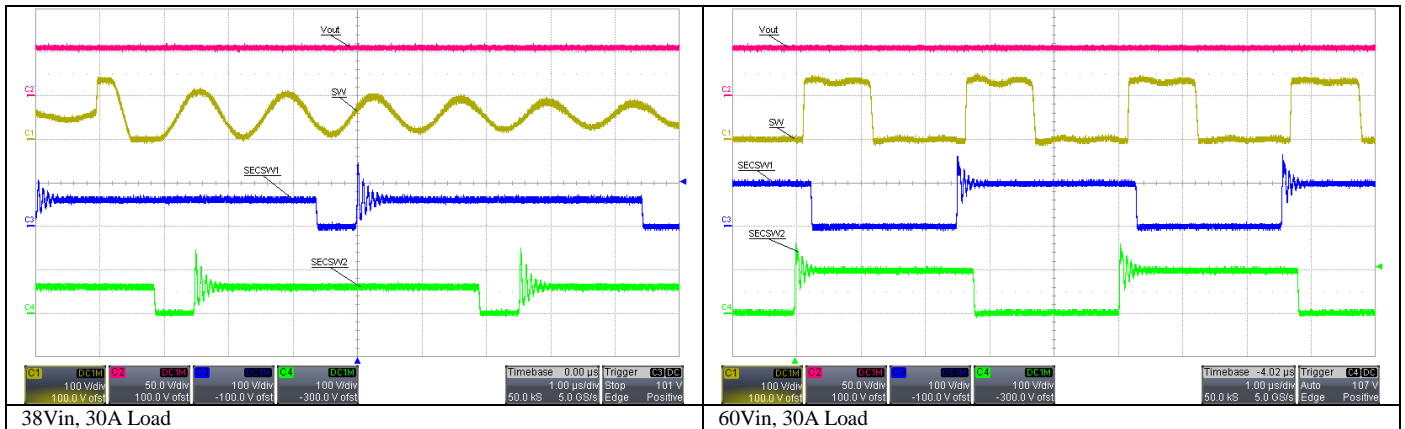
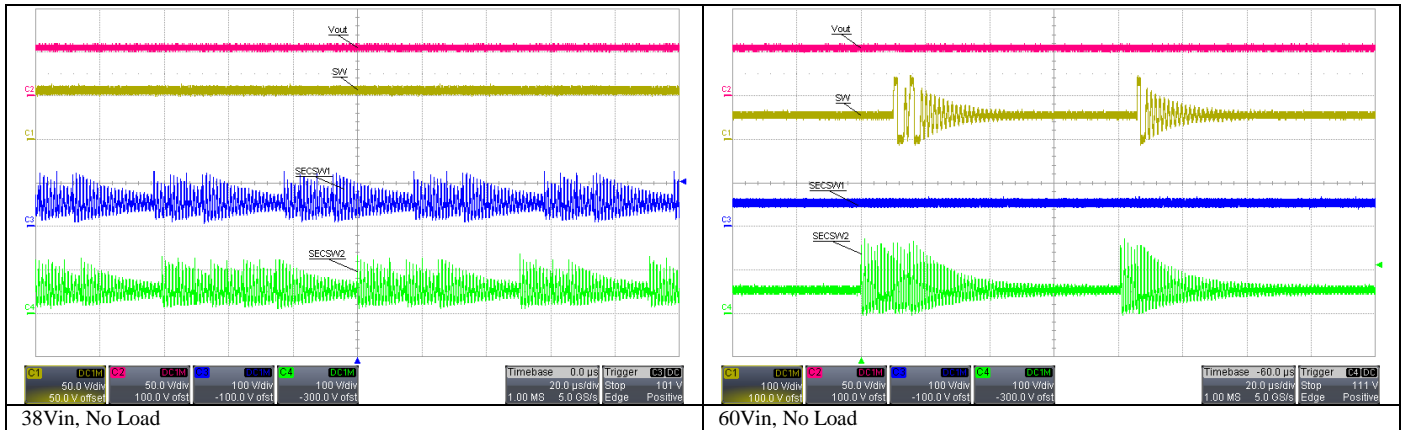
6.4 Passive Snubber Switching

Passive RC snubbers are used across the secondary-side rectifiers to control voltage spikes and ringing. The snubber power dissipation may be estimated as $P = \frac{1}{2} * C * (V_p^2 + V_n^2) * F_{sw}$, where V_p and V_n represent the positive and negative voltage spikes across the snubber resistor. From the measured spike voltages $P = \frac{1}{2} * 220 \text{ pF} * (50\text{V}^2 + 25^2) * 100 \text{ kHz} = 34\text{mW}$. This power is dissipated in the snubber resistor. Increasing the snubber capacitor will help to reduce the voltage spikes, at the expense of additional power dissipation in the snubber resistor. See the TI Power Management page on Snubber Circuit Design – Practical Tips.



6.5 Active Snubber Switching

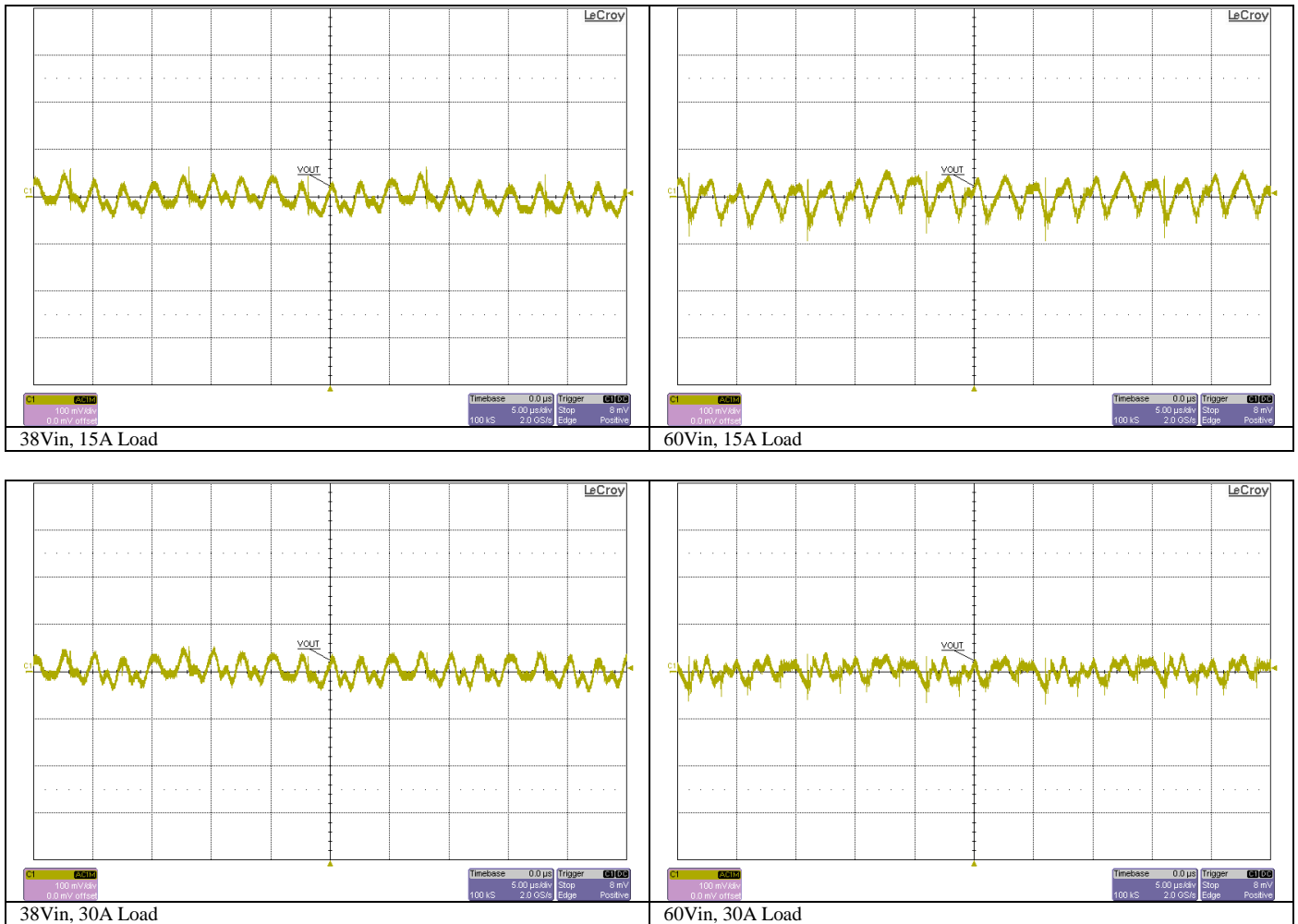
Due to the nature of the transformer and circuit parasitic elements, energy is stored in the leakage and wiring inductance each switching cycle. In order to limit the secondary peak voltage to a safe level, a diode and capacitor are used to clamp the voltage. Instead of dissipating this energy in a resistor, a hysteretic buck is used to regulate the clamp voltage to 130V and return the energy to the output. At light load, there is little or no energy stored in the snubber. At heavier load, the buck snubber switches in sync with the power stage, returning the excess energy to the output. This improves the overall efficiency by about 1% saving 16W of power.



7 Output Voltage Ripple

7.1 Output Voltage Ripple

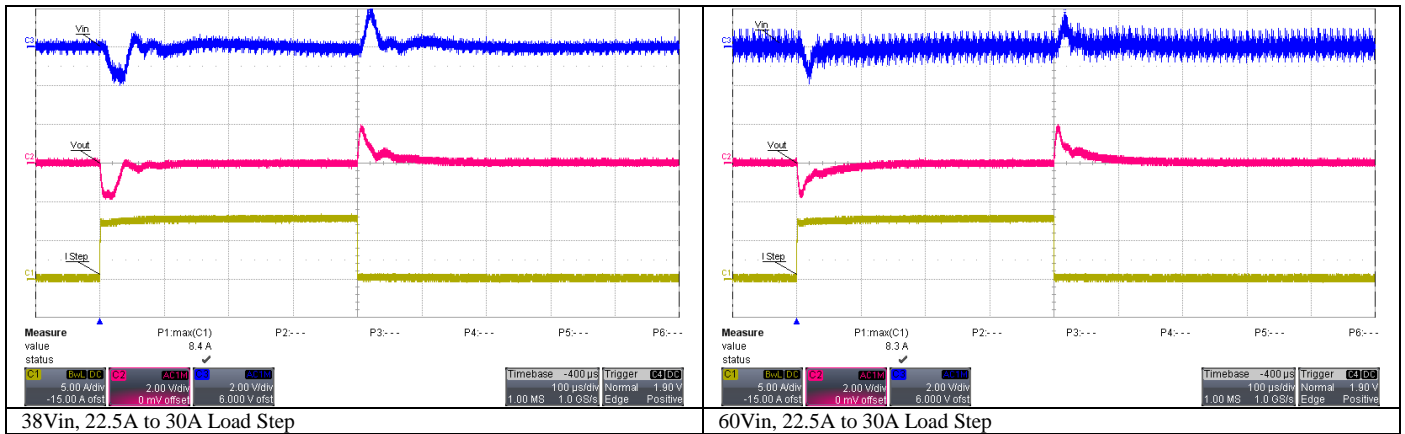
The output voltage ripple is well controlled, exhibiting 100 mV typical peak-peak at the full 350 MHz bandwidth limit of the oscilloscope and probe. The nominal switching frequency is 100 kHz, with two power pulses per cycle per phase. This results in 400 kHz output ripple frequency.



8 Load Transient Response

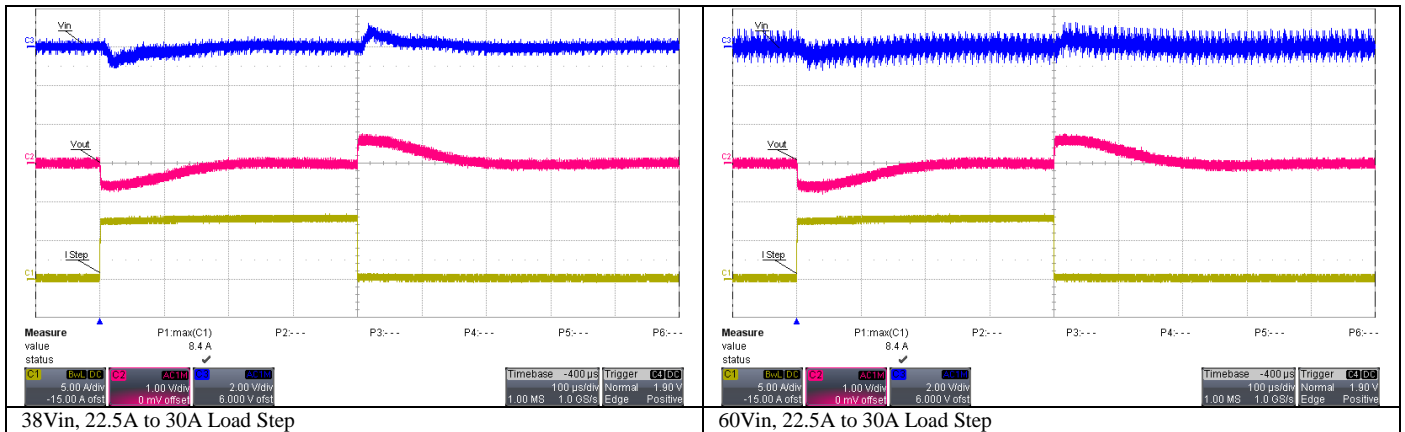
8.1 No External Capacitor

With no external capacitor, the output voltage transient is less than 2V for a 25% load step. The input voltage is also monitored to show the relative stability of the input filter.



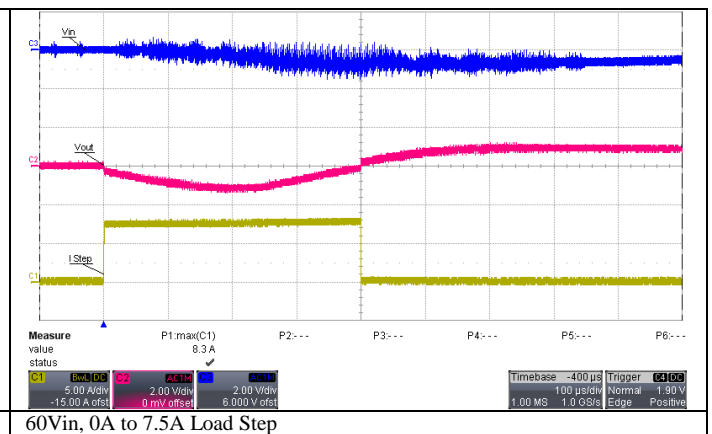
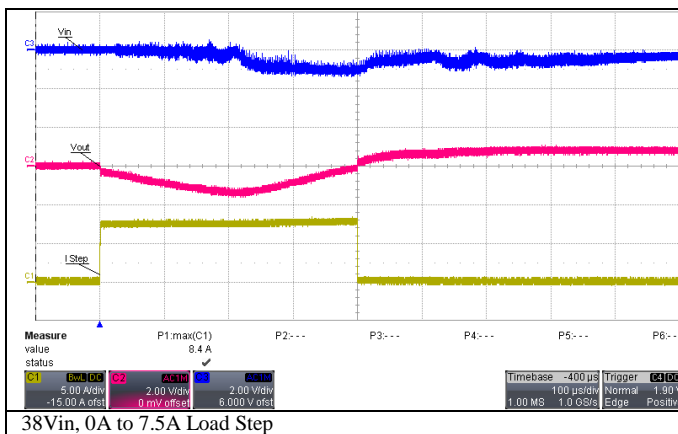
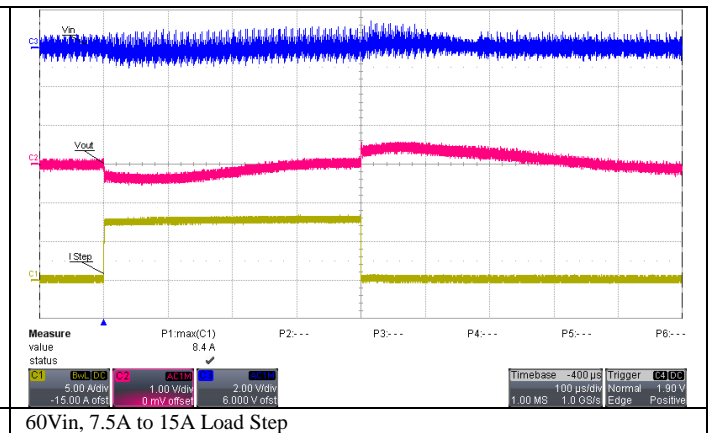
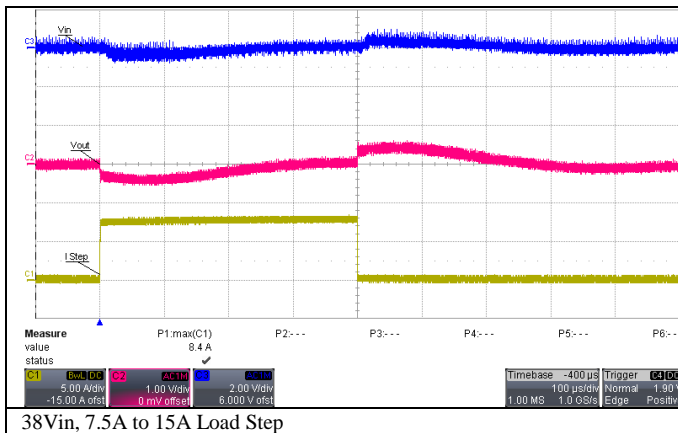
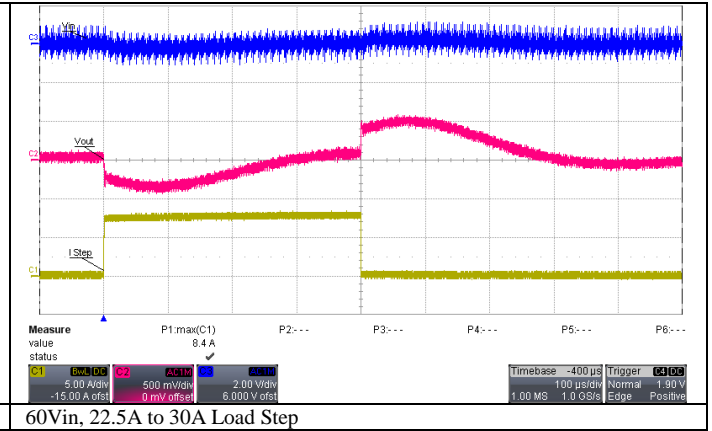
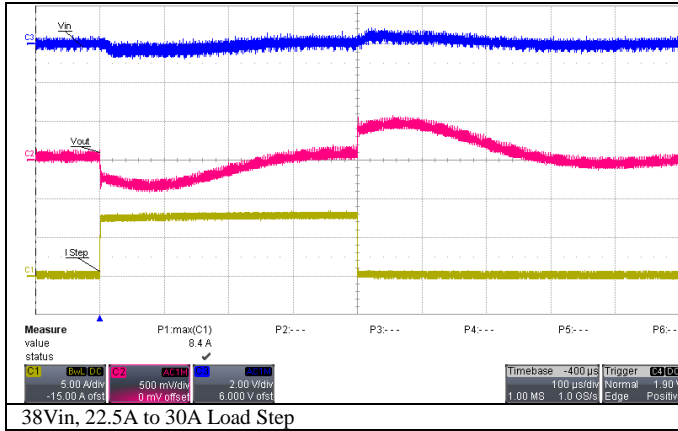
8.2 330 μ F External Capacitor

With 330 μ F external capacitor, the output voltage transient is reduced to 0.6V for a 25% load step.



8.3 1000 μ F External Capacitor

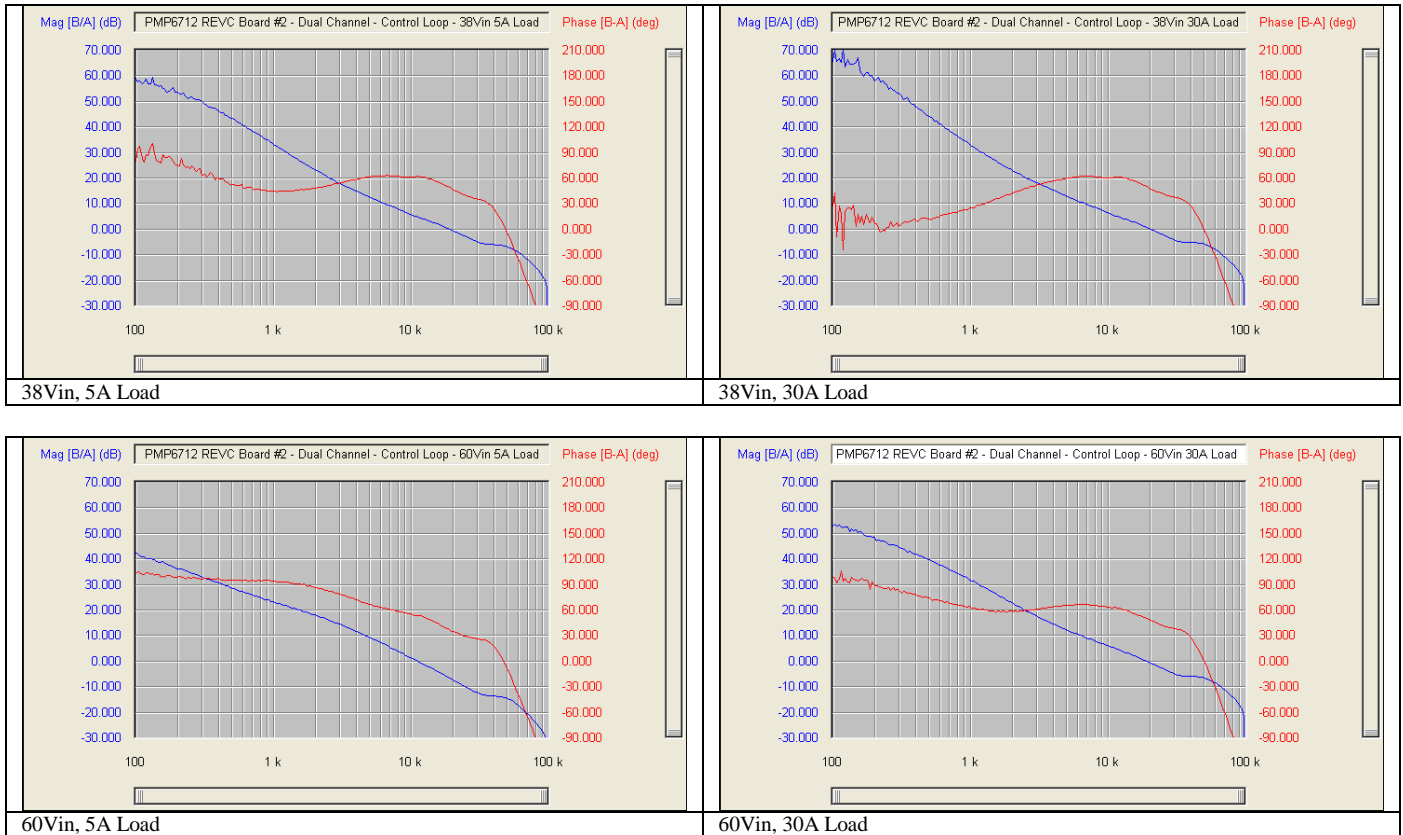
With 1000 μ F external capacitor, the output voltage transient is further reduced to less than 0.5V for a 25% load step.



9 Frequency Response

9.1 No External Capacitor

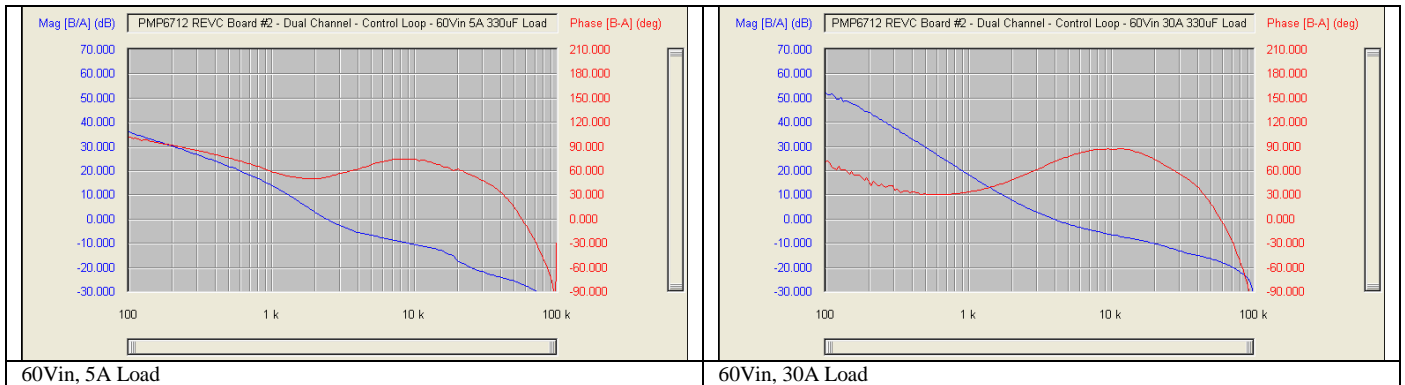
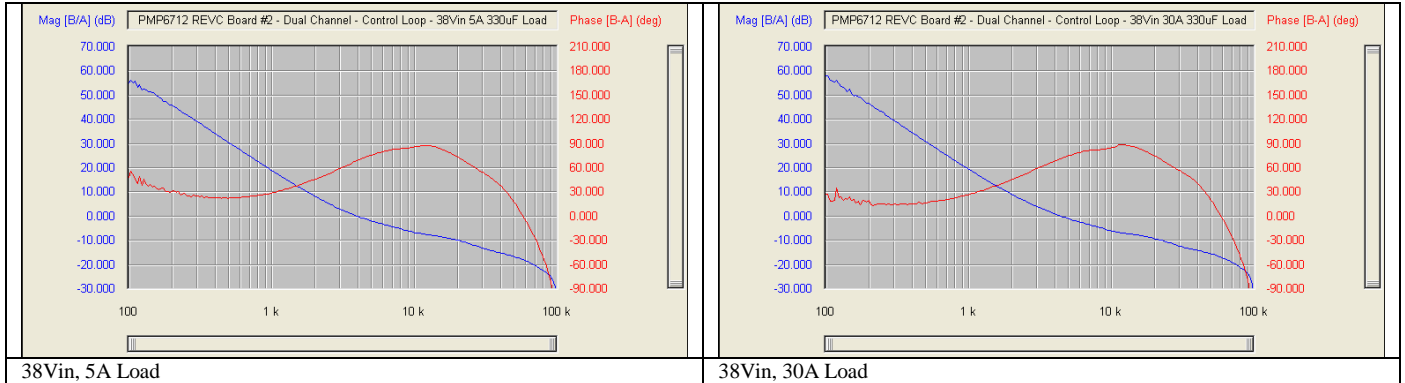
With no external capacitor, the control loop bandwidth is 20 kHz with at least 45 degrees of phase margin. This represents the practical upper limit for current-mode control bandwidth at 1/5 the switching frequency of 100 kHz. At 60V input with 5A load, discontinuous conduction mode operation lowers the overall loop gain.



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9.2 330 μ F External Capacitor

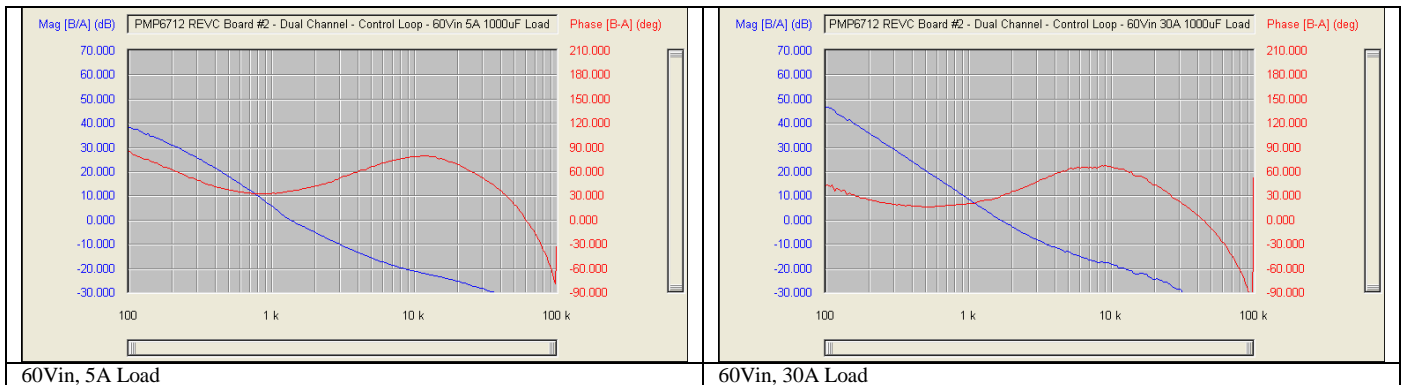
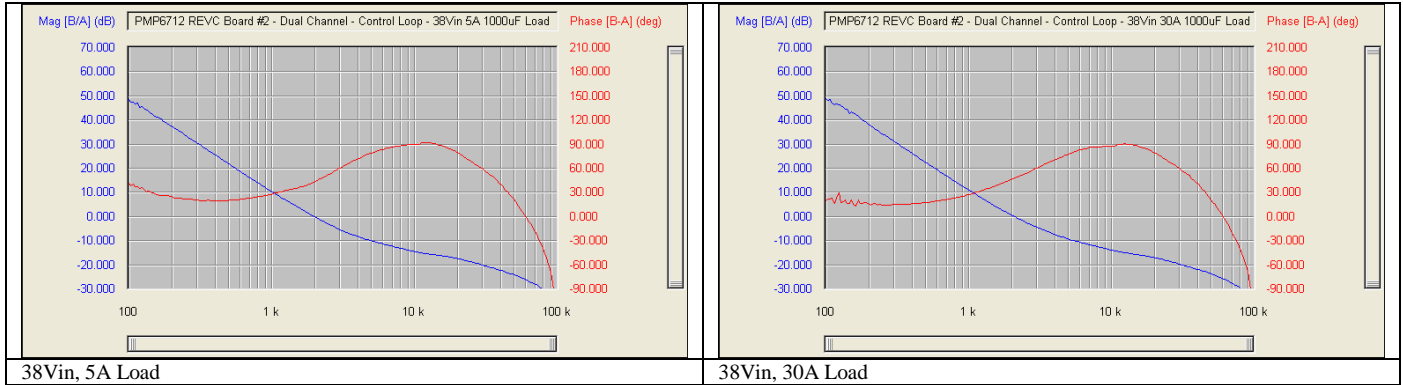
With 330 μ F external capacitor, the control loop bandwidth is reduced to 4 kHz with increased phase margin. At 60V input with 5A load, discontinuous conduction mode operation lowers the overall loop gain.



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9.3 1000 μ F External Capacitor

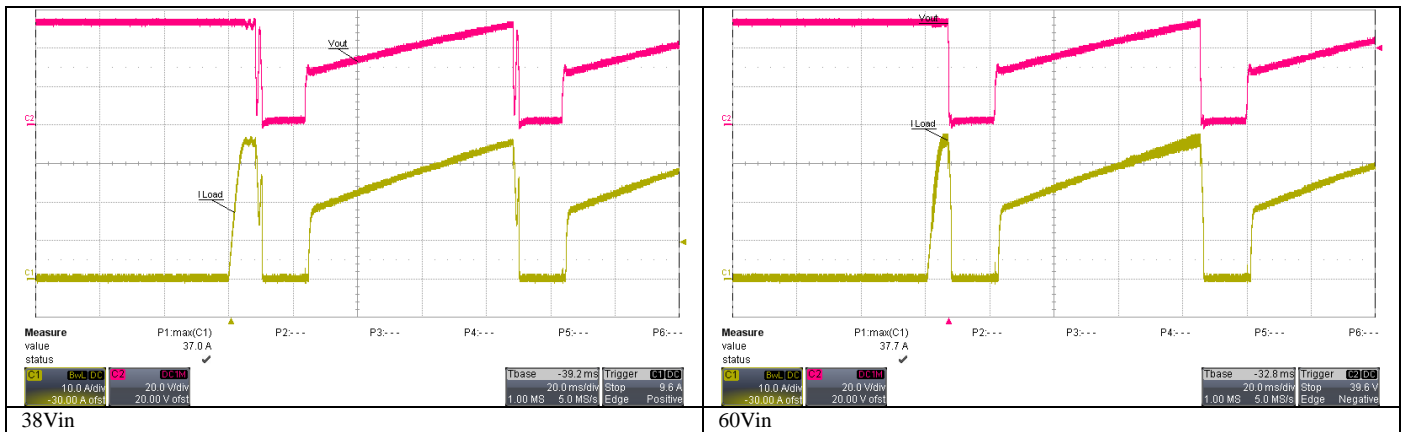
With 1000 μ F external capacitor, the control loop bandwidth is further reduced to 2 kHz, but phase margin is starting to suffer. At 60V input with 5A load, discontinuous conduction mode operation lowers the overall loop gain.



10 Over-Current Protection

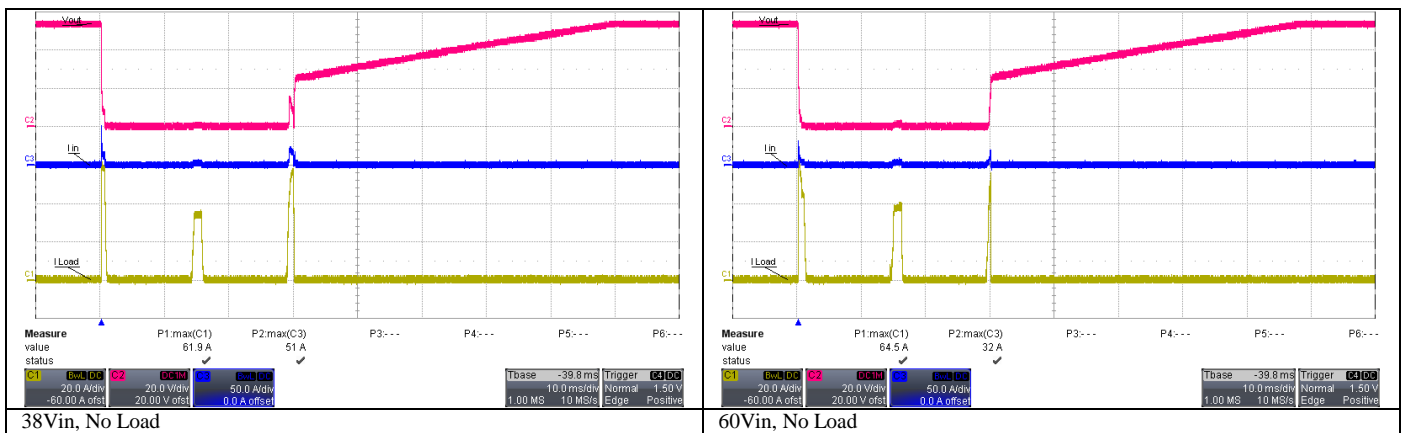
10.1 Current Limit Protection

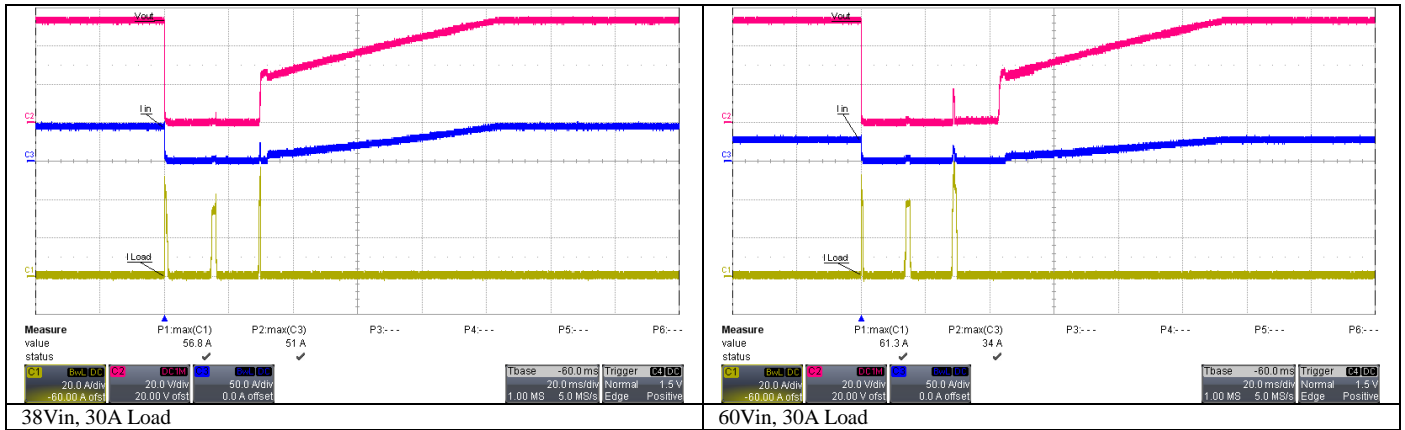
A pulsed MOSFET current limit test was performed to check the current limit threshold. The results show current limit at 37A for both 38V_{in} and 60V_{in}.



10.2 Short Circuit Protection

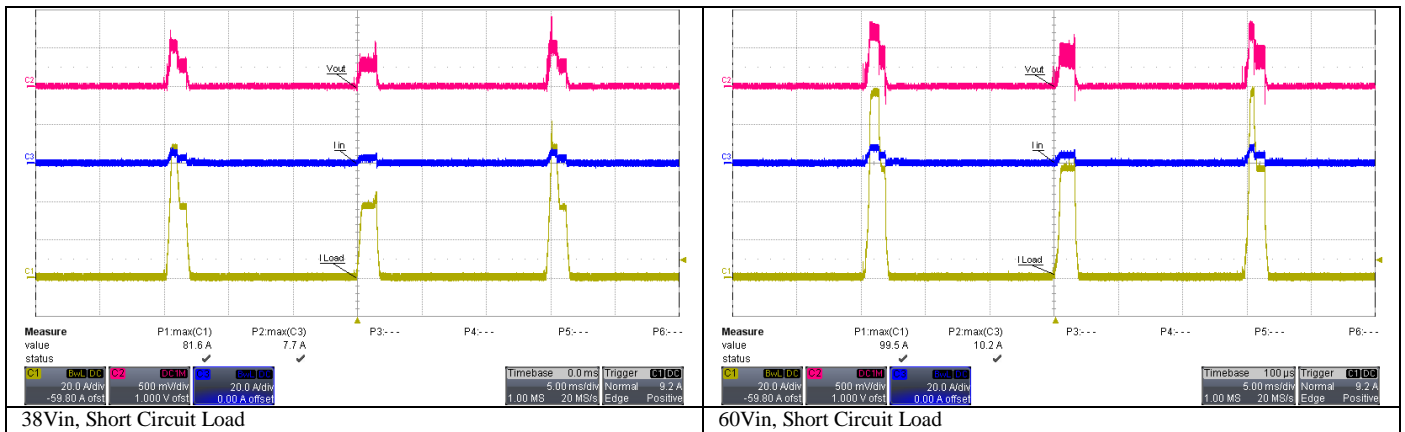
A pulsed MOSFET load was used to check short circuit protection. The results show hiccup protection with normal restart of the output voltage when the short is removed.





10.3 Short Circuit Power-Up

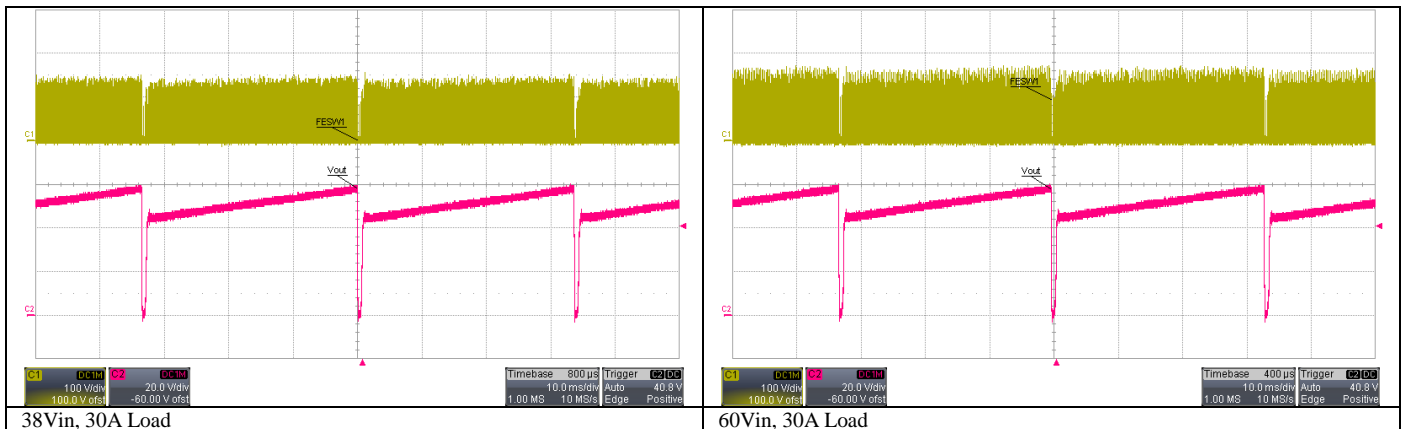
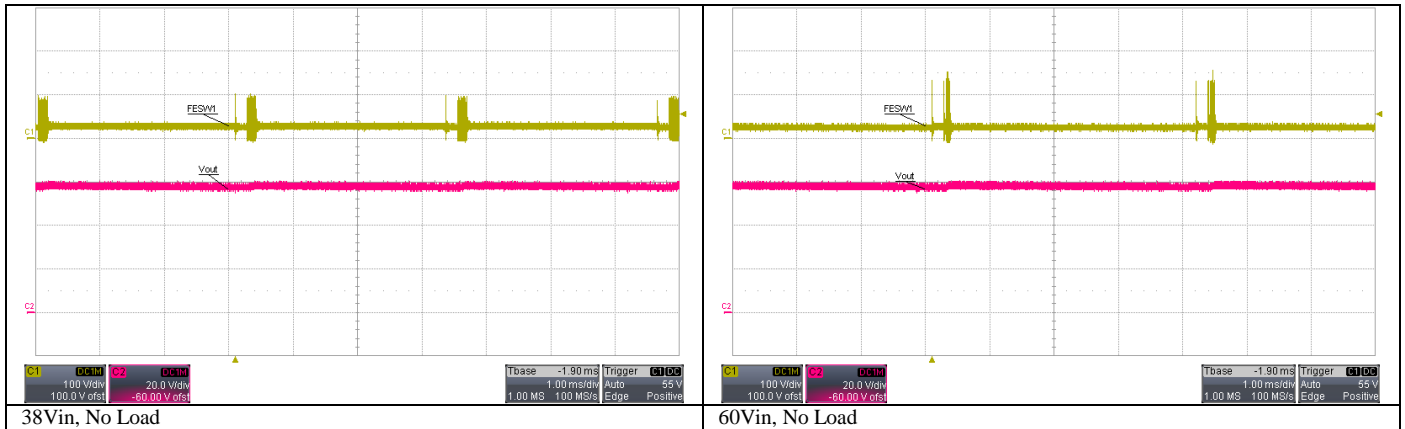
A power-up test was conducted with short circuit applied to the output. The results show normal hiccup protection.



11 Output Over-Voltage Protection

11.1 Output Over-Voltage

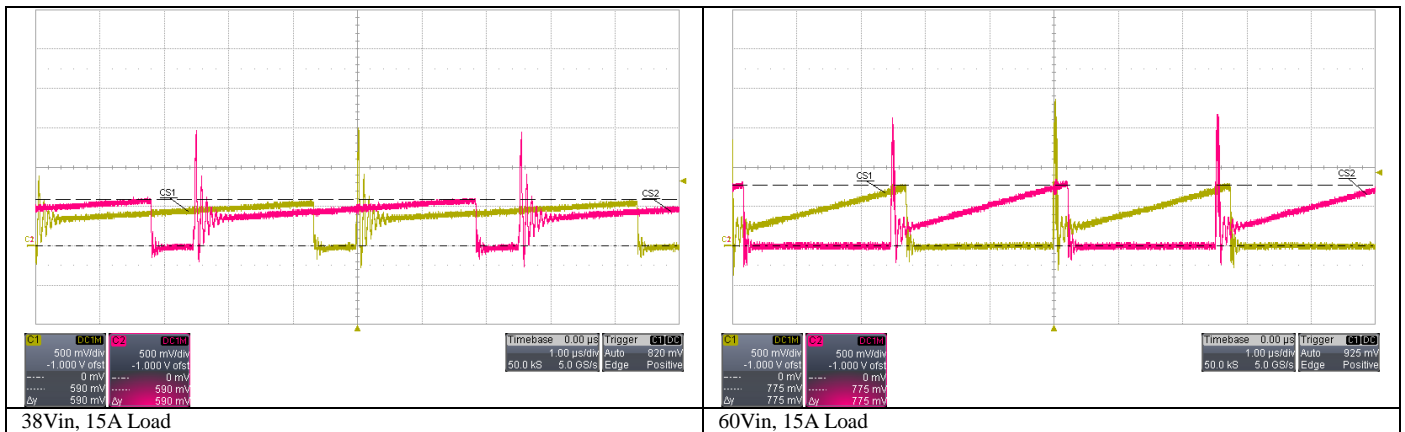
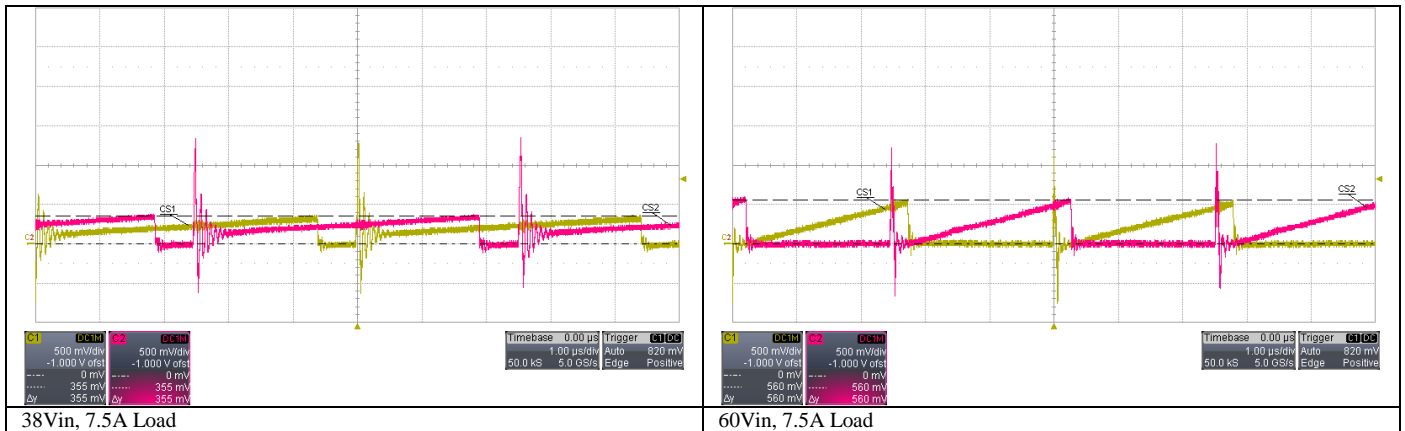
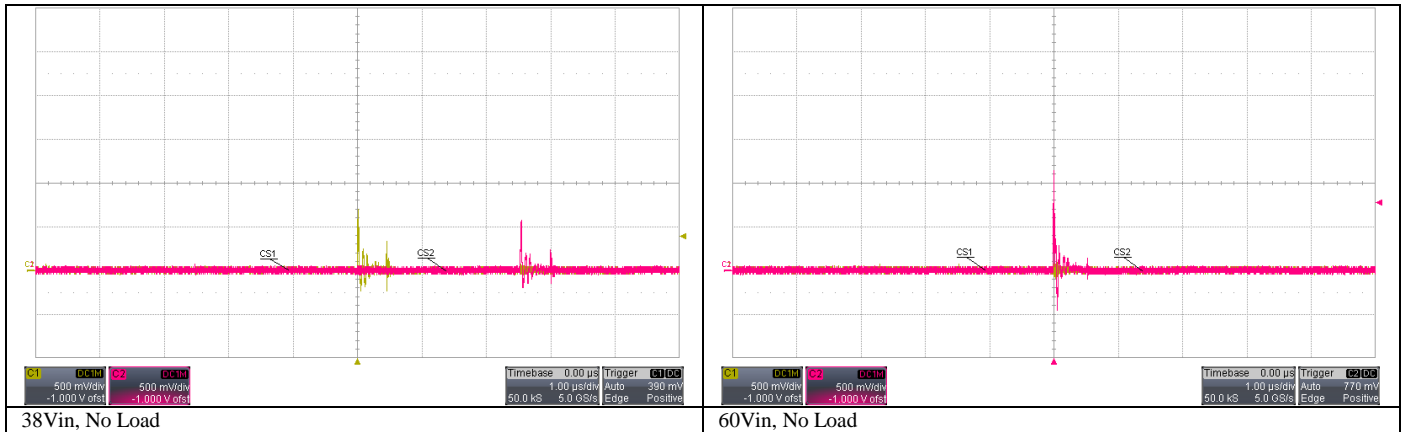
An output over-voltage test was performed by paralleling the lower feedback divider resistor with 20 kΩ. At no load, the output voltage is limited to about 59V. With load, the over-voltage protection circuit shuts down the switching with automatic restart until the fault is removed.

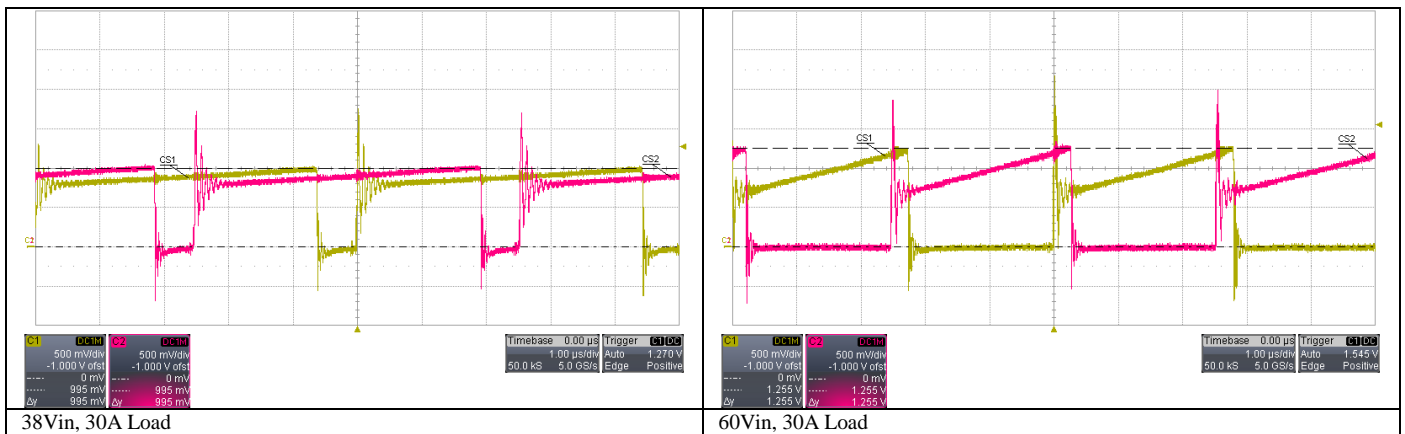
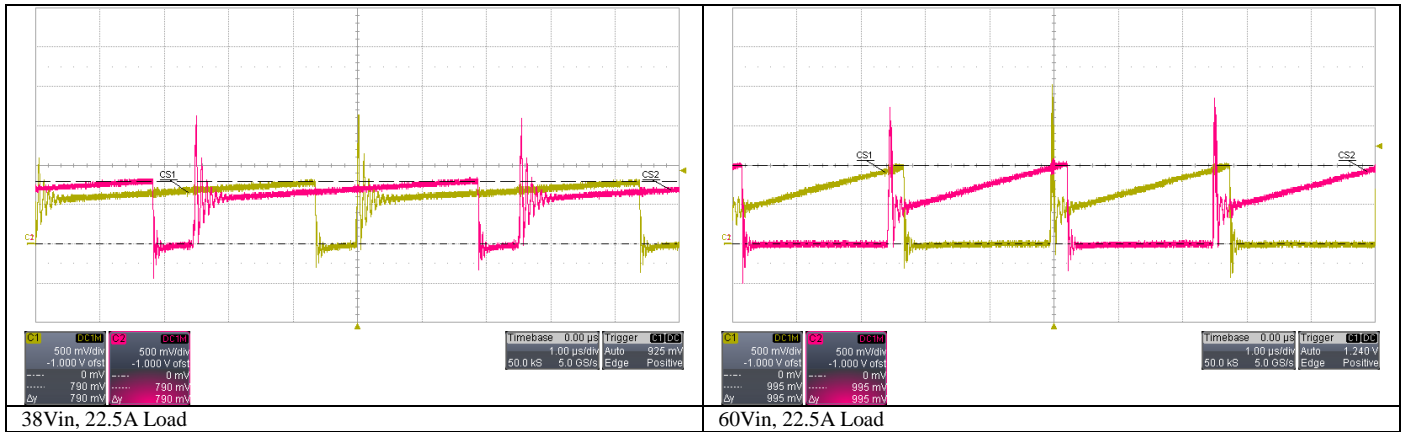


12 Current Sharing

12.1 Primary Current Sense

The primary current sense signals at each phase were monitored to evaluate the current sharing. As shown by the results, the current sense signals track very well as the load is varied from no load to 30A.





13 Bias Voltages

Bias voltages were monitored to ensure proper operation and adequate design margin. The primary bias supply is regulated to about 10.5V, with 10.2V on the secondary.

The active buck snubber is designed to regulate at about 130V. Having at least 5V available for its floating bias supply ensures adequate gate drive for the buck switch.

Bias Voltages					
Vin (V)		38	38	60	60
I Load (A)		0	30	0	30
VDDP (V)	Primary Bias Supply	10.525	10.539	10.634	10.623
VDDS (V)	Secondary Bias Supply	10.168	10.095	10.297	10.206
SNUB (V)	Snubber Voltage	112.612	132.130	131.550	131.770
SNUB-VR (V)	Snubber Bias Supply	6.709	6.274	6.702	5.034

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14 Hipot

DC tests were performed to verify the insulation resistance and safety rating. AC tests were performed to verify the integrity of the bridging capacitors. The AC voltage was reduced to keep the current within the 3mA equipment limit.

Test	AC 10 Seconds			DC 10 Seconds			Result
	Apply	Measure	Limit	Apply	Measure	Limit	
Input - Output	500 VAC 60 Hz	2.5 mA	3 mA	2250 VDC	0.3 μ A	1 μ A	Pass
Input - Chassis J7 J8	250 VAC 60 Hz	2.8 mA	3 mA	1000 VDC	0.3 μ A	1 μ A	Pass
Output - Chassis J5 J6	250 VAC 60 Hz	2.8 mA	3 mA	1000 VDC	0.3 μ A	1 μ A	Pass
Input - Heat Sink HS1	500 VAC 60 Hz	1.9 mA	2.2 mA	1000 VDC	0.4 μ A	1 μ A	Pass
Input - Heat Sink HS2	500 VAC 60Hz	1.9 mA	2.2 mA	1000 VDC	0.4 μ A	1 μ A	Pass
Output - Heat Sink HS3	500 VAC 60 Hz	1.8 mA	2.2 mA	1000 VDC	0.3 μ A	1 μ A	Pass

15 Test Equipment

Device	Manufacturer	Model
Power Supply	Chroma	62024P-80-60
Oscilloscopes	LeCroy LeCroy	WaveSurfer 434 WaveSurfer 64MXs-B
Passive Probes	LeCroy LeCroy	PP007-WS PP009-1
Current Probes	LeCroy LeCroy	CP030 CP150
Electronic Loads	Kikusui	PLZ1004W
Network Analyzer	AP Instruments	AP200
Multimeters	Agilent BK Precision	34401A 5492
Hipot Tester	QuadTech	Sentry 30+

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