Functional Safety Information

UCC21222-Q1 and UCC21330-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for UCC21222-Q1 and UCC21330-Q1 (SOIC package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

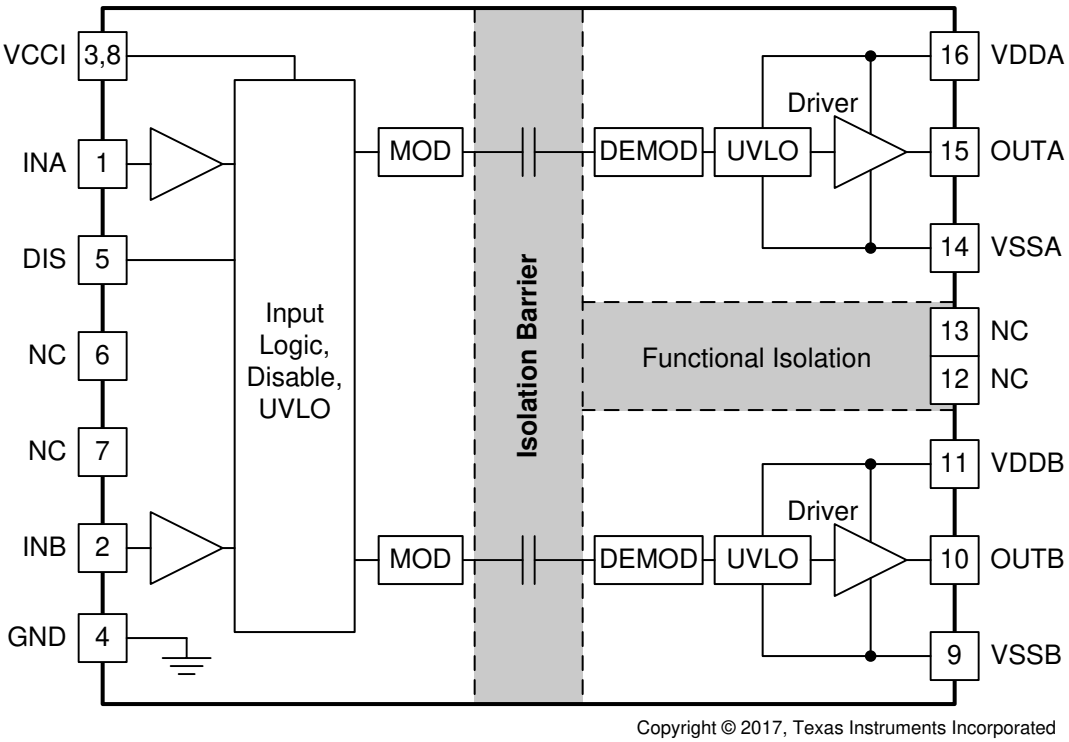

Figure 1-1. Functional Block Diagram

UCC21222-Q1 and UCC21330-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for UCC21222-Q1 and UCC21330-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10	20
	100	21
	300	23
Die FIT rate	10	2
	100	3
	300	4
Package FIT rate	10	18
	100	18
	300	19

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 10mW, 100mW, 300mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC21222-Q1 and UCC21330-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTA stuck low	15
OUTB stuck low	15
OUTA and OUTB stuck low	2
OUTA stuck high	10
OUTB stuck high	10
DT out of specified range	3
OUTA unknown or not in specified range	9
OUTB unknown or not in specified range	9
OUTA or OUTB stuck low	1
OUTA or OUTB stuck high	1
OUTA and OUTB unknown or not in specified range OUTA or OUTB unknown or not in specified range	15
No effect or distribution less than 1%	10

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC21222-Q1 and UCC21330-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the UCC21222-Q1 and UCC21330-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC21222-Q1 and UCC21330-Q1 data sheets.

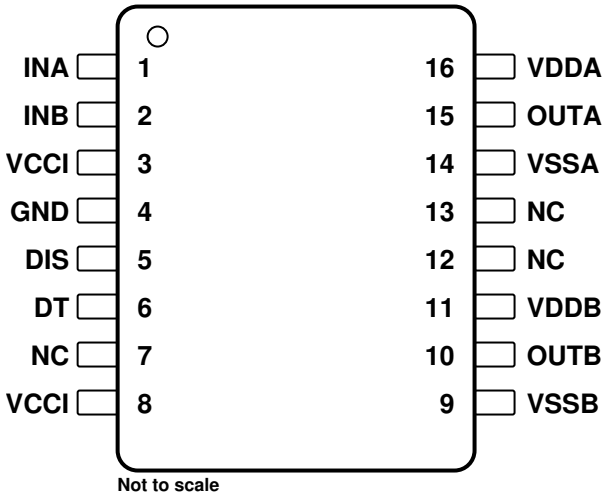

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pins 1-8, short to VCCI is considered for short circuit to supply
- Pins 13-16, short to VDDA is considered for short circuit to supply
- Pins 9-12, short to VDDB is considered for short circuit to supply
- GND is assumed to be a ground plane on the primary side
- Pins 9-12, short to VSSB is considered for short circuit to ground
- Pins 13-16, short to VSSA is considered for short circuit to ground
- Corner pin adjacent pin short, short to inner pin is considered

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
INA	1	OUTA remains low.	B
INB	2	OUTB remains low.	B
VCCI	3	Device in reset. No positive power applied to device.	B
GND	4	No effect.	D
DIS	5	DIS function not available.	B
DT	6	No dead time generated.	B
NC	7	No effect.	D
VCCI	8	Device in reset. No positive power applied to device.	B
VSSB	9	No effect.	D
OUTB	10	OUTB remains low. Possible damage to device.	A
VDDB	11	OUTB remains low.	B
NC	12	Possible isolation rating degradation.	C
NC	13	Possible isolation rating degradation.	C
VSSA	14	No effect.	B
OUTA	15	OUTA remains low. Possible damage to device.	A
VDDA	16	OUTA remains low.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
INA	1	OUTA remains low.	B
INB	2	OUTB remains low.	B
VCCI	3	No effect.	D
GND	4	Device in reset. OUTA and OUTB do not respond to INA and INB.	B
DIS	5	DIS function not available.	B
DT	6	No dead time generated.	B
NC	7	No effect.	D
VCCI	8	No effect.	D
VSSB	9	OUTB remains unknown.	B
OUTB	10	OUTB disconnected from the system.	B
VDDB	11	OUTB remains unknown.	B
NC	12	No effect.	D
NC	13	No effect.	D
VSSA	14	OUTA remains unknown.	B
OUTA	15	OUTA disconnected from the system.	B
VDDA	16	OUTB remains unknown.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to (Pin No. + 1)	Description of Potential Failure Effects	Failure Effect Class
INA	1	INB	INA and INB input level can be unknown.	B
INB	2	VCCI	OUTB remains high.	B
VCCI	3	GND	Device in reset.	B
GND	4	DIS	DIS function not available.	B
DIS	5	DT	No dead time generated.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to (Pin No. + 1)	Description of Potential Failure Effects	Failure Effect Class
DT	6	NC	No effect.	D
NC	7	VCCI	No effect.	D
VCCI	8	N/A	N/A	D
VSSB	9	OUTB	OUTB remains low. Device can be damaged.	A
OUTB	10	VDDB	OUTB remains high. Device can be damaged.	A
VDDB	11	NC	Possible isolation rating degradation.	C
NC	12	NC	Possible isolation rating degradation.	C
NC	13	VSSA	Possible isolation rating degradation.	C
VSSA	14	OUTA	OUTA remains low. Device can be damaged.	A
OUTA	15	VDDA	OUTA remains high. Device can be damaged.	A
VDDA	16	N/A	N/A	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
INA	1	OUTA remains high.	B
INB	2	OUTB remains high.	B
VCCI	3	No effect.	D
GND	4	Device in reset.	B
DIS	5	OUTA and OUTB remains low.	B
DT	6	No dead time generated.	B
NC	7	No effect.	D
VCCI	8	No effect.	D
VSSB	9	OUTB remains low.	B
OUTB	10	OUTB remains high. Device can be damaged.	A
VDDB	11	No effect.	B
NC	12	Possible isolation rating degradation.	B
NC	13	Possible isolation rating degradation.	B
VSSA	14	OUTA remains low.	B
OUTA	15	OUTA remains high. Device can be damaged.	A
VDDA	16	No effect.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2020) to Revision B (January 2025) **Page**

- Updated the document to reflect TI technical writing standards.....2
- Added UCC21330-Q1 device to document.....2

Changes from Revision * (June 2020) to Revision A (August 2020) **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document.....2

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