User's Guide
TPS62933EVM-129 3-A Regulator Evaluation Module

TEXAS INSTRUMENTS

ABSTRACT

This user's guide contains information for the TPS62933 as well as support documentation for the TPS62933 evaluation module. Included are the performance specifications, board layout, schematic, and the list of materials of the TPS62933EVM.

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1 Introduction

The TPS62933 is a high efficiency, easy-to-use synchronous buck converter. With the wide input voltage range of 3.8-V to 30-V, it is ideally suited for systems powered from 5-V, 12-V, 19-V, 24-V power-bus rails. It supports up to 3-A continuous output current, 0.8-V to 22-V output voltage and maximum 98% duty cycle operation. The device employs fixed frequency peak current control mode for fast transient response and good line & load regulation. The optimized internal loop compensation eliminates the external compensation components over a wide range of output voltage and operation frequency. The Pulse Frequency Modulation (PFM) mode maximizes the light load efficiency. The ULQ™ (Ultra Low Quiescent) feature is extremely beneficial for long battery life time in low power operation. The switching frequency can be set by the configuration of RT pin in the range of 200-kHz to 2.2-MHz, which allows optimizing system efficiency, filtering size and bandwidth.

The TPS62933EVM evaluation module (EVM) is a single, synchronous buck converter providing 5-V at 3-A from 5.1-V to 30-V input. This user's guide describes the TPS62933EVM performance. Rated input voltage and output current ranges for the evaluation module are given in Table 1-1.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS62933EVM	V_{IN} = 5.1 V to 30 V	0 A to 3 A

2 Performance Specification Summary

A summary of the TPS62933EVM performance specifications is provided in Table 2-1. Specifications are given for an input voltage of V_{IN} = 24-V and an output voltage of 5-V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. Performance Specifications Summary

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		5.1	24	30	V
Output voltage set point			5		V
Operating frequency	V_{IN} = 24 V, I_O = 3 A		500		kHz
Output current range		0		3	A
Over current limit	V_{IN} = 24 V, L_O = 6.8 µH		5		A
Output ripple voltage	V_{IN} = 24 V, I_O = 3 A		20		mV$_{PP}$

3 Modifications

These evaluation modules are designed to provide access to the features of the TPS62933. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R_4. Changing the value of R_4 can change the output voltage. The value of R_4 for a specific output voltage can be calculated using Equation 1.

$$R_4 = \frac{R_5 \times (V_{out} - 0.8)}{0.8}$$

(1)

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS62933EVM. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and shut-down.

4.1 Input/Output Connections

The TPS62933EVM is provided with input/output connectors and test points as shown in Table 4-1. Figure 4-1 shows connectors and jumpers placement on TPS62933EVM board.

A power supply capable of supplying 3-A must be connected to J2 through a pair of 20-AWG wires. The load must be connected to J1 through a pair of 20-AWG wires. The maximum load current capability is 3-A. Wire lengths must be minimized to reduce losses in the wires. Test point TP3 provides a place to monitor the V_{IN} input voltages with TP7 providing a convenient ground reference. TP1 is used to monitor the output voltage with TP9 as the ground reference.
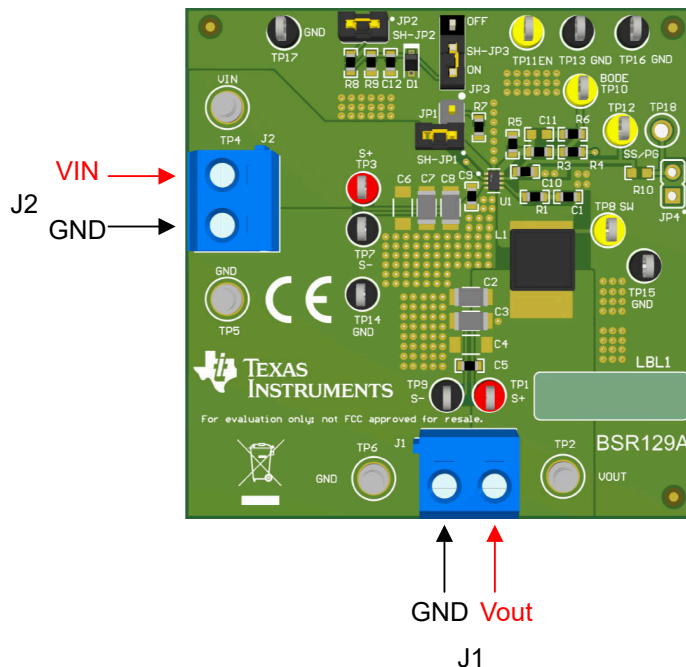

Figure 4-1. TPS62933EVM Connectors and Jumpers Placement
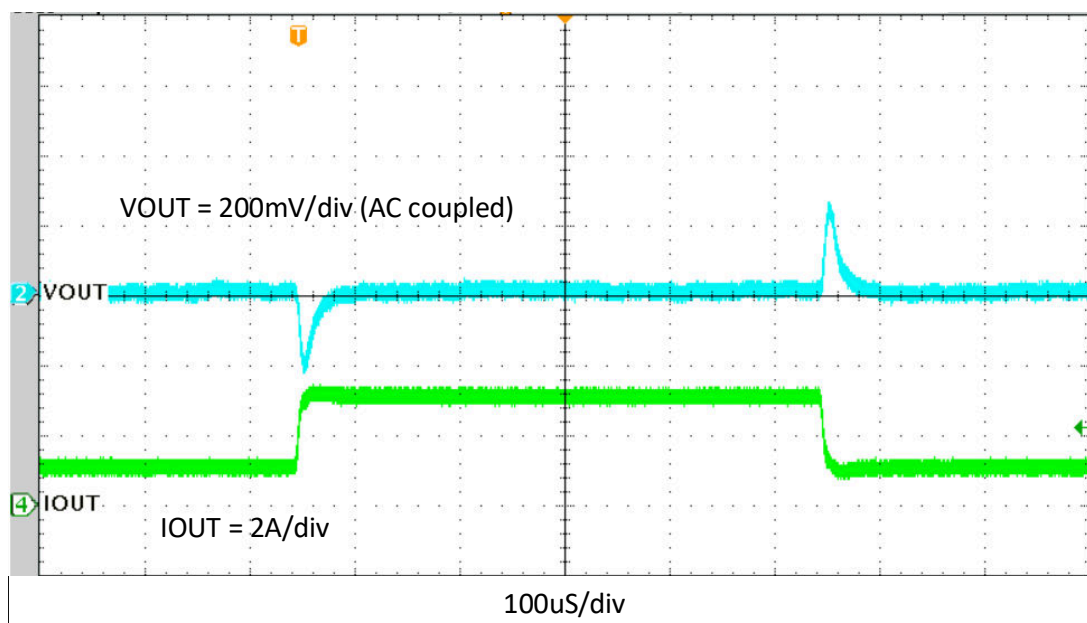
Table 4-1. Connection and Test Points

Reference Designator	Function
J1	V_{OUT}, 5V at 3-A maximum
J2	V_{IN} (see Table 1-1 for V_{IN} range)
JP1	Different frequency choice by changing the state of RT pin
JP2	V_{IN} divider
JP3	EN control. Shunt EN to GND to disable
JP4	PG or SS version choice
TP1	V_{OUT} positive monitor point
TP2	V_{OUT} positive power point
TP3	V_{IN} positive monitor point
TP4	V_{IN} positive power point
TP5, TP6	GND power point
TP7, TP9, TP13, TP14,TP15, TP16, TP17	GND monitor point
TP8	Switch node test point
TP10	Test point for loop response measurements
TP11	EN test point
TP12	SS test point
TP18	PGOOD test point

4.2 Start-Up Procedure

1. Ensure that the jumper at JP3 (Enable control) pins 2 and 3 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate V_{IN} voltage to VIN (J2-1) and GND (J2-2).
3. Move the jumper at JP3 (Enable control) pins 2 and 3 (EN and GND) to enable the output.

4.3 Load Transient Response

The TPS62933EVM response to load transient is shown in Figure 4-2 and Figure 4-3. The current steps and slew rates are indicated in the figures with 20MHz scope bandwidth. Total peak-to-peak voltage variation is as shown.

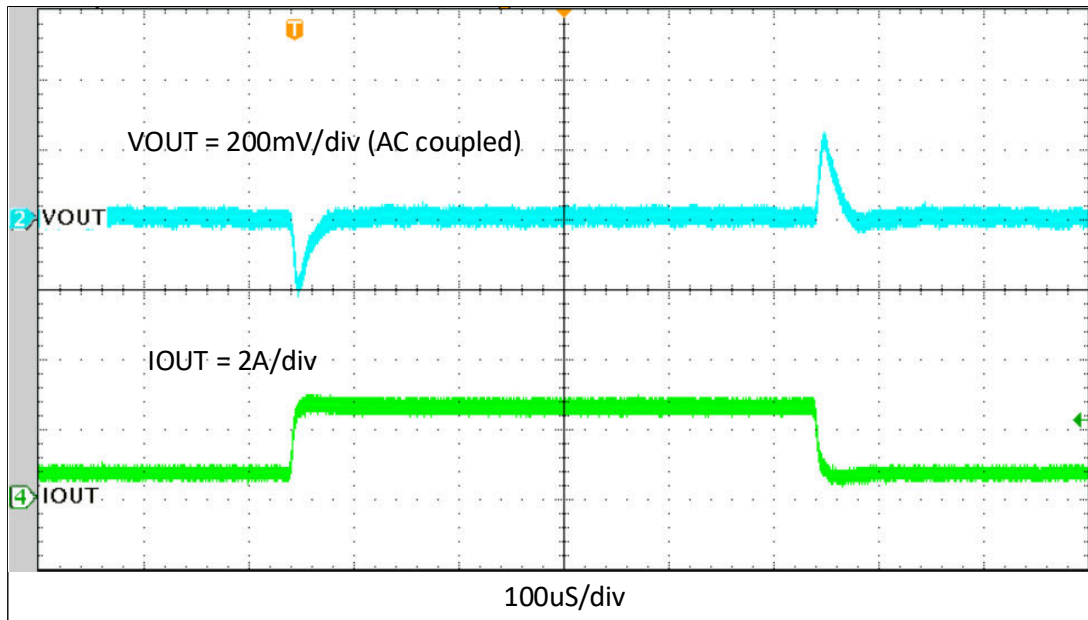**Figure 4-2. TPS62933EVM Load Transient Response, 1 A - 3 A Load Step, 0.8 A/µs**

Figure 4-3. TPS62933EVM Load Transient Response, 0.5 A - 2.5 A Load Step, 0.8 A/µs

4.4 Output Voltage Ripple

The TPS62933EVM output voltage ripple is shown in Figure 4-4, Figure 4-5, Figure 4-6, Figure 4-7, Figure 4-8 and Figure 4-9. The output currents are as indicated and all waveforms are with 20MHz scope bandwidth.
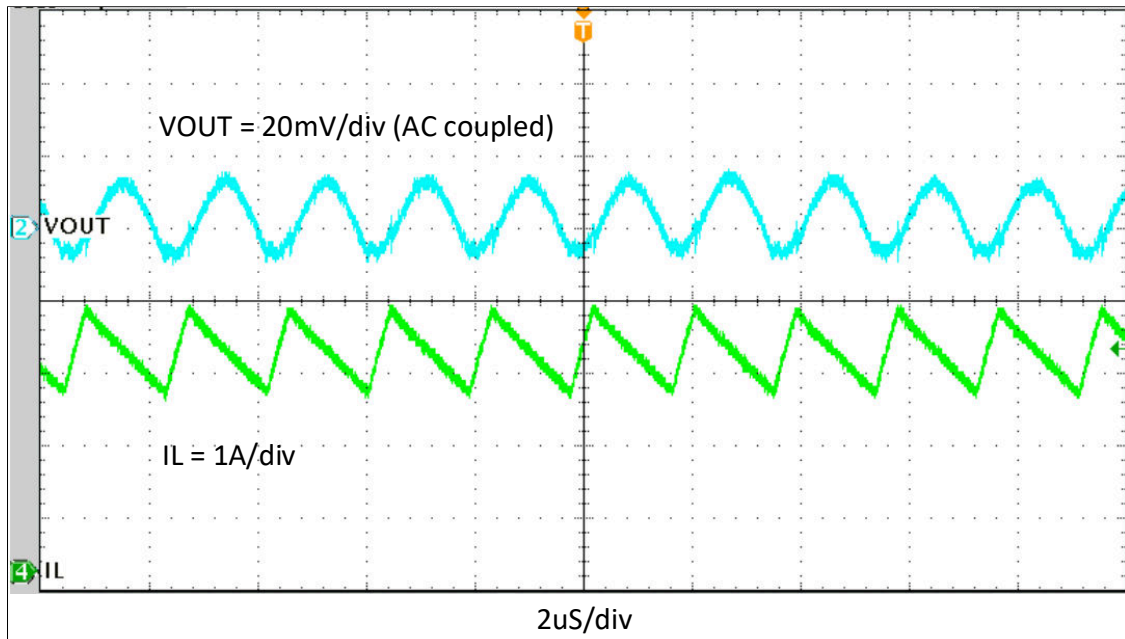
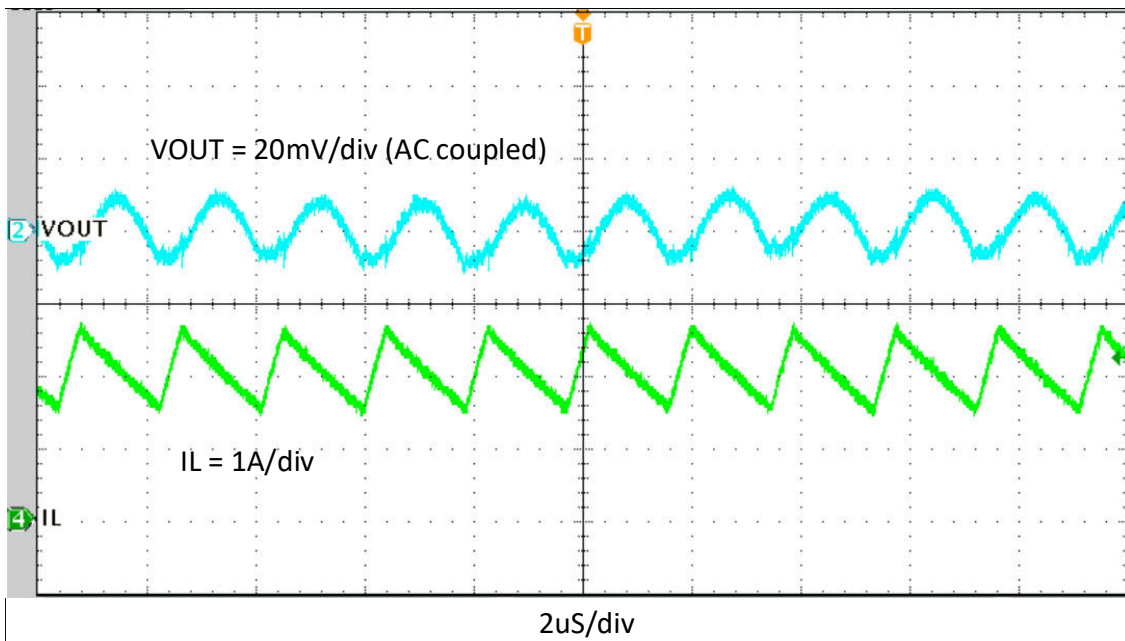**Figure 4-4. TPS62933EVM Output Voltage Ripple, I_{OUT} = 3 A**

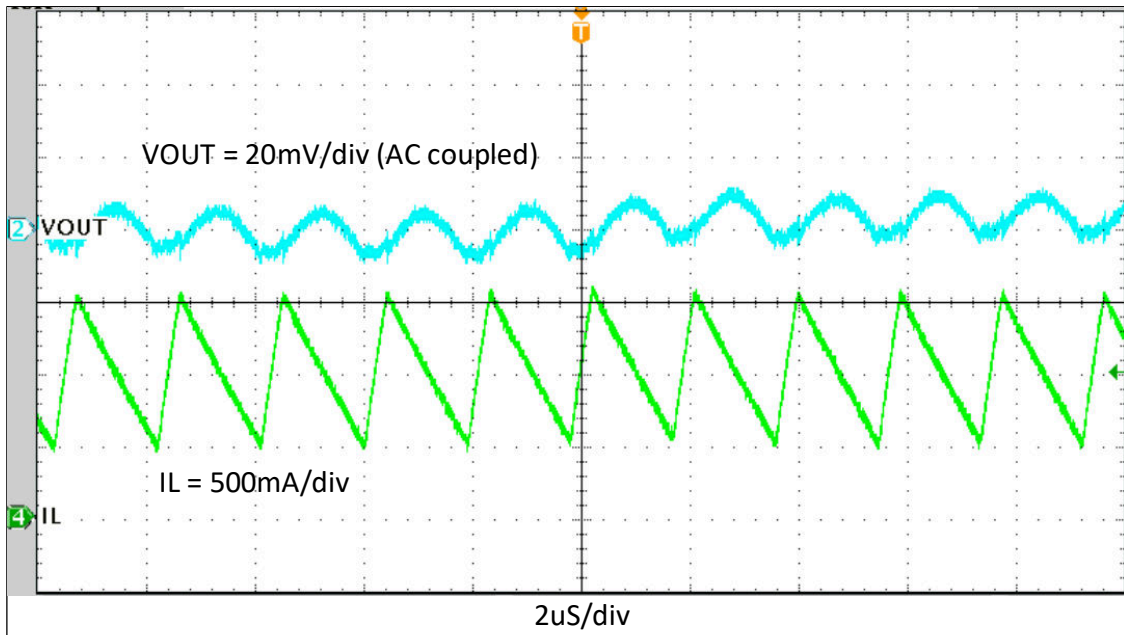**Figure 4-5. TPS62933EVM Output Voltage Ripple, I_{OUT} = 2 A**
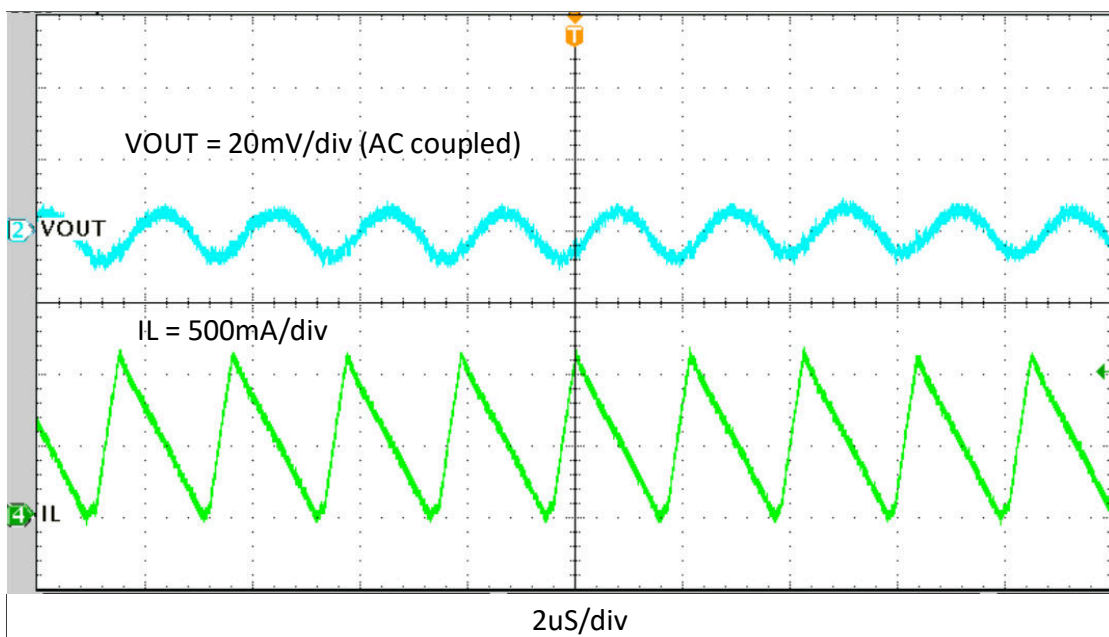
Figure 4-6. TPS62933EVM Output Voltage Ripple, I_{OUT} = 1 A

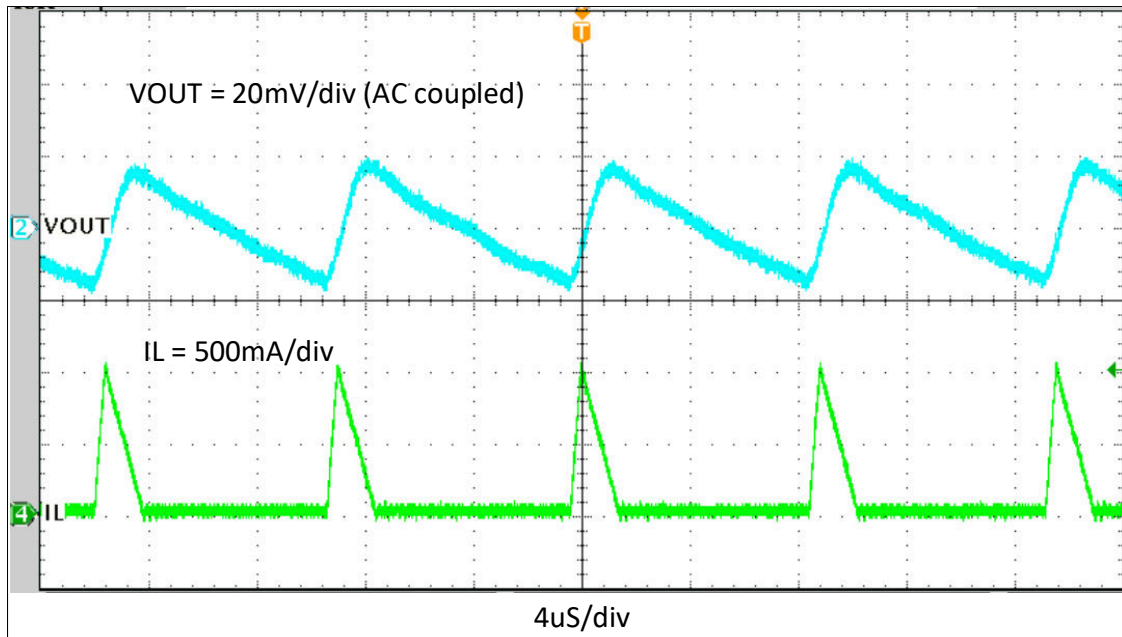**Figure 4-7. TPS62933EVM Output Voltage Ripple, I_{OUT} = 500 mA**

Figure 4-8. TPS62933EVM Output Voltage Ripple, I_{OUT} = 100 mA

Figure 4-9. TPS62933EVM Output Voltage Ripple, I_{OUT} = 0 A

4.5 Start-Up

The TPS62933EVM start-up waveform with 20MHz scope bandwidth relative to V_{IN} is shown in Figure 4-10. Load = 3-A.
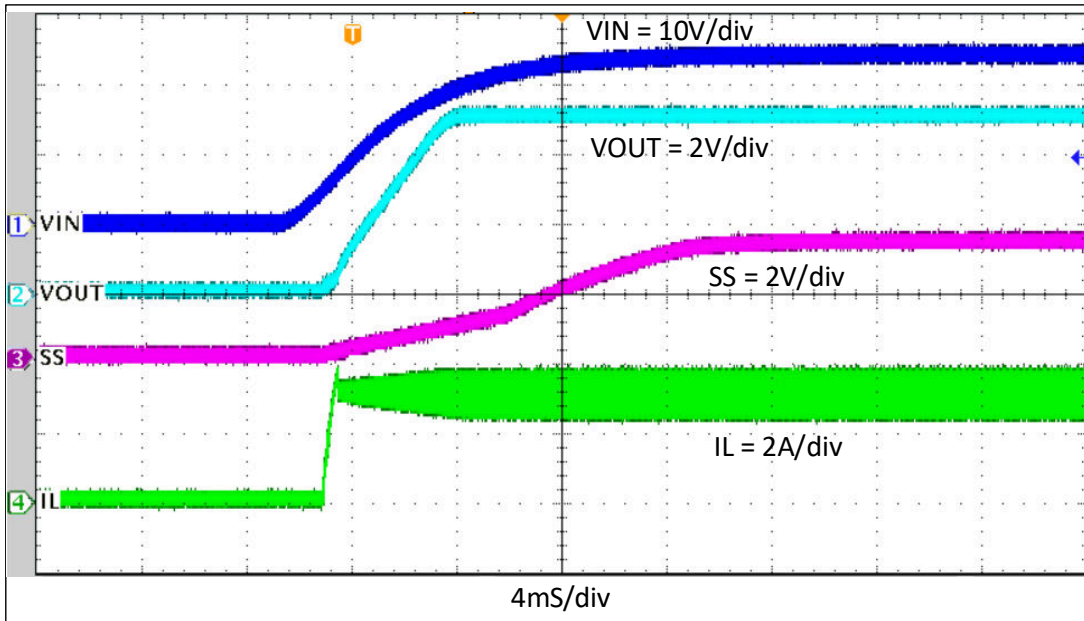

Figure 4-10. TPS62933EVM Start-Up Relative to V_{IN}

4.6 Shut-Down

The TPS62933EVM shut-down waveform with 20MHz scope bandwidth relative to V_{IN} is shown in Figure 4-11. Load = 3-A.
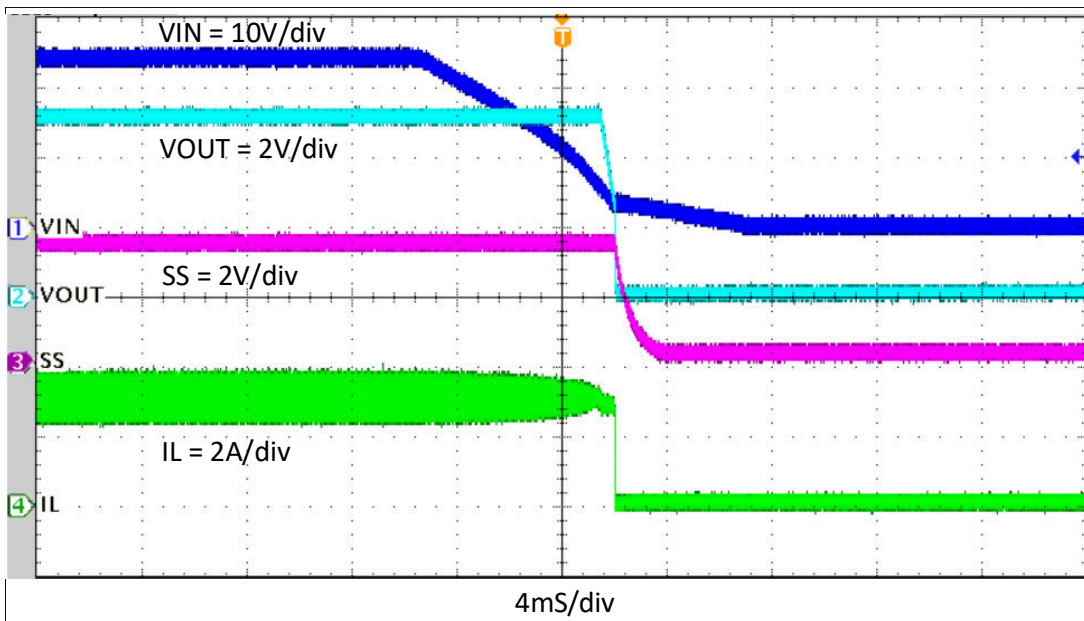

Figure 4-11. TPS62933EVM Shut-Down Relative to V_{IN}

5 Board Layout

This section provides a description of the TPS62933EVM, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS62933EVM is shown in Figure 5-1, Figure 5-2, and Figure 5-3. The top layer contains the main power traces for VIN, VOUT, and ground. Also on the top layer are connections for the pins of the TPS62933 and a large area filled with ground. Most of the signal traces are also located on the top side. The input decoupling capacitors, C6, C7, C8, and C9 are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. The bottom layer is a ground plane along with the switching node copper fill, signal ground copper fill and the feed back trace from the point of regulation to the top of the resistor divider network. Both the top layer and bottom layer use 2 oz copper thickness.

Figure 5-4 and Figure 5-5 are the TPS62933EVM board top view and bottom view, respectively.
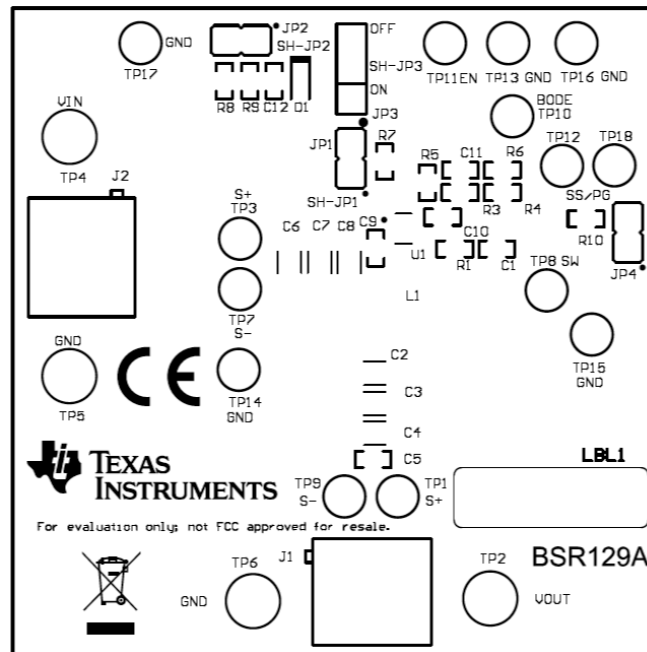

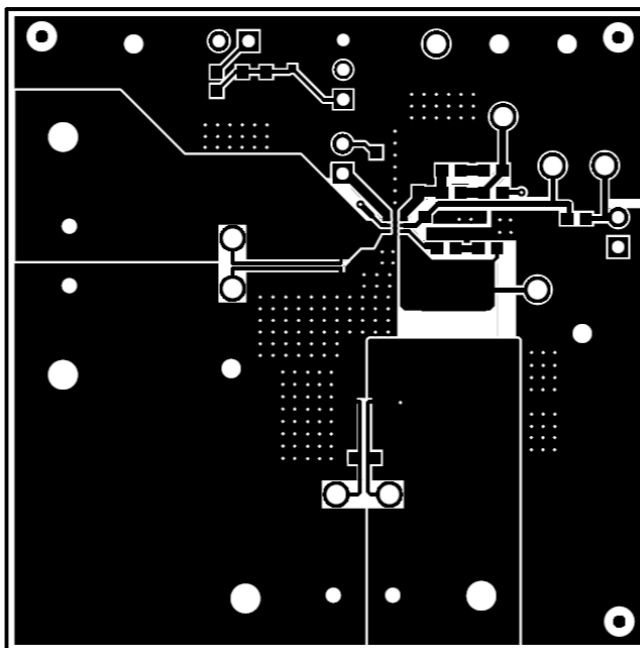**Figure 5-1. TPS62933EVM Top Assembly**

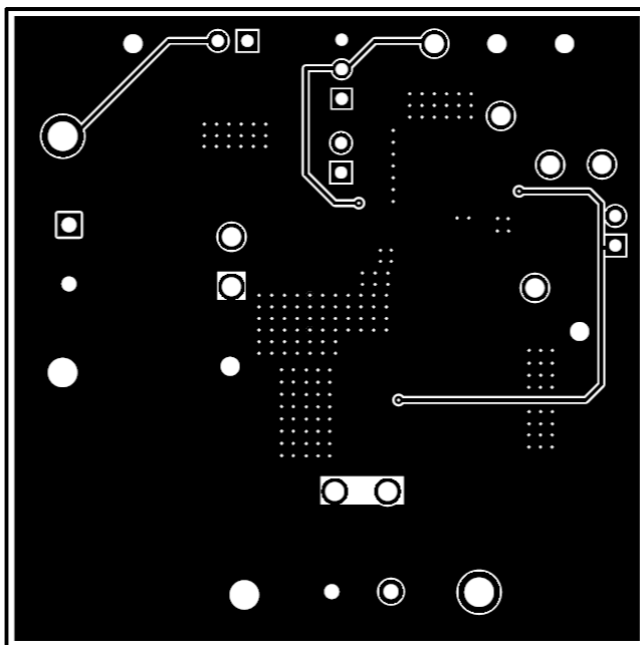**Figure 5-2. TPS62933EVM Top Layer**
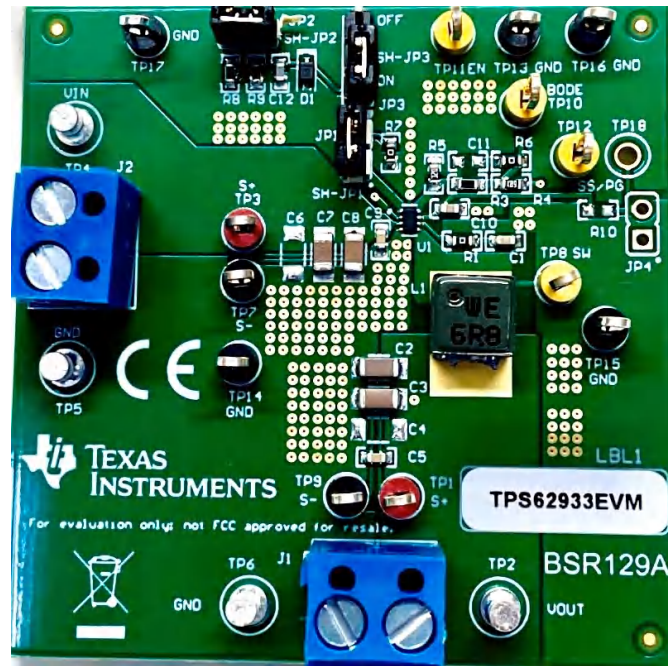

Figure 5-3. TPS62933EVM Bottom Layer

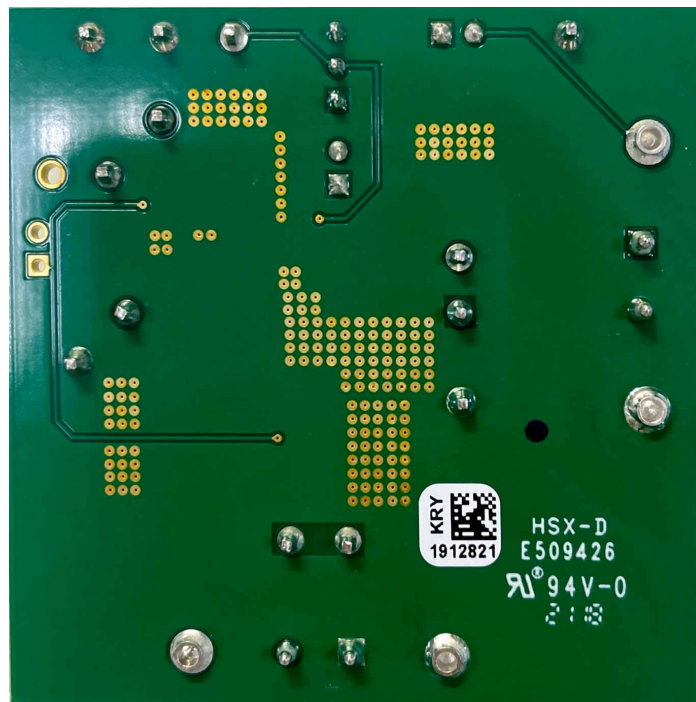**Figure 5-4. TPS62933EVM Board Top View**

Figure 5-5. TPS62933EVM Board Bottom View

6 Schematic, List of Materials, and Reference
6.1 Schematic

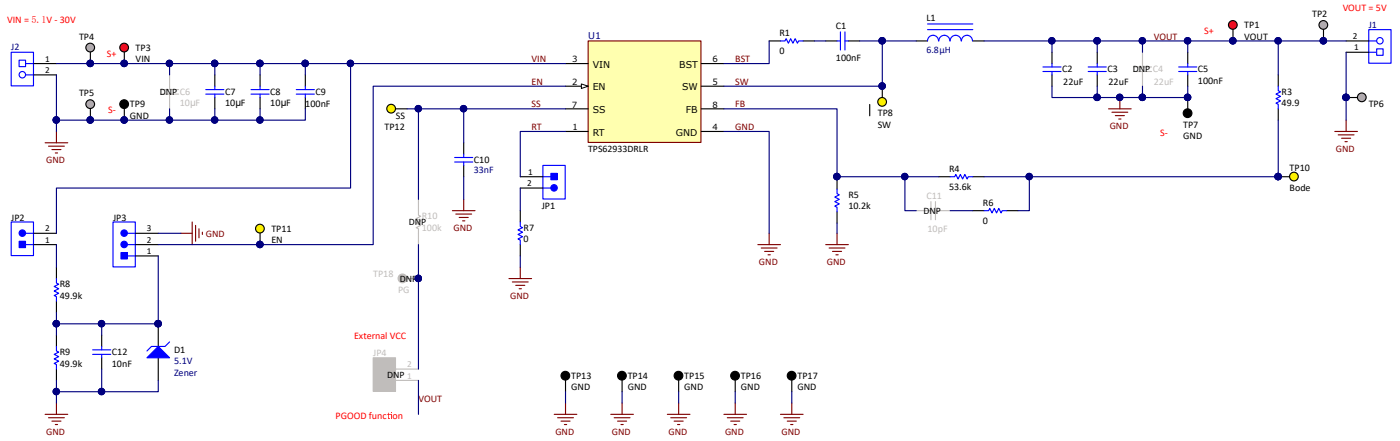Figure 6-1 is the schematic for the TPS62933EVM.

Figure 6-1. TPS62933EVM Schematic Diagram

6.2 List of Materials

Table 6-1. List of Materials

DESCRIPTION	DES	PART NUMBER	QTY	MANUFACTURER
Printed Circuit Board	!PCB1	BSR129	1	Any
CAP, CERM, 0.1 µF, 50 V,+/- 10%, X7R, 0603	C1, C5, C9	C0603C104K5RACAUTO	3	Kemet
CAP, CERM, 22 uF, 35 V, +/- 20%, X5R, 1206	C2, C3	C3216X5R1V226M160AC	2	TDK
CAP, CERM, 10 µF, 50 V,+/- 10%, X7R, 1206	C7, C8	CGA5L1X7R1H106K160AC	2	TDK
CAP, CERM, 6800 pF, 50 V, +/- 10%, X7R, 0603	C10	GRM188R71H682KA01D	1	MuRata
CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603	C12	C0603C103J5RACTU	1	Kemet
Diode, Zener, 5.1 V, 200 mW, SOD-323	D1	MMSZ5231BS-7-F	1	Diodes Inc.
Terminal Block, 5.08 mm, 2x1, Brass, TH	J1, J2	ED120/2DS	2	On-Shore Technology
Header, 100mil, 2x1, Gold, TH	JP1, JP2, JP4	PBC02SAAN	3	Sullins Connector Solutions
Header, 100mil, 3x1, Tin, TH	JP3	PEC03SAAN	1	Sullins Connector Solutions
Inductor, Shielded, Hyperflux, 6.8 µH, 6.5 A, 0.01936 ohm, SMD	L1	74439346068	1	Wurth Elektronik
Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	LBL1	THT-14-423-10	1	Brady
RES, 0, 5%, 0.1 W, 0603	R1, R6, R7	RC0603JR-070RL	3	Yageo
RES, 49.9, 1%, 0.1 W, 0603	R3	RC0603FR-0749R9L	1	Yageo
RES, 53.6 k, 1%, 0.1 W, 0603	R4	RC0603FR-0753K6L	1	Yageo
RES, 10.2 k, 1%, 0.1 W, 0603	R5	RC0603FR-0710K2L	1	Yageo
RES, 49.9 k, 1%, 0.1 W, 0603	R8, R9	RC0603FR-0749K9L	2	Yageo
RES, 100 k, 1%, 0.1 W, 0603	R10	RC0603FR-07100KL	1	Yageo
Shunt, 100mil, Gold plated, Black	SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5	SNT-100-BK-G	5	Samtec
Test Point, Multipurpose, Red, TH	TP1, TP3	5010	2	Keystone
Terminal, Turret, TH, Double	TP2, TP4, TP5, TP6	1502-2	4	Keystone
Test Point, Multipurpose, Black, TH	TP7, TP9, TP13, TP14, TP15, TP16, TP17	5011	7	Keystone
Test Point, Multipurpose, Yellow, TH	TP8, TP10, TP11, TP12, TP18	5014	5	Keystone
3.8-V to 30-V Input, 3-A/2-A, 300kHz-2.2MHz, Low IQ Synchronous Buck Converter in SOT583 Package	U1	TPS62933DRLR	1	Texas Instruments
CAP, CERM, 22 uF, 35 V, +/- 20%, X5R, 1206	C4	C3216X5R1V226M160AC	0	TDK
CAP, CERM, 10 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 1206	C6	CGA5L1X7R1H106K160AC	0	TDK
CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0603	C11	C0603C100J5GACTU	0	Kemet

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