User's Guide

TPSM843A26EVM Step-Down Module Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPSM843A26EVM evaluation module (BSR228) and the TPSM843A26 buck power module. This user's guide also includes the performance characteristics, schematic, and bill of materials for the TPSM843A26EVM.

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Trademarks

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1 Introduction

1.1 Background

The TPSM843A26 module is a synchronous buck power module designed to provide up to a 16-A output. The input (VIN) is rated for 4 V to 18 V. Table 1-1 provides the rated input voltage and output current range for the evaluation module.

The high-side and low-side MOSFETs are incorporated inside the TPSM843A26 package along with the gate-drive circuitry, inductor and basic passives. The low drain-to-source on-resistance of the MOSFET allows the TPSM843A26 to achieve high efficiencies and helps keep the junction temperature low at the rated output current. Fixed frequency advanced current mode control allows you to synchronize the module to an external clock source. An external divider allows for an adjustable output voltage. The TPSM843A26 FSEL and MSEL pins provide selectable switching frequency, soft-start time, current limit, and internal compensation. Lastly, the TPSM843A26 includes an enable pin and a power-good output, which can be used for sequencing multiple modules.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPSM843A26EVM	V_{IN} = 4 V to 18 V	0 A to 16 A

1.2 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPSM843A26EVM. Observe all safety precautions.

Caution

The TPSM843A26EVM may become hot during operation due to dissipation of power in some operating conditions. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

Caution Hot surface.

Contact may cause burns.

Do not touch!

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than one power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

1.3 Performance Characteristics Summary

A summary of the TPSM843A26EVM performance characteristics is provided in Table 1-2. The TPSM843A26EVM is designed and tested for V_{IN} = 4 V to 18 V. Characteristics are given for an input voltage of V_{IN} = 12 V and an output voltage of 1 V, unless otherwise specified. The ambient temperature is room temperature (25°C) for all measurements, unless otherwise noted.

Table 1-2. TPSM843A26EVM Performance Characteristics Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} voltage range		11.7	12	12.3	V
Input current	V_{IN} = 12 V, I_O = 0 A		33		mA
	V_{IN} = 5 V, I_O = 16 A		3.85		A
Output voltage setpoint			1.0		V
Output current range	V_{IN} = 11.7 V to 12.3 V	0		16	A
Line and load regulation	V_{IN} = 4 V to 13.2 , I_O = 0 A to 16 A		±1%		
Phase Margin	I_O =16 A		44		degrees
Input ripple voltage	I_O = 16 A		68		mVPP
Output rise time	Set by MSEL pin resistor, J5 short pins 3 and 4, 5 and 6, or 9 and 10		2		ms
Current limit	Set by MSEL pin resistor, J5 short pins 1 and 2, 3 and 4, 5 and 6, or 7 and 8		High		
Switching frequency (f_{SW})	Set by FSEL pin resistor, J4 short pins 9 and 10		1000		kHz
Peak efficiency	V_{IN} = 5 V, I_O = 3.75 A		91.4%		
	V_{IN} = 12 V, I_O = 5.75 A		86.9%		
IC case temperature	V_{IN} = 12 V, I_O = 16 A, 10-minute soak		101		°C

2 Configurations and Modifications

This evaluation module is designed to provide access to the features of the TPSM843A26. There are jumpers provided for testing different configurations. Jumper selections must be made prior to enabling the TPSM843A26.

If a desired configuration is not available, some modifications can be made to this module. When modifications are made to the components on the EVM, the internal compensation option selected with the MODE pin resistor can need to be changed. Changes to the f_{SW}, output voltage, and output capacitors can require a change in the compensation. TPSM843A26 data sheet equations or WEBENCH can be used to calculate the output capacitor value, compensation, and f_{SW}. Ensure all components have sufficient voltage and current ratings.

2.1 Output Voltage

There are a few ways to set the output voltage. First, jumper J6 can be used to select between the options shown in Table 2-1 for output voltages greater than 1.0 V. If the desired output voltage is not available, a resistor must be changed. For output voltages less than 1.0 V, TI recommends shorting pins 1 and 2 and decreasing R14. The desired value for R14 can be calculated with Equation 2, where R_{FBB} is R16 which is 10 kΩ.

$$V_{OUT} = V_{REF} \times \left[\frac{R_{FBB} + R_{14}}{R_{FBB}}\right] \quad (1)$$

$$R_{14} = R_{FBB} \times \left[\frac{V_{OUT} - V_{REF}}{V_{REF}}\right] \quad (2)$$

Table 2-1. VOUT Selection

JUMPER J6 SETTING	SELECTED BOTTOM FB RESISTOR (R_{FBB})	NOMINAL OUTPUT VOLTAGE
1 to 2 pin shorted(1)	10 kΩ	1.0 V
3 to 4 pin shorted	7.15 kΩ	1.2V
5 to 6 pin shorted	3.9 kΩ	1.80 V
7 to 8 pin shorted	1.78 kΩ	3.3 V
9 to 10 pin shorted	1.10 kΩ	5.0 V
11 to 12 pin shorted	768 Ω	7.0 V

(1) Default Setting

2.2 Switching Frequency (FSEL Pin)

Jumper J3 can be used to set the switching frequency mode of the device. Shorting pins 1 and 2 allows the user to synchronize the switching frequency with an external clock. Shorting pins 3 and 4 sets the frequency through a resistor to ground. Jumper J4 can be used to select between the switching frequency options shown in Table 2-2. If the desired option is not available, change one of the resistors to the value which sets the desired option.

Table 2-2. FSEL Selection

JUMPER J4 SETTING	FSEL RESISTOR	SWITCHING FREQUENCY
1 to 2 pin shorted	24.3 kΩ	500 kHz
3 to 4 pin shorted	17.4 kΩ	750 kHz
5 to 6 pin shorted(1)	11.8 kΩ	1000 kHz
7 to 8 pin shorted	8.06 kΩ	1500 kHz
9 to 10 pin shorted	4.99 kΩ	2200 kHz

(1) Default Setting

2.3 Current Limit, Soft-Start Time, and Internal Compensation (MSEL Pin)

Jumper J5 can be used to select between the current limit, soft-start time, and internal compensation options shown in Table 2-3. If the desired option is not available, change one of the resistors to the value which sets the desired option.

Table 2-3. MODE Selection

JUMPER J5 SETTING	MODE RESISTOR	CURRENT LIMIT	SOFT-START TIME	RAMP
1 to 2 pin shorted	1.78 kΩ	High	1 ms	1 pF
3 to 4 pin shorted(1)	4.87 kΩ	High	2 ms	2 pF
5 to 6 pin shorted	11.3 kΩ	High	2 ms	4 pF
7 to 8 pin shorted	14.3 kΩ	High	4 ms	4 pF
9 to 10 pin shorted	60.4 kΩ	Low	2 ms	2 pF

(1) Default Setting

2.4 Enable, UVLO (EN Pin)

Jumper J2 can be used to switch the device on by shorting pins 1 and 2 or off by shorting pins 2 and 3. Depending on VIN, R1 and R2 can be adjusted externally for the desired enable voltage, typically 1.2 V.

3 Test Setup and Results

This section describes how to properly connect, set up, and use the TPSM843A26EVM evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, input ripple, start-up, and current limit modes. Measurements are taken with the following conditions unless otherwise noted.

- 12-V input
- Room temperature (20°C to 25°C)
- U1 with the default setting output voltage of 1 V, switching frequency of 1000 kHz, and maximum current limit setting

3.1 Input and Output Connections

The TPSM843A26EVM is provided with input connectors, output connectors, and test points as shown in Table 3-1 and Table 3-2.

To support the minimum input voltage with the full rated load on both outputs with the default EVM, a power supply capable of supplying greater than 16 A must be connected to J1 through a pair of 18-AWG wires or better.

The load must be connected to J8. Two pair of 18-AWG wires or better must be used for each connection. With the maximum current limit setting, the maximum load current capability is near 16 A before the TPSM843A26 goes into current limit. Wire lengths must be minimized to reduce losses in the wires.

Test point TP1 (VIN S+) provides a place to monitor the V_{IN} input voltage with TP2 (VIN S-) providing a convenient ground reference for U1. TP10 (VOUT S+) is used to monitor the output voltage of U1 with TP11 (VOUT S-) as the ground reference.

If modifications are made to the TPSM843A26EVM, the input current can change. The input power supply and wires connecting the EVM to the power supply must be rated for the input current.

Table 3-1. Connectors and Jumpers

REFERENCE DESIGNATOR	NAME	FUNCTION
J1	VIN	VIN screw terminal to connect input voltage (see Table 1-1 for V_{IN} range)
J2	EN Select	3-pin header to connect to enable pin and allow for selection between ON and OFF. Populate R1 and R2 for desired EN voltage.
J3	FSEL/SYNC	Select between internal frequency set through resistor or external clock
J4	FSEL Select	FSEL selection header. Use shunt to select FSEL resistor. See Table 2-2.
J5	MSEL Select	MSEL selection header. Use shunt to set current limit, soft-start time, ramp time. See Table 2-3.
J6	VOUT Select	VOUT selection header. Use shunt to set output voltage. See Table 2-1.
J7	VOUT	VOUT test point, coaxial cable
J8	VOUT	VOUT screw terminal to connect load to output

Table 3-2. Test Points

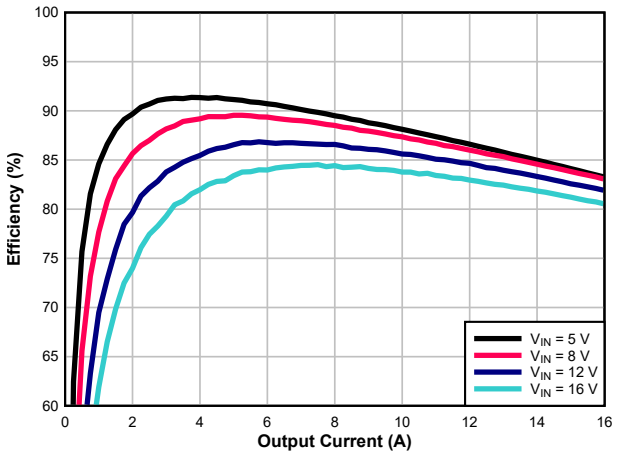
REFERENCE DESIGNATOR	NAME	FUNCTION
TP1	VIN S+	VIN test point. Use this for efficiency and VIN measurement.
TP2	VIN S-	PGND test point. Use this for efficiency and VIN measurement.
TP3	EN	EN test point. If applying an external voltage, keep the voltage below the absolute maximum voltage of the EN pin of 6 V.
TP4	SYNC	External clock test point
TP5	MSEL	MSEL test point
TP6	BODE+	Test point for Bode plot measurements.
TP7	BODE-	Test point for Bode plot measurements.
TP8	PGOOD	PG test point
TP9	SW	SW test point
TP10	VOUT S+	VOUT test point. Use this for efficiency, output regulation and VOUT measurement.
TP11	VOUT S-	PGND test point. Use this for efficiency, output regulation and VOUT measurement.
TP12	PGND	PGND test point
TP13	PGND	PGND test point
TP14	PGND	PGND test point

3.2 Efficiency

Figure 3-1 through Figure 3-5 shows the efficiency for the TPSM843A26EVM. Using the selection jumpers for U1, the results for different output voltage and switching frequency combinations are included. The test points listed in Table 3-3 are used for the efficiency measurement. Use these test points to minimize the contribution of PCB parasitic power loss to the measured power loss.

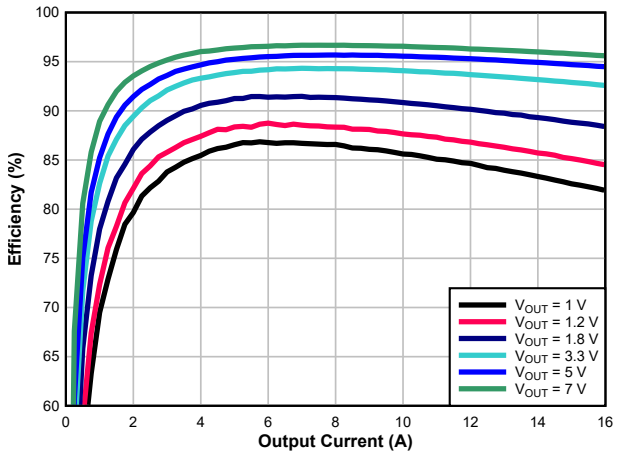
Table 3-3. Efficiency Measurement Test Points

TEST POINT NAME	REFERENCE DESIGNATOR	FUNCTION
VIN S+	TP1	Input voltage test point connected near J1
VIN S-	TP2	PGND reference test point for input voltages Kelvin connected
VOUT S+	TP10	Output voltage test point connected near J8
VOUT S-	TP11	PGND reference test point for output voltages Kelvin connected



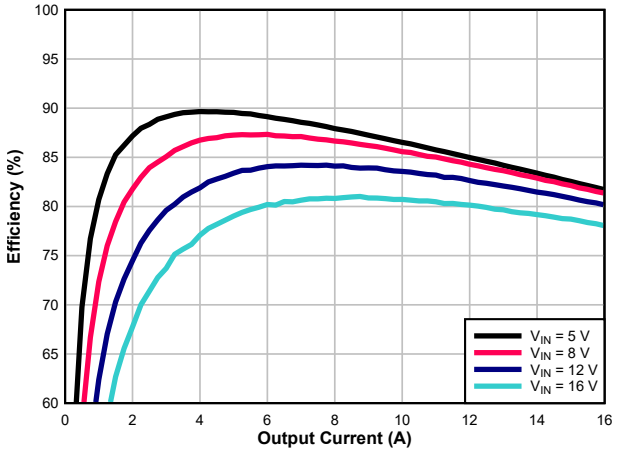
V_{OUT} = 1 V f_{SW} = 1000 kHz

Figure 3-1. Efficiency – Default Configuration



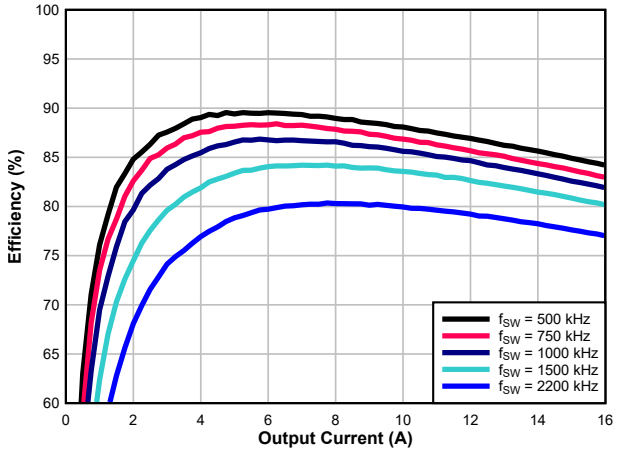
V_{IN} = 12 V f_{SW} = 1000 kHz

Figure 3-2. Efficiency – 1000-kHz Switching Frequency with Different Output Voltages



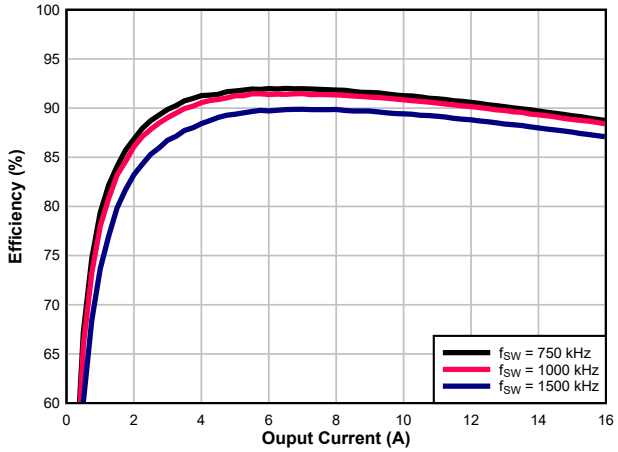
V_{OUT} = 1 V f_{SW} = 1500 kHz

Figure 3-3. Efficiency – 1500-kHz Switching Frequency with Different Input Voltages



V_{IN} = 12 V V_{OUT} = 1 V

Figure 3-4. Efficiency – 1-V Output with Different Switching Frequencies



V_{IN} = 12 V V_{OUT} = 1.8 V

Figure 3-5. Efficiency – 1.8-V Output with Different Switching Frequencies

3.3 Output Voltage Regulation

Figure 3-6 and Figure 3-7 show the load and line regulation for TPSM843A26EVM.

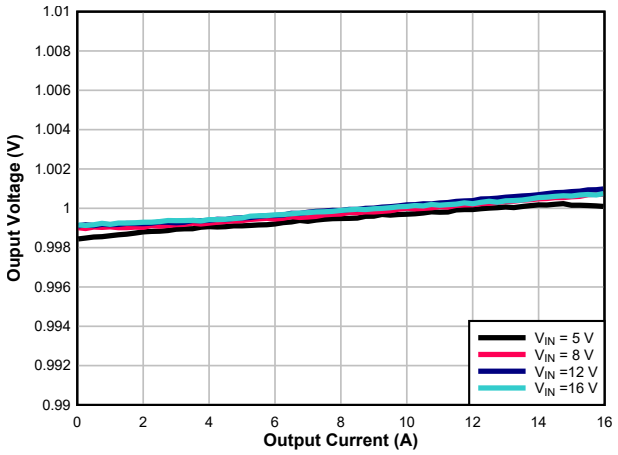


Figure 3-6. U1 Load Regulation

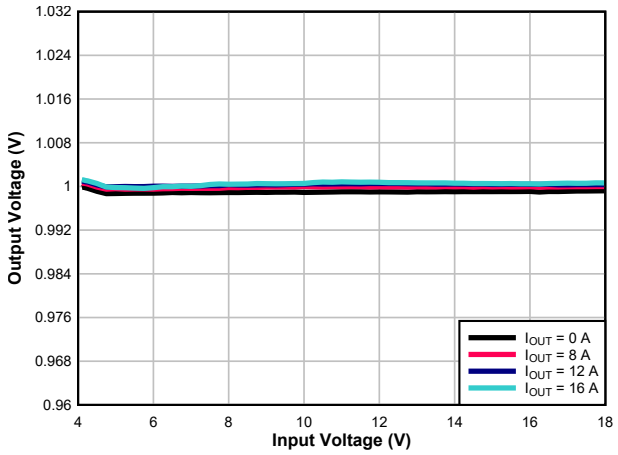


Figure 3-7. U1 Line Regulation

3.4 Load Transient and Loop Response

Figure 3-8 shows the load transient response. The current step is from 0 A to 10 A and the current step slew rate is 0.6 A/us. An electronic load is used to provide the step. The VOUT voltage is measured using J7 SMB connector.

Figure 3-9 shows the loop characteristic. Gain and phase plots are shown for V_{IN} voltage of 12-V and 12-A and 16-A load.

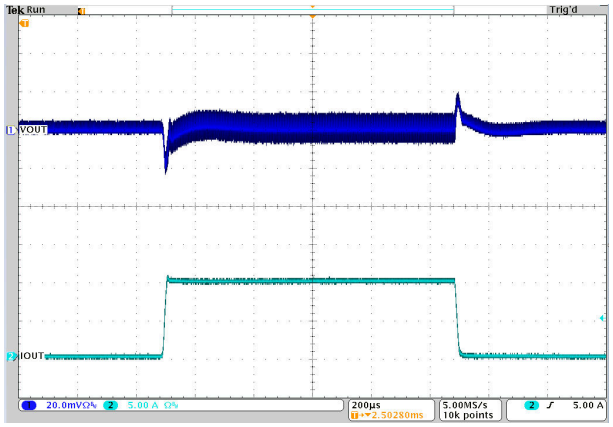


Figure 3-8. U1 Transient Response

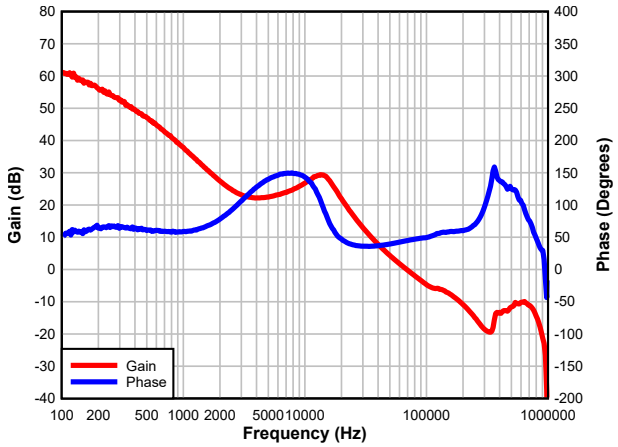


Figure 3-9. U1 Bode Plot – 12-A Load

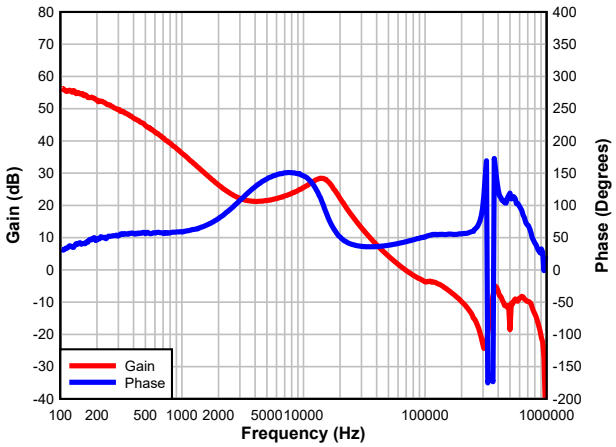


Figure 3-10. U1 Bode Plot – 16-A Load

Figure 3-11 and Figure 3-12 shows the loop characteristics for U1 with the three different ramp settings.

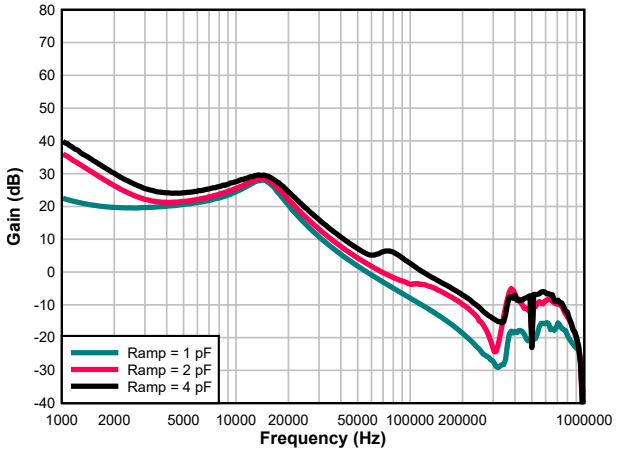


Figure 3-11. U1 Loop Gain with Different Ramp Settings

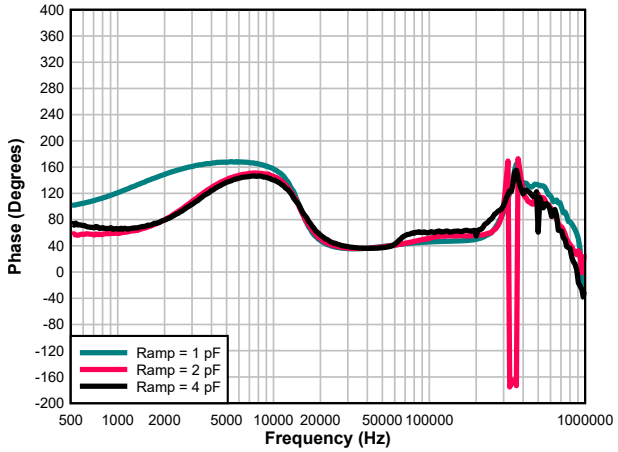


Figure 3-12. U1 Loop Phase with Different Ramp Settings

3.5 Input Voltage Ripple

Figure 3-13 through Figure 3-14 show the TPSM843A26EVM input voltage ripple with no load and 16-A load at V_{IN} = 12 V. The ripple voltage is measured across C12 for U1.

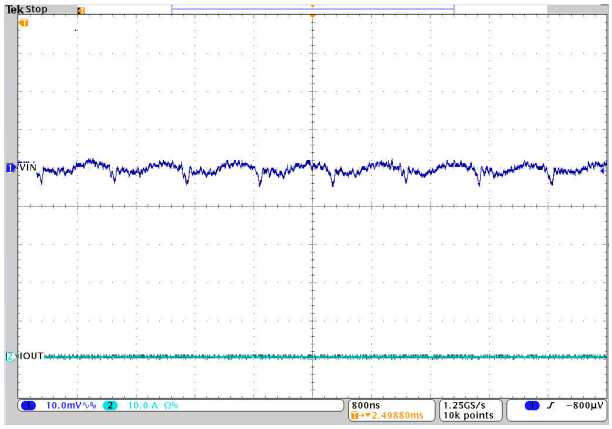


Figure 3-13. U1 Input Ripple – No Load

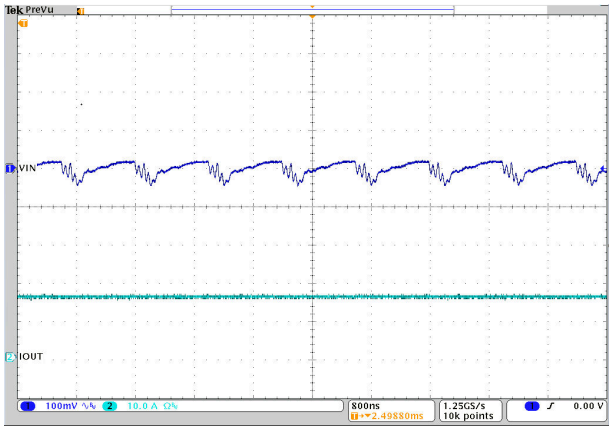


Figure 3-14. U1 Input Ripple – 16-A Load

3.6 Start-up and Shutdown with EN

Figure 3-15 and Figure 3-16 show the start-up and shutdown waveforms with EN. In Figure 3-15, the input voltage is initially applied and the output is inhibited by pulling EN to GND. When the EN voltage is increased above the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value.

Figure 3-17 shows EN start-up with a 8-A load. Figure 3-18 shows the BP5 internal LDO start-up relative to the EN pin.

A shunt on the EN jumper J2 can be used to test the EN start-up of U1. When the shunt is removed from EN jumper J2 or place on pin 1 and 2 of EN jumper J2, EN is released and the start-up sequence begins for U1.

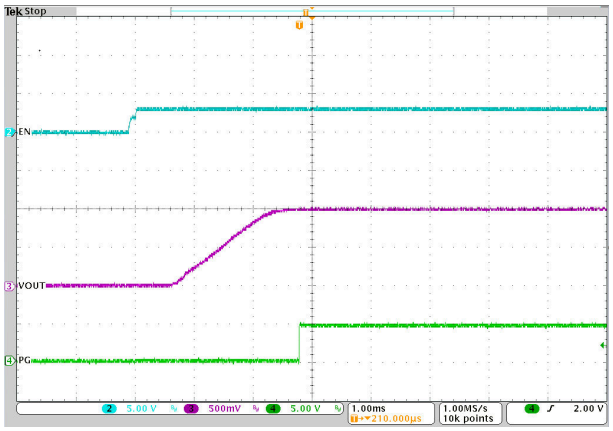


Figure 3-15. U1 Start-up with EN – No Load

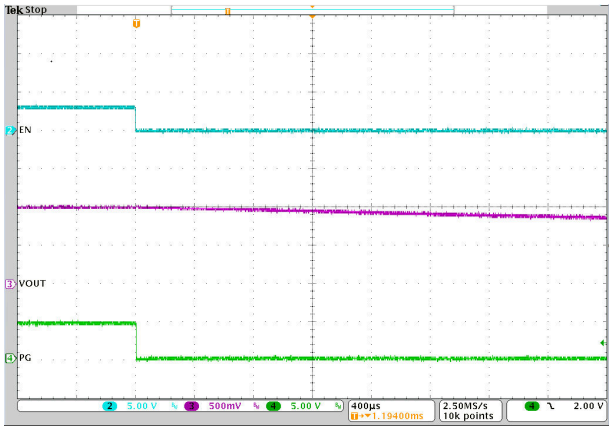


Figure 3-16. U1 Shutdown with EN – No Load

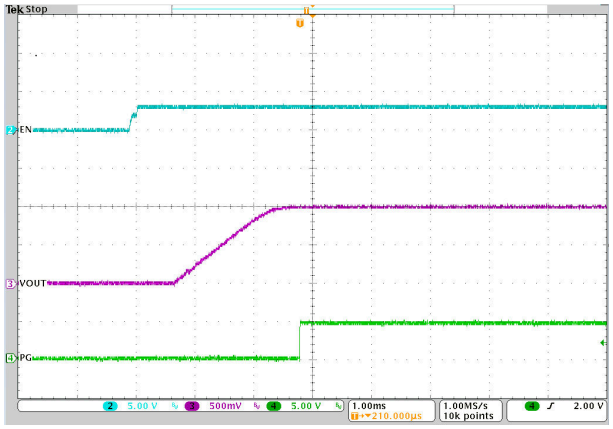


Figure 3-17. U1 Start-up with EN – 8-A

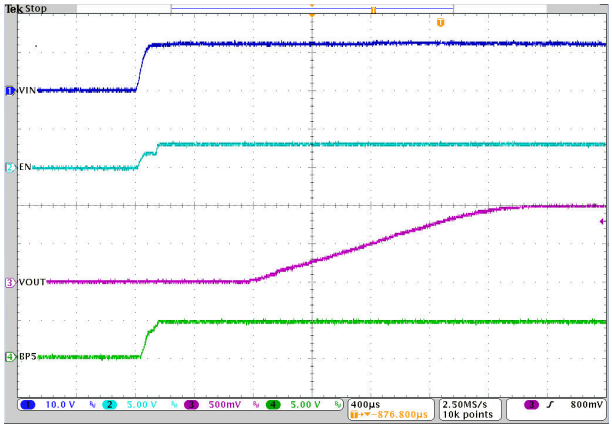


Figure 3-18. U1 Startup with EN – No Load and Measuring BP5

3.7 Start-up and Shutdown with VIN

Figure 3-19 and Figure 3-20 show the start-up and shutdown waveforms for U1 with VIN. In Figure 3-19, the VIN voltage ramps up and output voltage ramps up after the input and EN pin voltages reach their respective threshold. In Figure 3-20, the VIN voltage ramps down and the TPSM843A26 shuts down when the input or EN pin voltage reach their respective threshold. The rate at which VIN ramps down changes as soon as the TPSM843A26 is disabled because it is no longer loading the input supply.

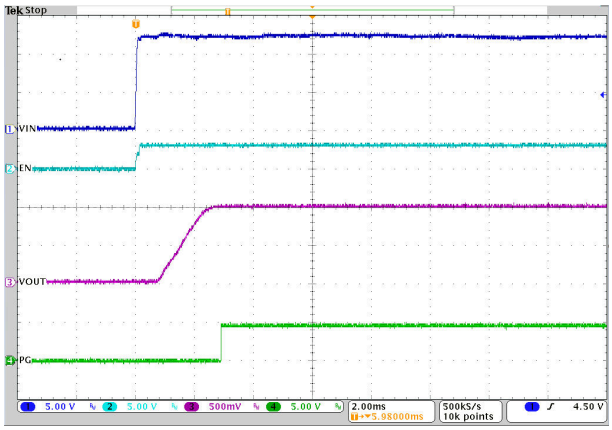


Figure 3-19. U1 Start-up with VIN – No Load

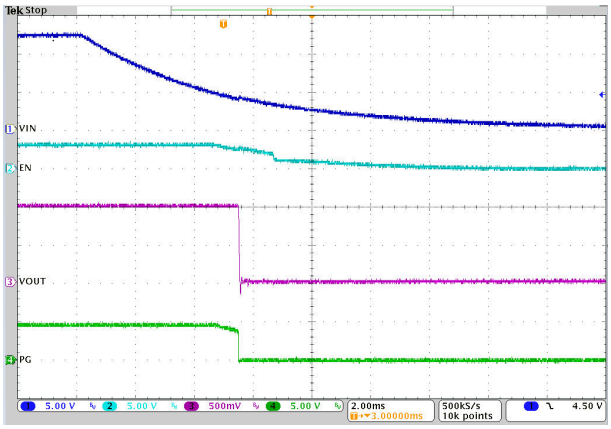


Figure 3-20. U1 Shutdown with VIN – 8-A Load

3.8 Start-up Into Pre-Bias

Figure 3-21 shows the EN start-up of U1 into a pre-biased output. The output voltage is pre-biased by toggling the EN pin low then high at a rate such that the output voltage does not fully discharge before EN goes high again.

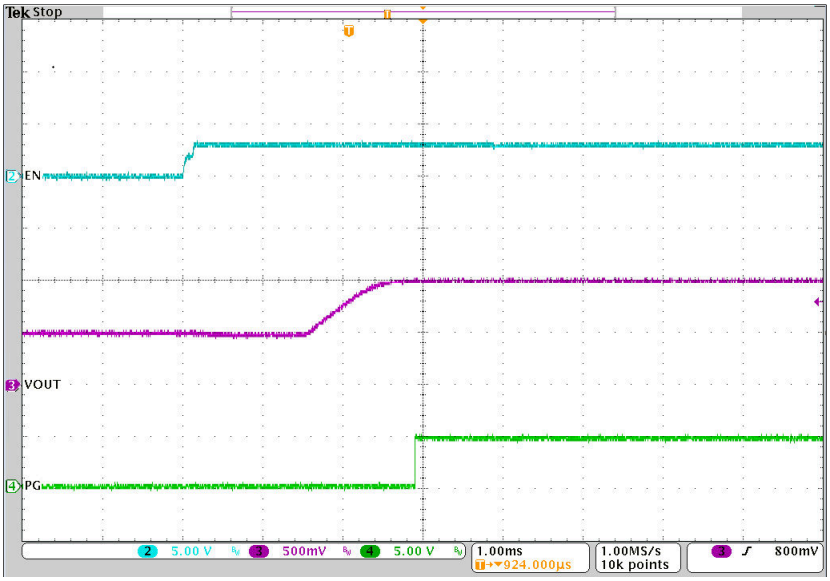


Figure 3-21. U1 Start-up Into 0.5-V Pre-Bias

3.9 Thermal Performance

Figure 3-22 and Figure 3-23 show the temperature rise of the TPSM843A26 at 12-A and 16-A load. A minimum of a 10 minute soak time was used before taking the measurement.

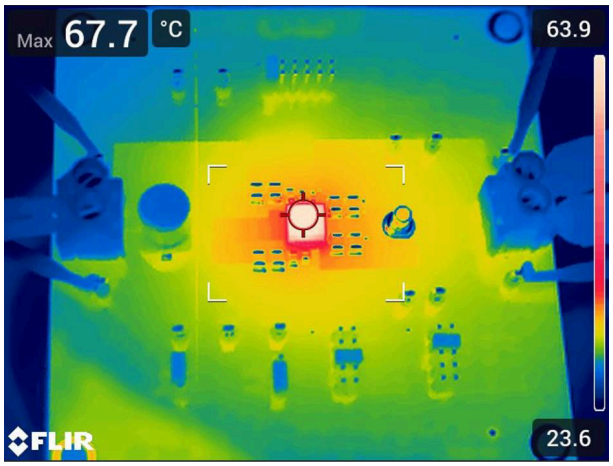


Figure 3-22. U1 Thermal Performance – 12-A Load

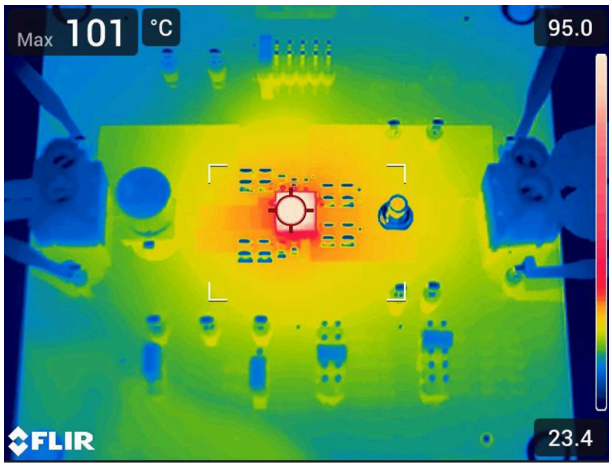


Figure 3-23. U1 Thermal Performance – 16-A Load

4 Board Layout

This section provides a description of the TPSM843A26EVM board layout and layer illustrations.

4.1 Layout

The board layout for the TPSM843A26EVM is shown in Figure 4-1 through Figure 4-8. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper. The U1 circuit takes up an area of only approximately 605 mm^2 as shown on the silkscreen.

All of the required components for the TPSM843A26 are placed on the top layer for U1. The input and output capacitors are placed on the top layer in a symmetrical pattern. Additionally, the voltage set point is interchangable with J6 on the top layer. The top resistor is connected close to the module on the top layer, the interchangable bottom resistors are located on the bottom later. Additional three input bulk capacitors are used near the input terminal to limit the noise entering the module from the supply used to power the board. Critical analog circuits such as the EN resistors, MSEL resistors, and SYNC/FSEL resistors are kept close to the IC and terminated to the quiet analog ground (AGND).

The top layer contains the main power traces for VIN, VOUT and a short trace to measure SW. The top layer power traces are connected to the planes on other layers of the board with multiple vias placed around the board. There are multiple vias near the PGND pins of the module to help maximize the thermal performance. The TPSM843A26 circuit has its own dedicated ground for quiet analog ground that is connected to the main power ground plane at a single point. This single point connection is done on the internal ground planes on signal layer 1.

The mid layers 1 to 4 are mostly power ground planes with some traces. Some layers contain VIN copper area beneath the IC to connect VIN pins together with a low impedance connection.

The bottom layer is mostly a ground plane. This layer has additional VOUT copper area for the U1 circuit. In addition, this layer also contains the interchangable resistors for SYNC/FSEL, MSEL and EN pins along with more space to add extra output capacitors. EN resistors were left unpopulated to allow the user to add accordingly to desired startup. In addition, BP5 resistor, Feedforward capacitor and resitor, 50-ohm resistor for bode measurements and 50-ohm resistor for VOUT SMB connection can be found on this layer.

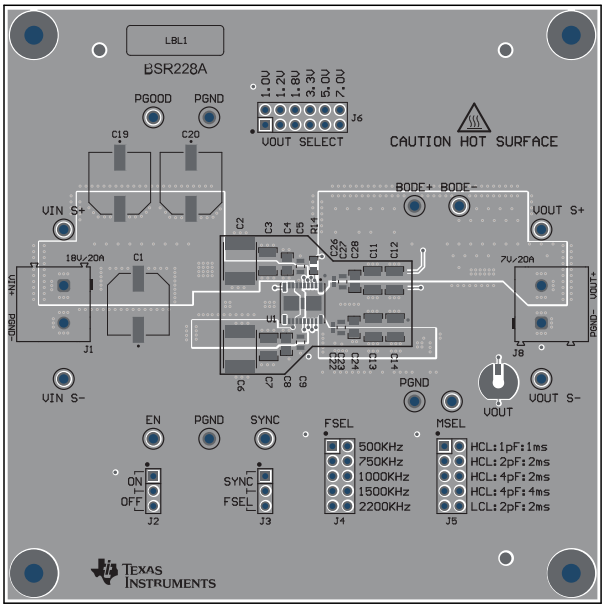


Figure 4-1. Top-Side Composite View

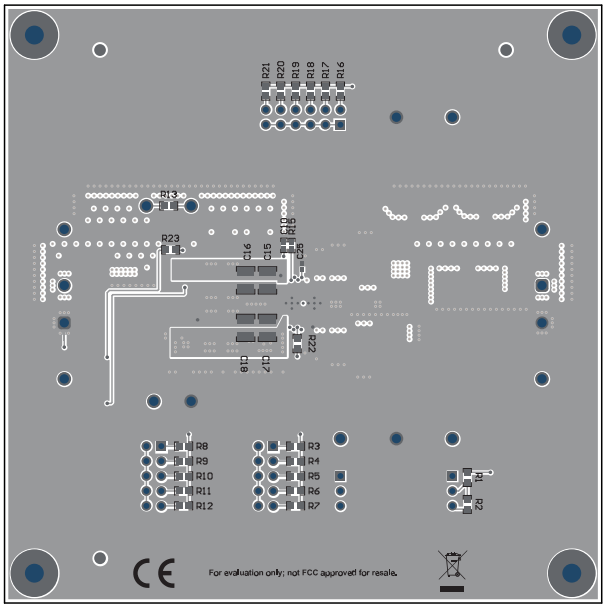


Figure 4-2. Bottom-Side Composite View (Viewed From Bottom)

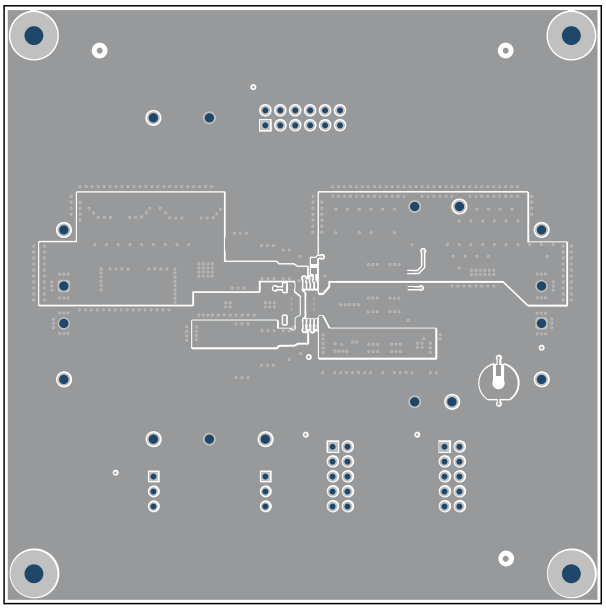


Figure 4-3. Top Layer Layout

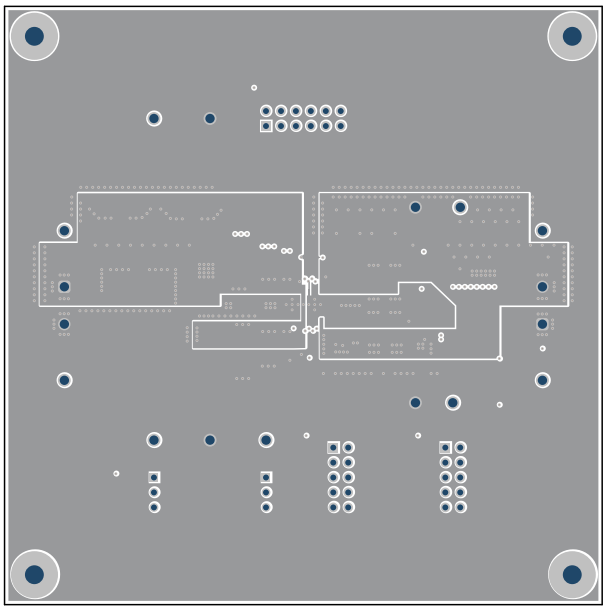


Figure 4-4. Mid Layer 1 Layout

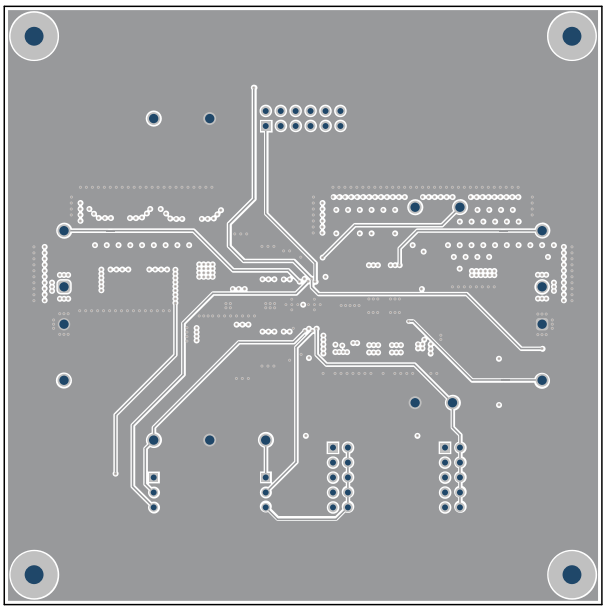


Figure 4-5. Mid Layer 2 Layout

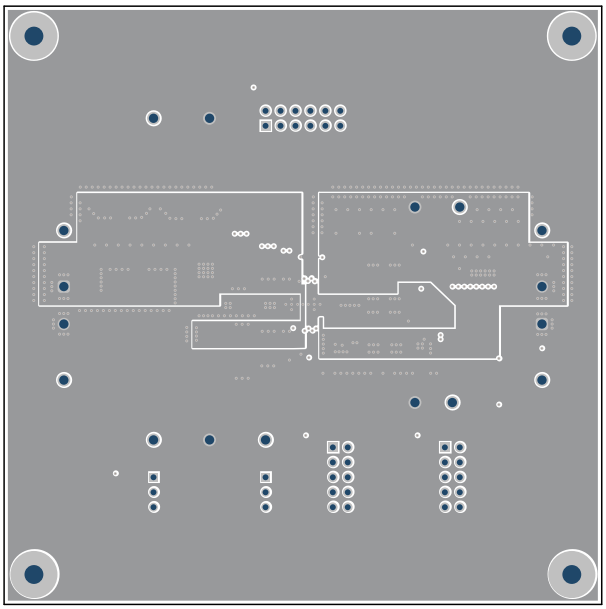


Figure 4-6. Mid Layer 3 Layout

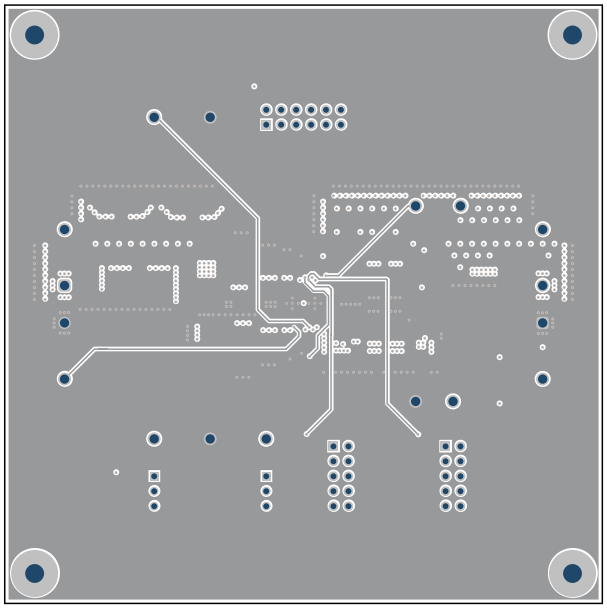


Figure 4-7. Mid Layer 4 Layout

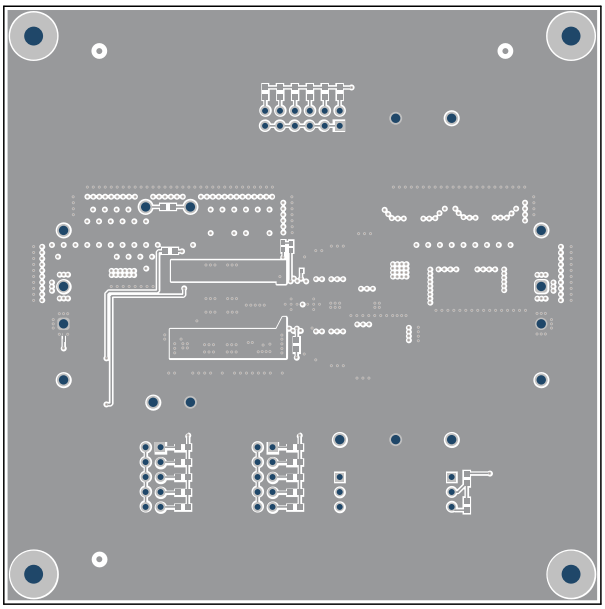


Figure 4-8. Bottom Layer Layout

5 Schematic and Bill of Materials

This section presents the TPSM843A26EVM schematic and bill of materials.

5.1 Schematic

Figure 5-1 is the schematic for TPSM843A26EVM.

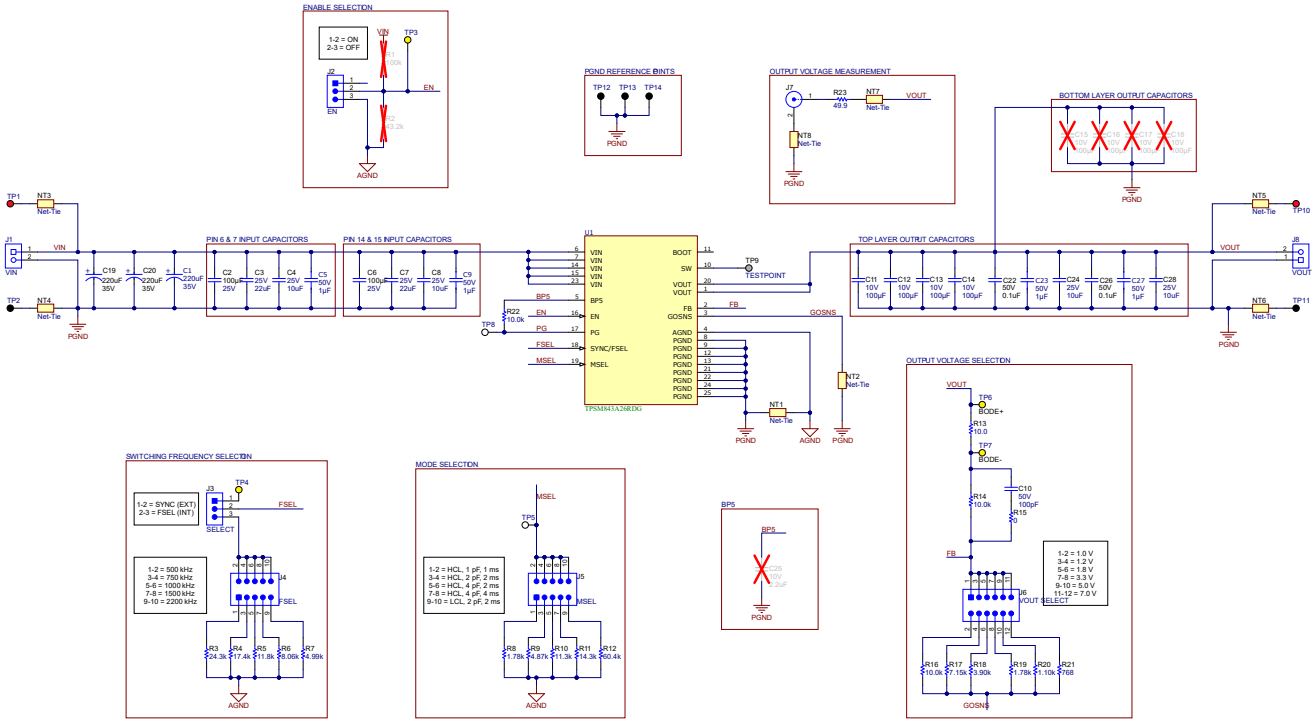


Figure 5-1. U1 Schematic

5.2 Bill of Materials

Table 5-1 presents the bill of materials for the TPSM843A26EVM.

Table 5-1. TPSM843A26EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		BSR228	Any
C1, C19, C20	3	220 µF	220 µF 35-V Aluminum - Polymer Capacitors Radial, Can - SMD 22 mOhm 2000 Hrs at 105°C	SMT_ECAP_10MM3_10MM3	8.75076E+11	Wurth Electronics
C2, C6	2	100 uF	CAP, CERM, 100 µF, 25 V,+/- 20%, X7R, 6x5x5mm	6x5x5mm	CKG57NX7R1E107M500JH	TDK
C3, C7	2	22 uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X7R, 1210	1210	GRM32ER71E226KE15L	MuRata
C4, C8, C24, C28	4	10 uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7S, 0805	0805	GRM21BC71E106KE11L	MuRata
C5, C9, C23, C27	4	1 µF	Ceramic Capacitor, 1uF ±10% 50VDC X7R 0805 Embossed T/R	0805	GCM21BR71H105KA03L	Murata
C10	1	100 pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1H101JA01D	MuRata
C11, C12, C13, C14	4	100 uF	CAP, CERM, 100 µF, 10 V,+/- 20%, X5R, 1210	1210	GRM32ER61A107ME20K	MuRata
C22, C26	2	0.1 uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	0402	C1005X7R1H104K050BB	TDK
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J8	2		Terminal Block, 6.35mm, 2x1, TH	On-Shore_OSTT7020150	OSTT7020150	On-Shore Technology
J2, J3	2		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
J4, J5	2		Header, 100mil, 5x2, Tin, TH	Header, 5x2, 100mil, Tin	PEC05DAAN	Sullins Connector Solutions
J6	1		Header, 100mil, 6x2, Tin, TH	Header, 6x2, 100mil, Tin	PEC06DAAN	Sullins Connector Solutions
J7	1		Connector, Receptacle, 50 ohm, TH	SMB Connector	SMBR004D00	JAE Electronics
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R3	1	24.3k	RES, 24.3 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060324K3FKEA	Vishay-Dale

Table 5-1. TPSM843A26EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R4	1	17.4k	RES, 17.4 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060317K4FKEA	Vishay-Dale
R5	1	11.8k	RES, 11.8 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060311K8FKEA	Vishay-Dale
R6	1	8.06k	RES, 8.06 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06038K06FKEA	Vishay-Dale
R7	1	4.99k	RES, 4.99 k, 1%, 0.1 W, 0603	0603	CRCW06034K99FKEAC	Vishay-Dale
R8, R19	2	1.78k	RES, 1.78 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K78FKEA	Vishay-Dale
R9	1	4.87k	RES, 4.87 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034K87FKEA	Vishay-Dale
R10	1	11.3k	RES, 11.3 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060311K3FKEA	Vishay-Dale
R11	1	14.3k	RES, 14.3 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060314K3FKEA	Vishay-Dale
R12	1	60.4k	RES, 60.4 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060360K4FKEA	Vishay-Dale
R13	1	10	RES, 10.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0FKEA	Vishay-Dale
R14, R16, R22	3	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R15	1	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R17	1	7.15k	RES, 7.15 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06037K15FKEA	Vishay-Dale
R18	1	3.90k	RES, 3.90 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06033K90FKEA	Vishay-Dale
R20	1	1.10k	RES, 1.10 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K10FKEA	Vishay-Dale
R21	1	768	RES, 768, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603768RFKEA	Vishay-Dale
R23	1	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
SH-J2, SH-J3, SH-J4, SH-J5, SH-J6	5	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP10	2		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone Electronics
TP2, TP11, TP12, TP13, TP14	5		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone Electronics
TP3, TP4, TP6, TP7	4		Test Point, Multipurpose, Yellow, TH	Yellow Multipurpose Testpoint	5014	Keystone Electronics
TP5, TP8	2		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone Electronics

Table 5-1. TPSM843A26EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U1	1		High-efficiency 18-V, 16-A synchronous buck converter module, B3QFN25	B3QFN25	TPSM843A26RDG	Texas Instruments
C15, C16, C17, C18	0	100uF	CAP, CERM, 100 µF, 10 V,+/- 20%, X5R, 1210	1210	GRM32ER61A107ME20K	MuRata
C25	0	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X5R, 0402	0402	C1005X5R1A225K050BC	TDK
R1	0	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R2	0	43.2k	RES, 43.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060343K2FKEA	Vishay-Dale

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

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2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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