Application Report

Calculating Power Dissipation for a H-Bridge or Half Bridge Driver

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ABSTRACT

When selecting an integrated H-bridge or Half bridge driver for a motor application or a load with inductive characteristics, it is imperative to consider the power dissipated on the driver due to the load current and PWM switching of the ouput for current regulation. Power dissipated on the device raises the junction temperature of the device over the ambient temperature depending on the thermal impedance. The thermal impedance depends on characteristics of the IC (packaging, die size, and so forth) and PCB design, which often is the limiting factor in how much current a given driver provides. To calculate the maximum allowable current in a given application, an estimation of the total motor driver power dissipation is needed. This application report shows how to estimate this power dissipation for the power FETs and the entire device itself in each case.

Table of Contents

1 Sources of Power Dissipation in an Integrated Driver

There are **two** fundamental sources of power dissipation on the power FETs in a driver IC.

1. Power dissipation from conduction loss of each FET due to its on-resistance is given by:

   $\mathbf{P_{RON}\ [W] = R_{ON} \times I_L^2}$, where, (1)

   a. R_{ON} = FET on-resistance [ohm]
   b. I_L = Load current [A]

   Note that R_{ON} increases with temperature. So as the device heats up, the power dissipation also increases. This must be considered when calculating the total device power dissipation. Typically, the R_{ON} approximately doubles its value at 150 Cº compared to room temperature at 25 Cº.

2. Power dissipation due to switching losses associated with PWM based current regulation can be **approximated** with the following expressions:

   a. Power dissipation due to output slewing during rising and falling edges is given by:

   $\mathbf{P_{SW1}\ [W] = (0.5 \times V_M \times I_L \times V_M / SR_{rise} \times f_{PWM}) + (0.5 \times V_M \times I_L \times V_M / SR_{fall} \times f_{PWM})}$, where, (2)

      i. f_{PWM} = PWM switching frequency [Hz]
      ii. V_M = Supply voltage to the driver [V]
      iii. I_L = Load current [A]
      iv. SR_{rise} = Output voltage slew rate during rise [V/sec]
      v. SR_{fall} = Output voltage slew rate during fall [V/sec]

      Output slewing rate is a balance between EM (Electro magnetic) performance and device power dissipation.

   b. Power dissipation due to the dead times between switching FETs is given by:

   $\mathbf{P_{SW2}\ [W] = (V_D \times I_L \times tDEAD_{rise} \times f_{PWM}) + (V_D \times I_L \times tDEAD_{fall} \times f_{PWM})}$, where, (3)

      i. f_{PWM} = PWM switching frequency [Hz]
      ii. V_D = FET body diode forward bias voltage [V]
      iii. I_L = Load current [A]
      iv. $tDEAD_{rise}$ = dead time during rise [sec]
      v. $tDEAD_{fall}$ = dead time during fall [sec]

      Dead times are necessary to mitigate any risk of current shoot through between the switching power FETs. Integrated FET drivers often have a feedback based self timed FET switching sequence to ensure the smallest possible dead times while avoiding any shoot through current.

   c. Power dissipation due to OUTPUT slewing during FET turn ON in the recirculation path is given by:

   $\mathbf{P_{SW3}\ [W] = (0.5 \times V_D \times I_L \times V_D / SR_{rise} \times f_{PWM}) + (0.5 \times V_D \times I_L \times V_D / SR_{fall} \times f_{PWM})}$, where, (4)

      i. f_{PWM} = PWM switching frequency [Hz]
      ii. V_D = FET body diode forward bias voltage [V]
      iii. I_L = Load current [A]
      iv. SR_{rise} = Output voltage slew rate during rise [V/sec]
      v. SR_{fall} = Output voltage slew rate during fall [V/sec]

      This dissipation is typically **not** considered as it is quite insignificant.

   d. Power dissipation also occurs due to reverse recovery losses of switching FET. This occurs due to change in current direction of the forward biased body diode of a typically large power FETs (R_{DSON} < ~100 mΩ). These losses typically limit the power dissipation savings at the higher slew rates (> 25 V/µsec). This dissipation is also typically **not** considered as it is quite insignificant.

3. Power dissipation due to device current consumption, given by,

   $\mathbf{P_{IVM}\ [W] = V_M \times I_{VM}}$, where, (5)

a. V_M = Supply voltage to the driver [V]
b. I_{VM} = Device operating supply current [A]

This dissipation is typically **not** considered as it is quite insignificant, given that I_{VM} is typically ~5 - 10 mA.

4. Some driver devices have an external LDO regulator output available that is used to provide some reference current, or current to power external loads. Power dissipation due to this external load current is given by,

$$P_{LDO}\ [W] = (V_M - V_{LDO}) \times I_{LDO} \text{, where,} \tag{6}$$

a. V_M = Supply voltage to the driver [V]
b. V_{LDO} = LDO output voltage [V]
c. I_{LDO} = External load current [A]

This dissipation is typically **not** considered as it is quite insignificant.

In summary, power dissipation total is given by:

$$P_{TOT} = P_{RON} + P_{SW1} + P_{SW2} + P_{SW3} + P_{IVM} + P_{LDO} \tag{7}$$

Typically, this can be approximated to just three sources, given by:

$$P_{TOT} = \sim(P_{RON} + P_{SW1} + P_{SW2}) \tag{8}$$

The next set of sub-sections show the power dissipation in each power FET for conduction and switching losses based on the application configuration (H-bridge or Half bridge driver using high-side or low-side recirculation).

1.1 H-Bridge

1.1.1 H-Bridge Driver Using High-Side Recirculation

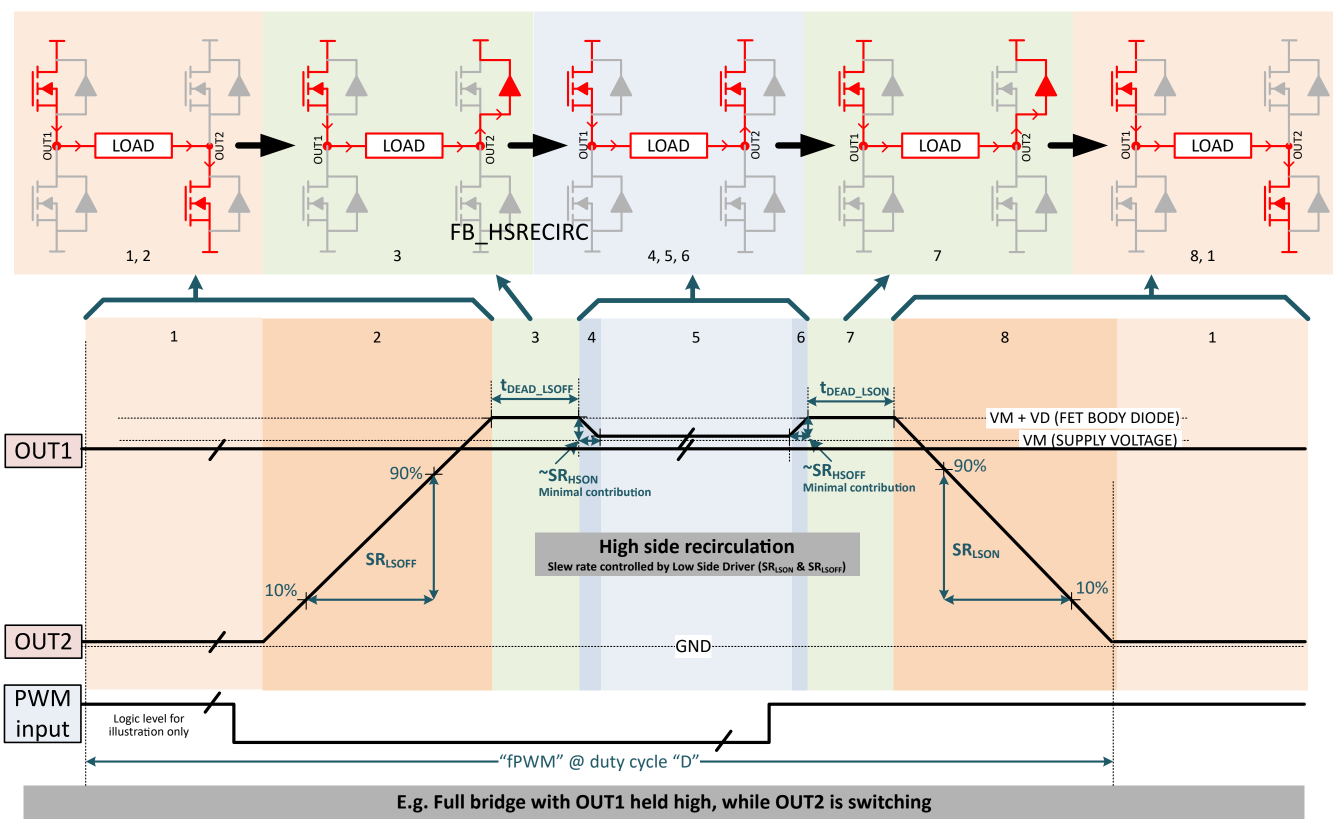

Figure 1-1. H-Bridge Using High-Side Recirculation

Figure 1-1 shows the switching sequence of a full bridge in PWM regulation between HS1 - load - LS2 (region # 1) and HS1 - load - HS2 (region # 5) with other transitions (region # 2, 3 & 4 for rising edge and region # 6, 7 & 8 for falling edge). The power dissipation on each FET is as follows:

Table 1-1. Power Dissipation for H-Bridge with High-Side Recirculation

Region	Time ratio within PWM cycle	HS1 [W]	LS1 [W]	HS2 [W]	LS2 [W]
1	D = On-time × f_{PWM} 1	$R_{ON} \times I_L^{\ 2}$	0	0	$R_{ON} \times I_L^{\ 2}$
2	$V_M/SR_{LSOFF} \times f_{PWM}$	$R_{ON} \times I_L^{\ 2}$	0	0	$0.5 \times V_M \times I_L$
3	$t_{DEAD\_LSOFF} \times f_{PWM}$	$R_{ON} \times I_L^{\ 2}$	0	$V_D \times I_L$	0
4	$V_D/SR_{HSON} \times f_{PWM}$	$R_{ON} \times I_L^{\ 2}$	0	$0.5 \times V_D \times I_L$	0
5	$(1 - D)$ = Off-time × f_{PWM} 1	$R_{ON} \times I_L^{\ 2}$	0	$R_{ON} \times I_L^{\ 2}$	0
6	$V_D/SR_{HSOFF} \times f_{PWM}$	$R_{ON} \times I_L^{\ 2}$	0	$0.5 \times V_D \times I_L$	0
7	$t_{DEAD\_LSON} \times f_{PWM}$	$R_{ON} \times I_L^{\ 2}$	0	$V_D \times I_L$	0
8	$V_M/SR_{LSON} \times f_{PWM}$	$R_{ON} \times I_L^{\ 2}$	0	0	$0.5 \times V_M \times I_L$

1. If the slew time is significant portion of the PWM period, we recommend to adjust the duty cycle number based on slew times for regions # 1 and 5.

In Table 1-1,

1. R_{ON} = FET on-resistance [ohm]
2. f_{PWM} = PWM switching frequency [Hz]
3. V_M = Supply voltage to the driver [V]
4. I_L = Load current [A]
5. D = PWM duty cycle [a fractional number between 0 and 1]
6. SR_{LSOFF} = Output voltage slew rate during rise when LS2 is turned off [V/sec]
7. SR_{LSON} = Output voltage slew rate during fall when LS2 is turned on [V/sec]
8. V_D = FET body diode forward bias voltage [V]
9. t_{DEAD_LSOFF} = dead time after LS2 has been turned off [sec]
10. t_{DEAD_LSON} = dead time before LS2 is turned on [sec]
11. SR_{HSON} = Output voltage slew rate during rise when HS2 is turned on [V/sec]
12. SR_{HSOFF} = Output voltage slew rate during fall when HS2 is turned off [V/sec]

If we assume power dissipation in regions #4 and #6 are negligible, slews rate match for rising and falling edges, dead times are equal, then power dissipation for each FET can be approximated as follows:

1. $P_{HS1} = R_{ON} \times I_L^{\ 2}$
2. $P_{LS1} = 0$
3. $P_{HS2} = [R_{ON} \times I_L^{\ 2} \times (1-D)] + [2 \times V_D \times I_L \times t_{DEAD} \times f_{PWM}]$
4. $P_{LS2} = [R_{ON} \times I_L^{\ 2} \times D] + [V_M \times I_L \times (V_M / SR) \times f_{PWM}]$

For estimating power dissipation for load current flow in the reverse direction, identical equations apply, with only swapping of HS1 with HS2 and LS1 with LS2.

1.1.2 H-Bridge Driver Using Low-Side Recirculation

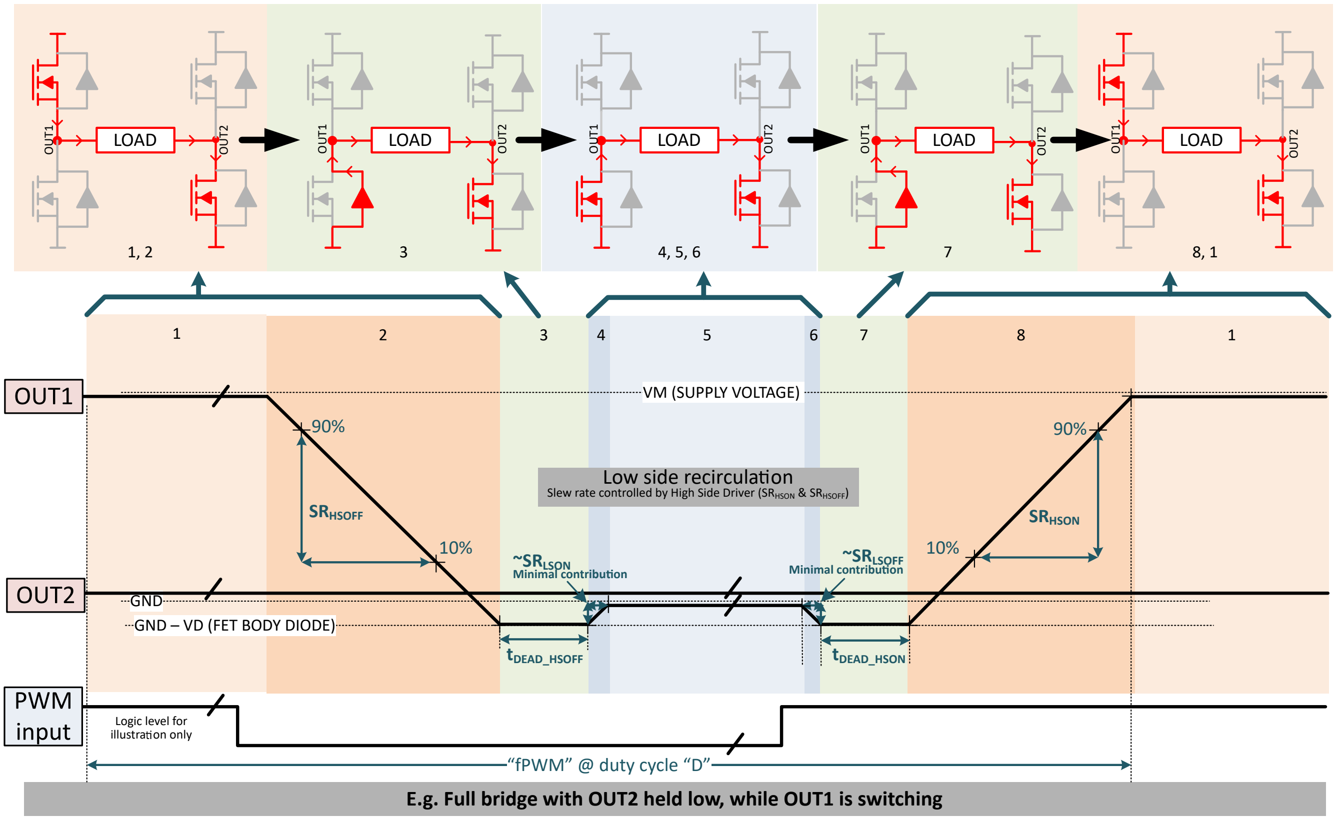

Figure 1-2. H-Bridge Using Low-Side Recirculation

Figure 1-2 shows the switching sequence of a full bridge in PWM regulation between HS1 - load - LS2 (region # 1) and LS1 - load - LS2 (region # 5) with other transitions (region # 2, 3 & 4 for rising edge and region # 6, 7 & 8 for falling edge). The power dissipation on each FET is as follows:

Table 1-2. Power Dissipation for H-Bridge with Low-Side Recirculation

Region	Time ratio within PWM cycle	LS2 [W]	HS2 [W]	LS1 [W]	HS1 [W]
1	D[1]	$R_{ON} \times I_L{}^2$	0	0	$R_{ON} \times I_L{}^2$
2	$V_M/SR_{LSOFF} \times f_{PWM}$	$R_{ON} \times I_L{}^2$	0	0	$0.5 \times V_M \times I_L$
3	$t_{DEAD\_LSOFF} \times f_{PWM}$	$R_{ON} \times I_L{}^2$	0	$V_D \times I_L$	0
4	$V_D/SR_{HSON} \times f_{PWM}$	$R_{ON} \times I_L{}^2$	0	$0.5 \times V_D \times I_L$	0
5	$(1 - D)$[1]	$R_{ON} \times I_L{}^2$	0	$R_{ON} \times I_L{}^2$	0
6	$V_D/SR_{HSOFF} \times f_{PWM}$	$R_{ON} \times I_L{}^2$	0	$0.5 \times V_D \times I_L$	0
7	$t_{DEAD\_LSON} \times f_{PWM}$	$R_{ON} \times I_L{}^2$	0	$V_D \times I_L$	0
8	$V_M/SR_{LSON} \times f_{PWM}$	$R_{ON} \times I_L{}^2$	0	0	$0.5 \times V_M \times I_L$

1. If the slew time is significant portion of the PWM period, we recommend to adjust the duty cycle number based on slew times for regions # 1 and 5.

In Table 1-2,

1. R_{ON} = FET on-resistance [ohm]
2. f_{PWM} = PWM switching frequency [Hz]
3. V_M = Supply voltage to the driver [V]
4. I_L = Load current [A]
5. D = PWM duty cycle between 0 and 1
6. SR_{HSOFF} = Output voltage slew rate during rise when HS1 is turned off [V/sec]
7. SR_{HSON} = Output voltage slew rate during fall when HS1 is turned on [V/sec]

8. V_D = FET body diode forward bias voltage [V]
9. t_{DEAD_HSOFF} = dead time after HS1 has been turned off [sec]
10. t_{DEAD_HSON} = dead time before HS1 is turned on [sec]
11. SR_{LSON} = Output voltage slew rate during rise when LS1 is turned on [V/sec]
12. SR_{LSOFF} = Output voltage slew rate during fall when LS1 is turned off [V/sec]

If we assume power dissipation in regions #4 and #6 are negligible, slews rate match for rising and falling edges, dead times are equal, then power dissipation for each FET can be approximated as follows:

1. $P_{LS2} = R_{ON} \times I_L^{\ 2}$
2. $P_{HS2} = 0$
3. $P_{LS1} = [R_{ON} \times I_L^{\ 2} \times (1\text{-}D)] + [2 \times V_D \times I_L \times t_{DEAD} \times f_{PWM}]$
4. $P_{HS1} = [R_{ON} \times I_L^{\ 2} \times D] + [V_M \times I_L \times (V_M / SR) \times f_{PWM}]$

For estimating power dissipation for load current flow in the reverse direction, identical equations apply, with only swapping of HS1 with HS2 and LS1 with LS2.

1.2 Half Bridge

1.2.1 Half Bridge Driver Using High-Side Recirculation

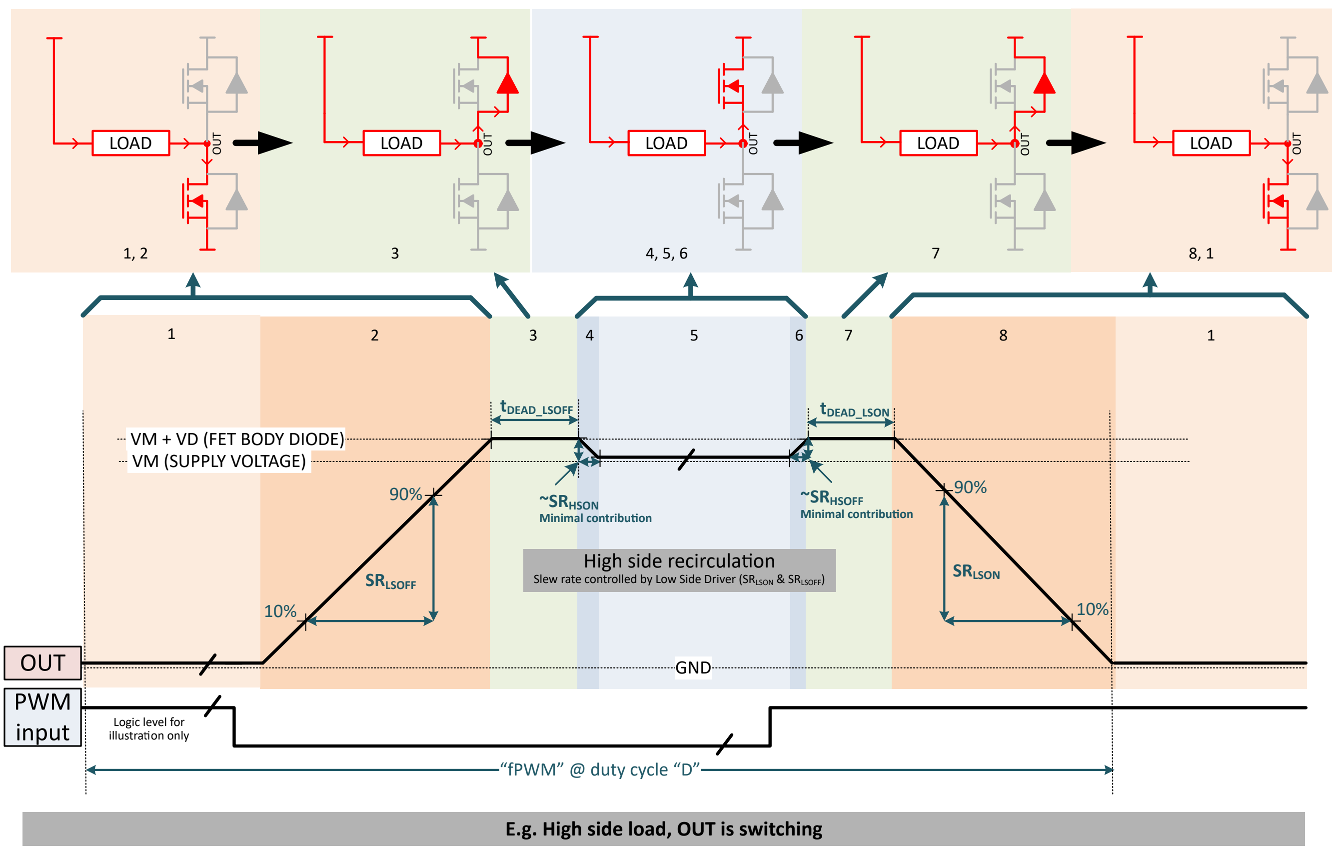

Figure 1-3. Half Bridge Driver Using High-Side Recirculation

The above figure shows the switching sequence of a half bridge in PWM regulation between Load - LS (region # 1) and Load - HS (region # 5) with other transitions (region # 2, 3 & 4 for rising edge and region # 6, 7 & 8 for falling edge). The load is assumed to be a high side load (connected directly to supply or through a external high side FET). The power dissipation on each FET is as follows:

Table 1-3. Power Dissipation for Half-Bridge with High-Side Recirculation

Region	Time ratio within PWM cycle	HS [W]	LS [W]
1	D_1	0	$R_{ON} \times I_L^{\ 2}$
2	$V_M/SR_{LSOFF} \times f_{PWM}$	0	$0.5 \times V_M \times I_L$

Table 1-3. Power Dissipation for Half-Bridge with High-Side Recirculation (continued)

Region	Time ratio within PWM cycle	HS [W]	LS [W]
3	t_{DEAD_LSOFF} x f_{PWM}	V_D x I_L	0
4	V_D/SR_{HSON} x f_{PWM}	0.5 x V_D x I_L	0
5	(1 - D)[1]	$R_{ON} \times I_L^{\ 2}$	0
6	V_D/SR_{HSOFF} x f_{PWM}	0.5 x V_D x I_L	0
7	t_{DEAD_LSON} x f_{PWM}	V_D x I_L	0
8	V_M/SR_{LSON} x f_{PWM}	0	0.5 x V_M x I_L

1. If the slew time is significant portion of the PWM period, we recommend to adjust the duty cycle number based on slew times for regions # 1 and 5.

InTable 1-3 ,

1. R_{ON} = FET on-resistance [ohm]
2. f_{PWM} = PWM switching frequency [Hz]
3. V_M = Supply voltage to the driver [V]
4. I_L = Load current [A]
5. D = PWM duty cycle between 0 and 1
6. SR_{LSOFF} = Output voltage slew rate during rise when LS is turned off [V/sec]
7. SR_{LSON} = Output voltage slew rate during fall when LS is turned on [V/sec]
8. V_D = FET body diode forward bias voltage [V]
9. t_{DEAD_LSOFF} = dead time after LS has been turned off [sec]
10. t_{DEAD_LSON} = dead time before LS is turned on [sec]
11. SR_{HSON} = Output voltage slew rate during rise when HS is turned on [V/sec]
12. SR_{HSOFF} = Output voltage slew rate during fall when HS is turned off [V/sec]

If we assume power dissipation in regions #4 and #6 are negligible, slews rate match for rising and falling edges, dead times are equal, then power dissipation for each FET can be approximated as follows:

1. $P_{HS} = [R_{ON} \times I_L^{\ 2} \text{ x } (1\text{-}D)] + [2 \text{ x } V_D \text{ x } I_L \text{ x } t_{DEAD} \text{ x } f_{PWM}]$
2. $P_{LS} = [R_{ON} \times I_L^{\ 2} \text{ x } D] + [V_M \text{ x } I_L \text{ x } (V_M / SR) \text{ x } f_{PWM}]$

Compared to a H-bridge driver, the power dissipation due to conduction losses is approximately cut in half, however, the switching losses remain the same.

1.2.2 Half Bridge Driver Using Low-Side Recirculation

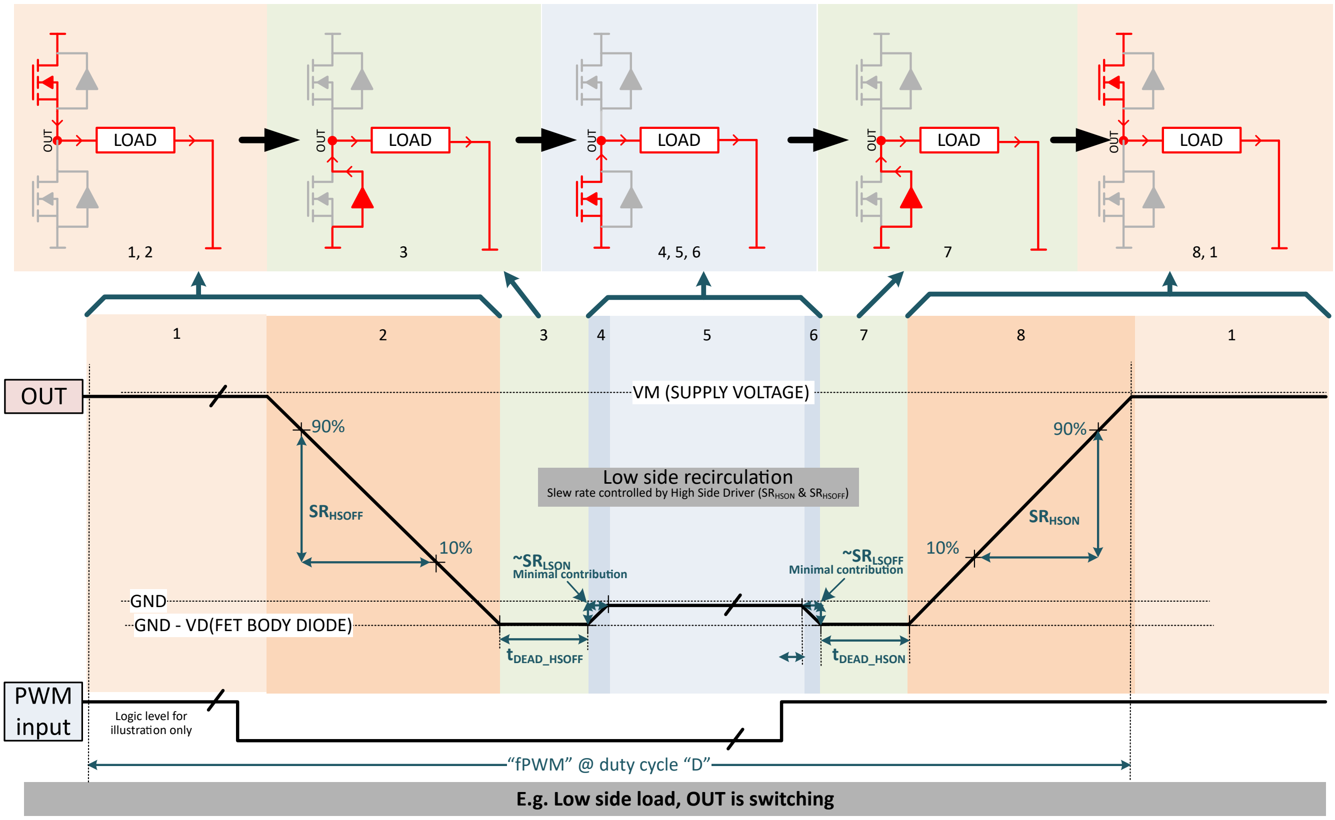

Figure 1-4. Half Bridge Driver Using Low-Side Recirculation

Figure 1-4 shows the switching sequence of a half bridge in PWM regulation between HS - Load (region # 1) and LS - Load (region # 5) with other transitions (region # 2, 3 & 4 for rising edge and region # 6, 7 & 8 for falling edge). The power dissipation on each FET is as follows:

Table 1-4. Power Dissipation for Half-Bridge with Low-Side Recirculation

Region	Time ratio within PWM cycle	LS [W]	HS [W]
1	D_1	0	$R_{ON} \times I_L{}^2$
2	V_M/SR_{LSOFF} x f_{PWM}	0	0.5 x V_M x I_L
3	t_{DEAD_LSOFF} x f_{PWM}	V_D x I_L	0
4	V_D/SR_{HSON} x f_{PWM}	0.5 x V_D x I_L	0
5	$(1 - D)_1$	$R_{ON} \times I_L{}^2$	0
6	V_D/SR_{HSOFF} x f_{PWM}	0.5 x V_D x I_L	0
7	t_{DEAD_LSON} x f_{PWM}	V_D x I_L	0
8	V_M/SR_{LSON} x f_{PWM}	0	0.5 x V_M x I_L

1. If the slew time is significant portion of the PWM period, we recommend to adjust the duty cycle number based on slew times for regions # 1 and 5.

In Table 1-4,

1. R_{ON} = FET on-resistance [ohm]
2. f_{PWM} = PWM switching frequency [Hz]
3. V_M = Supply voltage to the driver [V]
4. I_L = Load current [A]
5. D = PWM duty cycle between 0 and 1
6. SR_{HSOFF} = Output voltage slew rate during rise when HS is turned off [V/sec]
7. SR_{HSON} = Output voltage slew rate during fall when HS is turned on [V/sec]

8. V_D = FET body diode forward bias voltage [V]
9. t_{DEAD_HSOFF} = dead time after HS has been turned off [sec]
10. t_{DEAD_HSON} = dead time before HS is turned on [sec]
11. SR_{LSON} = Output voltage slew rate during rise when LS is turned on [V/sec]
12. SR_{LSOFF} = Output voltage slew rate during fall when LS is turned off [V/sec]

If we assume power dissipation in regions #4 and #6 are negligible, slews rate match for rising and falling edges, dead times are equal, then power dissipation for each FET can be approximated as follows:

1. $P_{LS} = [R_{ON} \times I_L{}^2 \times (1-D)] + [2 \times V_D \times I_L \times t_{DEAD} \times f_{PWM}]$
2. $P_{HS} = [R_{ON} \times I_L{}^2 \times D] + [V_M \times I_L \times (V_M / SR) \times f_{PWM}]$

Compared to a H-bridge driver, the power dissipation due to conduction losses is approximately cut in half, however, the switching losses remain the same.

2 Example Calculation

This section shows examples of power dissipation calculation for Full-Bridge and Half-Bridge motor drivers. The following values will be used for the calculations below.

- R_{ON} = 100 mΩ
- f_{PWM} = 20 KHz
- V_M = 13.5 V
- I_L = 1 A
- D = 50%
- SR_{LSOFF} = (13.5 V/µs)
- SR_{LSON} = (13.5 V/µs)
- V_D = 1 V
- t_{DEAD_LSOFF} = 100 ns
- t_{DEAD_LSON} = 100 ns
- SR_{HSON} = (13.5 V/µs)
- SR_{HSOFF} = (13.5 V/µs)
- I_{IVM} = 10 mA
- V_{LDO} = 5 V supports an external load of I_{LDO} = 5 mA (External load support is supported only in some devices.)

2.1 H-Bridge

2.1.1 High-Side Recirculation Example

Table 2-1. Power dissipation for H-Bridge with high-side recirculation

Region	Time ratio within PWM cycle	HS1 [W]	LS1 [W]	HS2 [W]	LS2 [W]
1	50% = On-time × 20 KHz[1]	100 mΩ × $1A^2$	0	0	100 mΩ × $1A^2$
2	13.5 V/(13.5 V/µs) x 20 KHz	100 mΩ × $1A^2$	0	0	0.5 x 13.5 V x 1 A
3	100 ns x 10 KHz	100 mΩ × $1A^2$	0	1 V x 1 A	0
4	1 V/(13.5 V/µs) x 20 KHz	100 mΩ × $1A^2$	0	0.5 x 1 V x 1 A	0
5	(1 - 50%) = Off-time × 20 KHz[1]	100 mΩ × $1A^2$	0	100 mΩ × $1A^2$	0
6	1 V/(13.5 V/µs) x 20 KHz	100 mΩ × $1A^2$	0	0.5 x 1 V x 1 A	0
7	100 ns x 20 KHz	100 mΩ × $1A^2$	0	1 V x 1 A	0
8	13.5 V/(13.5 V/µs) x 20 KHz	100 mΩ × $1A^2$	0	0	0.5 x 13.5 V x 1 A

P_{HS1} = 100 mΩ × 1 A^2 = 0.1 W

P_{LS1} = 0

P_{HS2} = [100 mΩ × 1 A^2 x (1-0.5)] + [2 x 1 V x 1 A x 100 ns x 20 KHz] = 0.054 W

P_{LS2} = [100 mΩ × 1 A^2x 0.5] + [13.5 x 1 A x 13.5 V/ (13.5 V/µs) x 20 KHz] = 0.32 W

It is not necessary to include P_{IVM} and P_{LDO} as their impact is usually minimal enough to be inconsequential. That being said, they can be calculated as:

P_{IVM} = 13.5 V × 10 mA = 0.135 W and P_{LDO} = 5 mA × (13.5 V - 5 V) = 0.0425 W

P_{TOT} = P_{HS1} + P_{LS1} + P_{HS2} + P_{LS2} = 0.1 + 0 + 0.054 + 0.32 = 0.474 W

or P_{TOT} = 0.474 W + P_{IVM} + P_{LDO} = 0.6515 W

2.1.2 Low-Side Recirculation Example

Table 2-2. Power dissipation for H-Bridge with low-side recirculation

Region	Time ratio within PWM cycle	LS2 [W]	HS2 [W]	LS1 [W]	HS1 [W]
1	50%	100 mΩ × 1 A^2	0	0	100 mΩ × 1 A^2
2	13.5 V/13.5 V/µs x 20 KHz	100 mΩ × 1 A^2	0	0	0.5 x 13.5 V x 1 A
3	100 ns x 20 KHz	100 mΩ × 1 A^2	0	1 V x 1 A	0
4	1 V/13.5 V/µs x 20 KHz	100 mΩ × 1 A^2	0	0.5 x 1 V x 1 A	0

Table 2-2. Power dissipation for H-Bridge with low-side recirculation (continued)

Region	Time ratio within PWM cycle	LS2 [W]	HS2 [W]	LS1 [W]	HS1 [W]
5	(1 - 50%)	100 mΩ × 1 A^2	0	100 mΩ × 1 A^2	0
6	1 V/13.5 V/µs x 20 KHz	100 mΩ × 1 A^2	0	0.5 x 1 V x 1 A	0
7	100 ns x 20 KHz	100 mΩ × 1 A^2	0	1 V x 1 A	0
8	13.5 V/13.5 V/µs x 20 KHz	100 mΩ × 1 A^2	0	0	0.5 x 13.5 V x 1 A

P_{LS2} = 100 mΩ × 1 A^2 = 0.1 W

P_{HS2} = 0 W

P_{LS1} = [100 mΩ × 1 A^2 x (1-0.5)] + [2 x 1 V × 1 A x 100 ns x 20 KHz] = 0.054 W

P_{HS1} = [100 mΩ × 1 A^2 x 0.5] + [13.5 V x 1 A x 13.5 V / 13.5 V/µs x 20 KHz] = 0.32 W

P_{TOT} = 0.1 + 0 + 0.054 + 0.32 = 0.474 W or P_{TOT} = 0.6515 W if P_{IVM} and P_{LDO} are included. These values are the same as the H-Bridge in High-Side Recirculation.

2.2 Half Bridge

2.2.1 Half-Bridge High-Side Recirculation Example

Table 2-3. Power dissipation for Half-Bridge with high-side recirculation

Region	Time ratio within PWM cycle	HS [W]	LS [W]
1	50%	0	100 mΩ × 1 A^2
2	13.5 V/13.5 V/µs x 20 KHz	0	0.5 x 13.5 V x 1 A
3	100 ns x 20 KHz	1 V x 1 A	0
4	1 V/13.5 V/µs x 20 KHz	0.5 x 1 V x 1 A	0
5	(1 - 50%)	100 mΩ × 1 A^2	0
6	1 V/13.5 V/µs x 20 KHz	0.5 x 1 V x 1 A	0
7	100 ns x 20 KHz	1 V x 1 A	0
8	13.5 V/13.5 V/µs x 20 KHz	0	0.5 x 13.5 V x 1 A

P_{HS} = [100 mΩ × 1 A^2 x (1-0.5)] + [2 x 1 V x 1 A x 100 ns x 20 KHz] = 0.054 W

P_{LS} = [100 mΩ × 1 A^2 x 0.5] + [13.5 V x 1 A x 13.5 V / 13.5 V/µs x 20 KHz] = 0.32 W

P_{TOT} = 0.054 + 0.32 = 0.374 W

2.2.2 Half-Bridge Low-Side Recirculation Example

Table 2-4. Power dissipation for Half-Bridge with low-side recirculation

Region	Time ratio within PWM cycle	LS [W]	HS [W]
1	50 %	0	100 mΩ × 1 A^2
2	13.5 V/13.5 V/µs x 20 KHz	0	0.5 x 1 V x 1 A
3	100 ns x 20 KHz	1 V x 1 A	0
4	1 V/13.5 V/µs x 20 KHz	0.5 x 1 V x 1 A	0
5	(1 - 50%)	100 mΩ × 1 A^2	0
6	1 V/13.5 V/µs x 20 KHz	0.5 x 1 V x 1 A	0
7	100 ns x 20 KHz	1 V x 1 A	0
8	13.5 V/13.5 V/µs x 20 KHz	0	0.5 x 13.5 V x 1 A

P_{LS} = [100 mΩ × 1 A^2 x (1-0.5)] + [2 x 1 V x 1A x 100 ns x 20 KHz] = 0.054 W

P_{HS} = [100 mΩ × 1 A^2 x 0.5] + [13.5 V x 1 A x 13.5 V / 13.5 V/µs x 20 KHz] = 0.32 W

P_{TOT} = 0.054 + 0.32 = 0.374 W

3 References

1. Texas Instruments, *Understanding Motor Driver Current Ratings* application report.
2. Texas Instruments, PCB Thermal Calculator .

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