Application Report
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TPS65381-Q1 and TPS65381A-Q1 Design Checklist

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ABSTRACT

This checklist is provided as an aid for customers of Texas Instruments related to their use of the TPS65381-Q1 and TPS65381A-Q1 (TPS65381x-Q1) device.

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Trademarks

1 Description

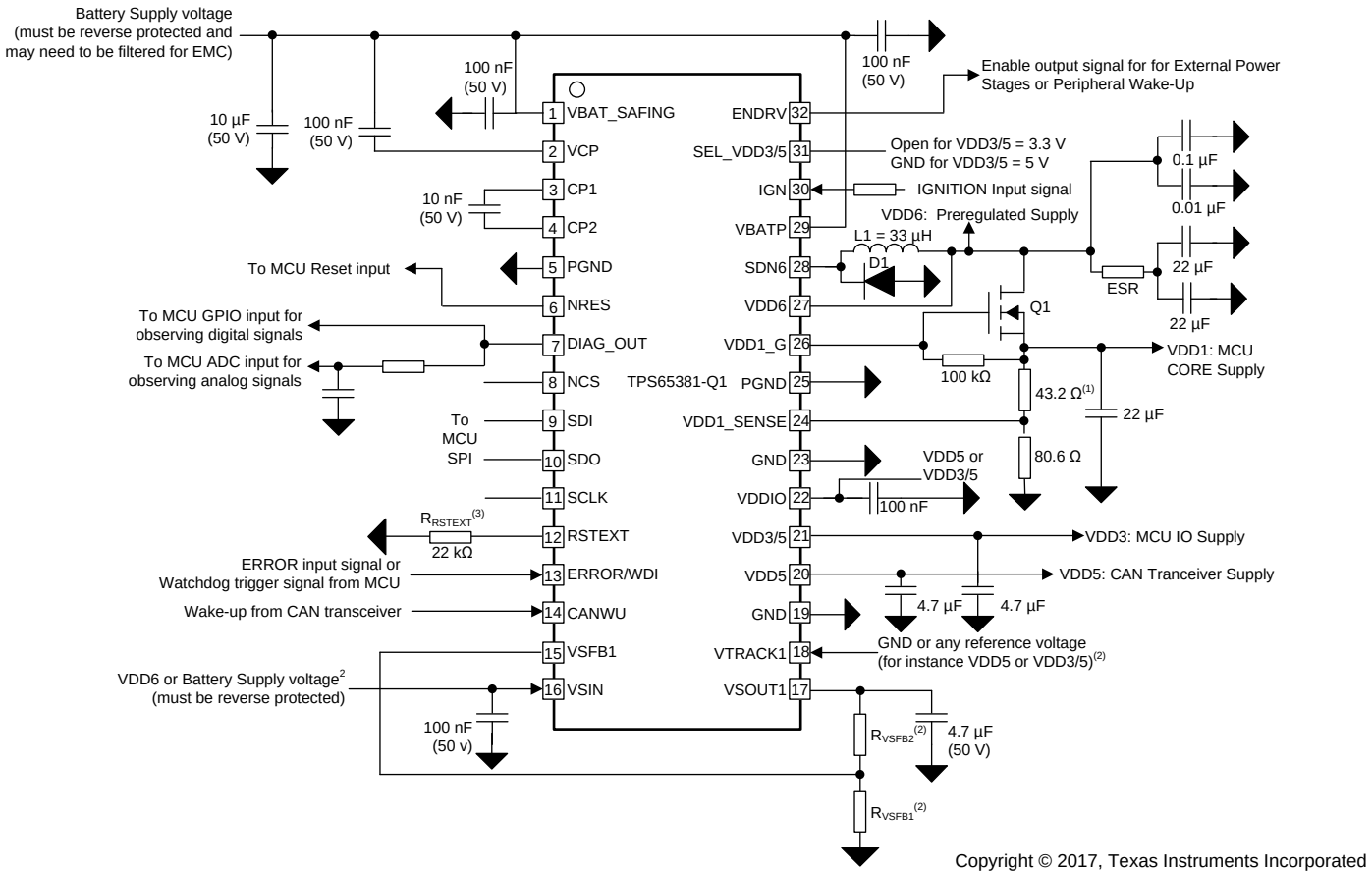
Refer to the corresponding data sheet for absolute maximum ratings and recommended operating conditions. The data sheet and other application notes have specific and more detailed application information. This checklist is a summary and intended to be used as a way to double check an application to help ensure the key points have been considered. To find the corresponding data sheet and additional information, go to www.ti.com/product/tps65381-q1 or www.ti.com/product/tps65381a-q1.

2 References

- *TPS65381-Q1 Multi-Rail Power Supply for Microcontrollers in Safety Applications*
- *TPS65381A-Q1 Multi-Rail Power Supply for Microcontrollers in Safety Applications*
- *AN-2162 Simple Success With Conducted EMI From DC-DC Converters*

3 Typical Application

Figure 1 shows a typical application.



A Example components:

- Q1: BUK9213-30A
- D1: Vishay SS3H09/10, OnSemi MBRS340T3
- L1: TDK CLF10060NIT-330M-D or COILCRAFT MSS1246T-333ML

Figure 1. Typical Application Diagram

4 Checklists

To enable a successful design, many design considerations must be considered. The following checklists should be used to help ensure key points for use of the TPS65381x-Q1 have been considered.

- Voltage regulator (VDDx and VSOUT1) use and configuration details: Refer to the regulator-specific section in the *Detailed Description* section and the *Application and Implementation* section of the device data sheet.
  - VDD6: Review the inductor (L), effective output capacitance ($C_{Effective}$), and controlled total effective series resistance (R_{ESR}) of the output capacitance to ensure it is balanced according to the information for the VDD6 preregulator in the *Detailed Design Procedure* of the device data sheet.
  - The resistor tolerance for resistor dividers, such as the feedback path in VDD1 and VSOUT1 regulators, adds to the regulation and voltage monitoring tolerance. TI recommends using 0.1% resistors or make sure total regulation and voltage monitoring tolerance including the impact from the resistor divider tolerance meets the application requirements.
- Capacitors: While selecting capacitors for the application consider the following characteristics so that the circuit has the specified effective capacitance required for this device at the application operating conditions:
  - The effective capacitance at the operating voltage must be used when selecting the proper capacitor. Capacitors derate with operating voltage (DC bias derating), sometimes as much as 70%. Therefore the effective capacitance of the circuit could be outside of the specified capacitance range in the data sheet if the DC bias derating is not considered.
  - The temperature and lifetime of the capacitor may also have an impact on the effective capacitance and should be considered.
  - The voltage ratings of the capacitor should be considered, especially on the high-voltage input circuits that may also experience transient voltages. The voltage ratings for the output capacitors should also consider any fault cases that may occur in the application.
  - The ESR for the capacitors should meet the requirements of the data sheet for the specific circuit.
- VDD6 inductor: While selecting the inductor for the application consider the following characteristics:
  - The minimum inductance is specified in the data sheet, L_{VDD6} minimum, 22 µH. This minimum includes the inductance tolerance, so the typical inductance of the inductor must be higher than L_{VDD6} minimum. The tolerance range of the selected inductor determines how close the typical inductance can be to L_{VDD6} minimum.
  - The peak switch current for SDN6 is specified in the TPS65381x-Q1 data sheet, I_{VDD6_limit}. The inductance should stay within the specified inductance range, L_{VDD6}, even if VDD6 is put into current limit which normally translates that the saturation current of the inductor needs to be higher than SDN6 current limit.
  - The impact of self heating or a temperature rise in the inductor should be included in the analysis so that the inductance stays in the specified inductance range, L_{VDD6}, throughout the operating range of the application.
- Consider the power dissipation of the device and system and design adequate thermal management. Special consideration and thermal management may be needed for high input voltages and load current applications. The *Derating Profile for Power Dissipation Based on High-K JEDEC PCB* figure in the data sheet provides a guideline, however all applications are unique and will not match the high-K JEDEC profile so thermal consideration or modeling should be done for each application. Ensure the thermal pad of the device is connected to the ground plane by thermal vias.
- Make sure the PCB layout of the design considers the key recommendations from the *Layout* section of the data sheet.
- The device has two main supply inputs, VBATP and VBAT_SAFING.
  - These supply inputs should be provided by a reverse protected supply. A simple Schottky diode can be used or for better low-voltage operation, an active-reverse protection supplied by charge pump (VCP) or other FET based scheme could be used.
  - For better EMC performance, a PI filter is suggested depending on the application requirements to reduce conducted emissions. This may also include the need to filter the main supply between the TPS65381x-Q1 and other high-current switching devices in the application such as a motor driver or other power output stage. To help with filter design, refer to Reference 3.

Table 1. Checklist by Device Pin (Applies to TPS65381-Q1 and TPS65381A-Q1)

Pin Name	Pin No.	Type	Signal	Description	External Circuit	If Not Used
VBAT_SAFING	1	Supply	PWR	Battery (supply) input for monitoring (VMON) and BG2 functions (must be reverse protected), should be connected to VBATP When below the minimum, the device does not start up and the NRES and ENDRV pins are low.	Supply from battery (main supply) with filter capacitor of minimum of 0.1 µF (ceramic, voltage rating higher than the main supply voltage). Supply must be reverse protected. For better EMC performance, a PI filter is suggested on the battery (main supply) depending on customer requirements to reduce conducted emission.	N/A
VCP	2	Power	PWR	Charge-pump output voltage	Storage capacitor with typical value of 0.1 µF to VBATP (ceramic, voltage rating higher than 20 V). If charge-pump output is used for system level reverse-battery protection circuit, a series resistance of about 10 kΩ must be connected between VCP and the gate of the NMOS-PowerFET.	N/A
CP1	3	Power	PWR	Charge-pump external capacitor, high-voltage side	Capacitor to CP2, 0.01 µF, typical (ceramic, voltage rating higher than the main supply voltage)	N/A
CP2	4	Power	PWR	Charge-pump external capacitor, low-voltage side	Capacitor to CP1, 0.01 µF, typical (ceramic, voltage rating higher than the main supply voltage)	N/A
PGND	5	GND	GND	Ground (Power)	Low-impedance ground plane	N/A
NRES	6	Digital	O	Hardware reset output signal for the microcontroller (active-low, internal pullup, open drain output)	Check at the system level if the internal pullup, $R_{NRES\_ENDRV\_PULLUP}$, meets system requirements.	Leave open
DIAG_OUT	7	Analog and Digital	O	Diagnostic output pin for diagnostic MUX. Internal analog (AMUX) and digital (DMUX) signal connection to MCU ADC and digital IO.	Connect to MCU ADC and GPIO. Analog internal signals through AMUX selection connect to MCU ADC. External filter may be required depending on MCU ADC. External filter and loading will impact stabilization time and steady state output level of analog signals. Digital internal signals via DMUX selection may connect to MCU GPIO.	Leave open
NCS	8	Digital	I	SPI chip select (active-low, internal pullup)	Low-value series resistors can be added to adjust delays, add current limiting between devices, and lower EMC if required. External pulup or pulldown resistors can be added as necessary for the application.	N/A[1]
SDI	9	Digital	I	SPI serial data IN (internal pulldown)		N/A[1]
SDO	10	Digital	O	SPI serial data OUT		N/A[1]
SCLK	11	Digital	I	SPI clock (internal pulldown)		N/A[1]
RSTEXT	12	Analog	I	Configuration pin to set reset extension time with resistor to GND	Resistor to GND, see the device data sheet. The maximum recommended resistance is 120 kΩ.	N/A
ERROR/WDI	13	Digital	I	Error input signal from MCU while using MCU Error Signal Monitor (ESM) (with watchdog in Q&A Mode), trigger input for the watchdog in Trigger Mode (MCU ESM not used). This pin is edge triggered.	For MCU error signal monitoring, connect to the output pin from the fault monitoring logic function of the MCU. Use the TPS65381x-Q1 watchdog in Q&A Mode. For Window Watchdog trigger input (watchdog in trigger mode) connect to an MCU output pin that is providing the watchdog trigger signal (MCU ESM should not be used while watchdog is in Trigger Mode).	Leave open
CANWU	14	Digital (HV)	I	Wake up input from CAN transceiver or other source. Wake up request latched via CANWU_L. (internal pulldown, I_CANWU)	Connect to the INH pin of the CAN transceiver or other wake-up source. Wake-up source must be reverse protected. If transients are present, filtering and clamping may be required and a series resistance of at least 10 kΩ is recommended.[2]	Leave open[3]
VSFB1	15	Analog	I	Feedback input reference for sensor-supply regulator (VSOUT1)	See the data sheet for VSOUT1 details and modes of operation. VSFB1 either is connected to VSOUT1 as follower or through a resistor-divider. 0.1% or better resistor tolerance is recommended to minimize the impact from the resistors on the total tolerance of regulation and UV/OV monitoring for VVSOUT1. Minimize the length of the feedback trace to prevent issues from noise. Do not route it near noise sources in the application.	GND
VSIN	16	Supply	PWR	Sensor-supply regulator input supply voltage (VSOUT1)	Minimum 0.1-µF capacitor to ground as close as possible to VSIN pin (ceramic, voltage rating higher than the supply voltage for VSIN). Higher capacitance may be required if VSOUT1 load transient performance is critical. VSIN may be supplied by VDD6 for lower-power dissipation or to VBATP in case a higher VSOUT1 output voltage is required.	Leave open

(1) While using the TPS65381x-Q1 without with the SPI is possible, doing so prevents configuring the device and access to internal monitoring and diagnostics. Upon power up, the device transitions through the RESET state to DIAGNOSTIC state and then locks in SAFE state.

(2) Either IGN or CANWU must be used to wake up the device.

(3) Either IGN or CANWU must be used to wake up the device from the STANDBY state. Therefore, either CANWU or IGN may be un-used, but not both, the device requires at least one wake-up source to transition from the STANDBY state into the powered states.

Table 1. Checklist by Device Pin (Applies to TPS65381-Q1 and TPS65381A-Q1) (continued)

Pin Name	Pin No.	Type	Signal	Description	External Circuit	If Not Used
VSOUT1	17	Power	PWR	VSOUT1 sensor-supply regulator output voltage	Minimum 0.5-µF effective output capacitance to ground as close as possible to pin (ceramic, voltage rating higher than VSOUT1). Higher output capacitance provides better stabilization and transient load performance. If the sensor supply leaves the module: special protection is suggested against overvoltage and a low-pass filter will reduce conducted emissions.	Leave open
VTRACK1	18	Analog	I	Tracking input reference for sensor-supply regulator (VSOUT1) (internal pulldown)	Sets the VSOUT1 voltage regulator tracking or non-tracking mode. For tracking mode connect to supply VSOUT1 should track. For non-tracking mode connect to ground.	Leave open
GND	19	GND	GND	Ground (Analog)	Low-impedance ground plane	N/A
VDD5	20	Power	PWR	VDD5 regulator output voltage	Minimum 1-µF effective output capacitance to ground as close as possible to pin (ceramic, voltage rating higher than VDD5). Higher output capacitance provides better stabilization and transient load performance.	N/A
VDD3/5	21	Power	PWR	VDD3/5 regulator output voltage	Minimum 1-µF effective output capacitance to ground as close as possible to pin (ceramic, voltage rating higher than VDD3/5). Higher output capacitance provides better stabilization and transient load performance.	N/A
VDDIO	22	Supply	PWR	I/O supply input for pins to and from the MCU	Minimum 0.1-µF capacitor to GND as close as possible to pin (ceramic, voltage rating higher than VDDIO). The supply connected to this pin sets the logic level of digital pins.	N/A
GND	23	GND	GND	Ground (Analog)	Low-impedance ground plane	N/A
VDD1_SENSE	24	Analog	I	Reference input for VDD1 regulator (feedback) and input for UV/OV monitoring of VDD1 regulator	Reference input for VDD1 regulator and input to VMON for VDD1 voltage monitoring. Connect to source of VDD1 external output NMOS transistor for 0.8-V VDD1 output voltage or voltage resistor divider from VDD1 to get higher VDD1 output voltage for example, 1.2 V. 0.1% or better resistor tolerance is recommended to minimize the impact from the resistors on the total tolerance of regulation and UV/OV monitoring for VDD1. VDD1_SENSE can be used to monitor another rail if VDD1 regulator is not used.	Leave open (if VDD1 is not used or VDD1_SENSE is not used to monitor a rail)
PGND	25	GND	GND	Ground (Power)	Low-impedance ground plane	N/A
VDD1_G	26	Analog	O	Gate drive of external FET for VDD1 regulator	VDD1 output transistor should be close to TPS65381x-Q1 to avoid noise injection into high-impedance gate line.	Leave open (if VDD1 is not used)
VDD6	27	Power	PWR	VDD6 switch-mode regulator feedback input and supply input for integrated VDD5 and VDD3/5 regulators	Minimum 22-µF effective capacitance with 100- to 300-mΩ controlled ESR to ground as close as possible to pin and inductor (ceramic with external series R, voltage rating higher than VDD6, or main supply if fault case must be considered). See the data sheet, application section, VDD6 preregulator for details on how to balance L, C, and R for VDD6. For high frequency filtering a 0.1-µF and a 0.01-µF capacitor can placed in parallel to the main output capacitor between VDD6 and ground. These filtering capacitors can be low-ESR ceramic capacitors while the main output capacitance should have controlled total ESR. If VDD6 will be used to power other downstream components directly, a zener clamp can be used such as ROHM UDZSTE-176.2B.	N/A
SDN6	28	Power	PWR	Switching node for VDD6 switch-mode regulator	Low-impedance trace as short as possible to inductor and diode. An RC snubber can be added at this node if necessary to reduce emissions.	N/A
VBATP	29	Supply	PWR	Battery (supply) voltage (must be reverse protected), main power supply input for device When below the minimum, the device does not start up and the NRES and ENDRV pins are low.	Main supply to the device. This supply must be reverse protected. Input capacitors are suggested from VBATP to ground including low capacitance values such as 0.1 µF and 0.01 µF to help reduce high frequency noise (ceramic, voltage rating higher than the main supply voltage). Bulk input capacitance could be in the 10 to 100 µF range depending on system loading. To reduce conducted and radiated emissions an input filter is recommended. The cutoff frequency should be ~ 1/10 of f_{SW} (switching frequency) or lower.	N/A

Table 1. Checklist by Device Pin (Applies to TPS65381-Q1 and TPS65381A-Q1) (continued)

Pin Name	Pin No.	Type	Signal	Description	External Circuit	If Not Used
IGN	30	Digital (HV)	I	Wake up input from ignition (key) or other source (internal pulldown, I_IGN)	The IGN pin has an integrated deglitch, so if it is connected to a low-noise wake-up signal, no special care is needed. However in the case that the IGN pin is connected outside the module, the following points should be considered: a series resistor of 10-kΩ or higher should be connected directly to the IGN pin to limit current in case of a failure, optionally a capacitor or RC filter can be used to filter incoming signals, a resistor divider or clamp may be required if the external signal has significant transients.(4)	Leave open(5)
SEL_VDD3/5	31	Digital	I	Input selects voltage level for VDD3/5 regulator (SEL_VDD3/5 pin open: 3.3-V regulation from VDD3/5, SEL_VDD3/5 pin GND: 5-V regulation from VDD3/5)	Leave open for VDD3/5 to operate in 3.3V mode, connect to GND for VDD3/5 to operate in 5V mode. The level on this pin is read at device power up from the STANDBY state and latched.	N/A
ENDRV	32	Digital	O	Enable output signal for peripherals (for example, motor-driver IC), safing path output (internal pullup, open drain output)	Check at system level if internal pullup, $R_{NRES\_ENDRV\_PULLUP}$, meets system requirements. Connect to the system functional-safety monitors and safing paths as needed by system requirements.	Leave open
Thermal pad		GND	GND	Place thermal vias to large ground plane and connect to GND and PGND pins.	Low-impedance GND plane	N/A

(4) Either IGN or CANWU must be used to wake up the device.

(5) Either IGN or CANWU must be used to wake up the device from the STANDBY state. Therefore, either CANWU or IGN may be un-used, but not both, the device requires at least one wake-up source to transition from the STANDBY state into the powered states.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2013) to A Revision	Page
• Added TPS65381A-Q1 information to checklist	1
• Added *References* section	1
• Added the *Checklists* section to provide additional general information for consideration when reviewing designs	3
• Changed the Checklist by device pin list descriptions to add clarity in the *Checklists* section	4

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