Application Report
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Adaptive (Dynamic) Voltage (Frequency) Scaling—Motivation and Implementation

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ABSTRACT

To optimize power-dissipation and reduce junction temperature while achieving processing performance goals, various approaches are used to scale supply voltages to a system on chip (SoC) that contains several processors.

This application report details the nomenclature, summarizes the parameters influencing power-dissipation, and describes the implementation of one method known as adaptive voltage scaling (AVS). This report also describes how an optimized a power-management integrated circuit (PMIC), such as the TPS659038-Q1 device, can be used to implement this AVS method.

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1 Why is AVS Required?

With higher integration and exponentially increasing demands for processing power and clock-rates, power-consumption and thermal performance of integrated circuits (ICs) can become a limiting factor for high performance processor systems. Aside from power-saving benefits, reducing the self-heating of the processor chip operating in high automotive temperature environments creates a need for optimizing power supply solutions. The AVS method is one approach to supply each individual processor domain on a SoC with just enough voltage so that each processor can deliver the required performance while minimizing power consumption per processor domain.

2 Definition and Nomenclature

Texas Instruments uses the term SmartReflex™ to describe the multi-level and multi-parameter power management approach described in this report. The following sections describe several of the more common functionalities and terms associated with SmartReflex and AVS.

2.1 Process Variation or Process Strength

Process variation, or process strength, is the variation in the attributes of integrated transistors when a semiconductor device is fabricated. This phenomenon occurs on all semiconductor devices from all manufacturers. This process is more relevant for smaller semiconductor technology nodes or geometries. The process variation can be loosely classified into the three following categories:

- **Weak:** A weak device provides the lowest acceptable frequency performance allowed at nominal voltages. Weak devices do not have the potential to run at higher frequencies beyond the specified nominal frequency. Weak devices typically consume less leakage power than others devices in the population distribution.
- **Nominal:** A nominal device operates at the midpoint or average frequency performance across the population of devices at nominal voltages. Nominal devices have average performance when compared to weak and strong devices.
- **Strong:** A strong device provides the highest performance across the population of devices. Strong devices have the potential to run at faster frequencies than are required at nominal voltages. Strong devices can operate at the minimum specified frequency at voltages lower than nominal voltage values. However, strong devices exhibit more leakage power consumption than weak and nominal devices, especially during high temperature conditions.

NOTE: Semiconductor device populations from all manufacturers will contain devices from all three process categories—weak, nominal, and strong.

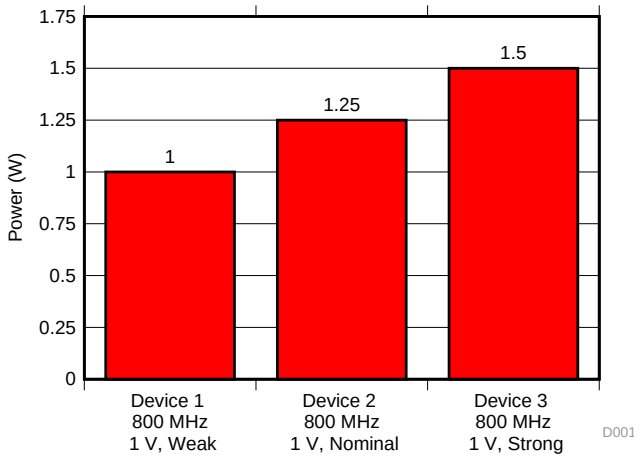


Figure 1. Power Consumption Versus Process Variations Example at a Fixed Temperature, Operating at Nominal Voltage

2.2 Adaptive Voltage Scaling

Adaptive voltage scaling (AVS) is the adaptation or modification of the supply voltage for a processor voltage-domain given the process strength. A processor from the strong category of the silicon process has high dynamic performance (a strong device can operate at a given frequency at a lower than nominal voltage), but it also has a higher leakage current which causes higher power dissipation when operated at a nominal voltage. Because of process variations, the supply voltage of each device can be adjusted to minimize power while still achieving desired performance. The resulting minimum supply voltage required for an individual device or IC, given the particular process strength of the IC, is programmed onto each IC. The PMIC can then read minimum supply voltage of each device and adjust the supply voltage level for optimal performance.

Power consumption is a concern in most systems. However, because of high ambient temperatures, power dissipation is a particular concern in automotive environments. Therefore AVS is frequently used, if not required, in automotive applications with high performance processors. The difference between the minimum supply voltages of weak silicon and strong silicon can result in supply current differences that range from several tens to hundreds of milli-amperes, resulting in a substantially better SoC thermal performance.

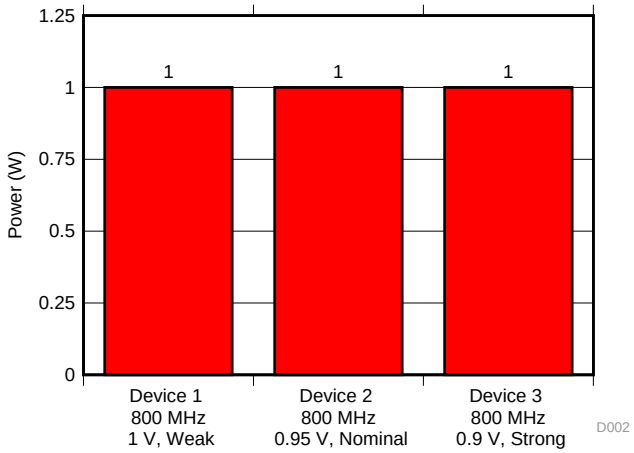


Figure 2. Example of AVS Normalization Effect Across Process Variation

AVS comes in different classes (see Section 4):

- Class 0
  - This class accounts for process variations. Temperature and aging should be factored into the voltage-margin.
- Class 1
  - This class accounts for process variations and aging. The device is calibrated and the voltage adjusted at boot. Because the temperature may change, temperature must be factored into the voltage-margin.
- Class 2
  - Software performs a self-check at intervals and accounts for process variations, temperature, and aging. During the self-check, only limited performance is available. No adoption of this class has been seen in automotive markets.
- Class 3
  - Hardware performs a self-check at intervals and accounts for process variations, temperature, and aging. During the self-check, only limited performance is available. No adoption of this class has been seen in automotive markets.

2.3 Voltage Domain

Voltage domain refers to a group of modules that share the same power supply voltage for the core logic of each device. Each voltage domain is powered externally by a dedicated power-supply voltage-rail interfaced to the device using the same terminals on the device package. Voltage domains can be independently adjusted using SmartReflex technology as a trade-off between power and performance. Examples of SoC voltage domains are VDD_MPU, VDD_DSPEVE, VDD_IVA, and VDD_GPU.

2.4 Operating Performance Point

The operating performance point (OPP), is the voltage specification for each voltage domain required to operate at a desired processor clocking frequency. The following table below shows an example of three different OPPs for one SoC voltage domain including nominal (OPP_NOM), over-drive (OPP_OD), and high-performance (OPP_HIGH).

DESCRIPTION	MAXIMUM FREQUENCY (MHz)		
	OPP_NOM	OPP_OD	OPP_HIGH
MPU_CLK	1000	1176	1500

2.5 Adaptive Body Bias

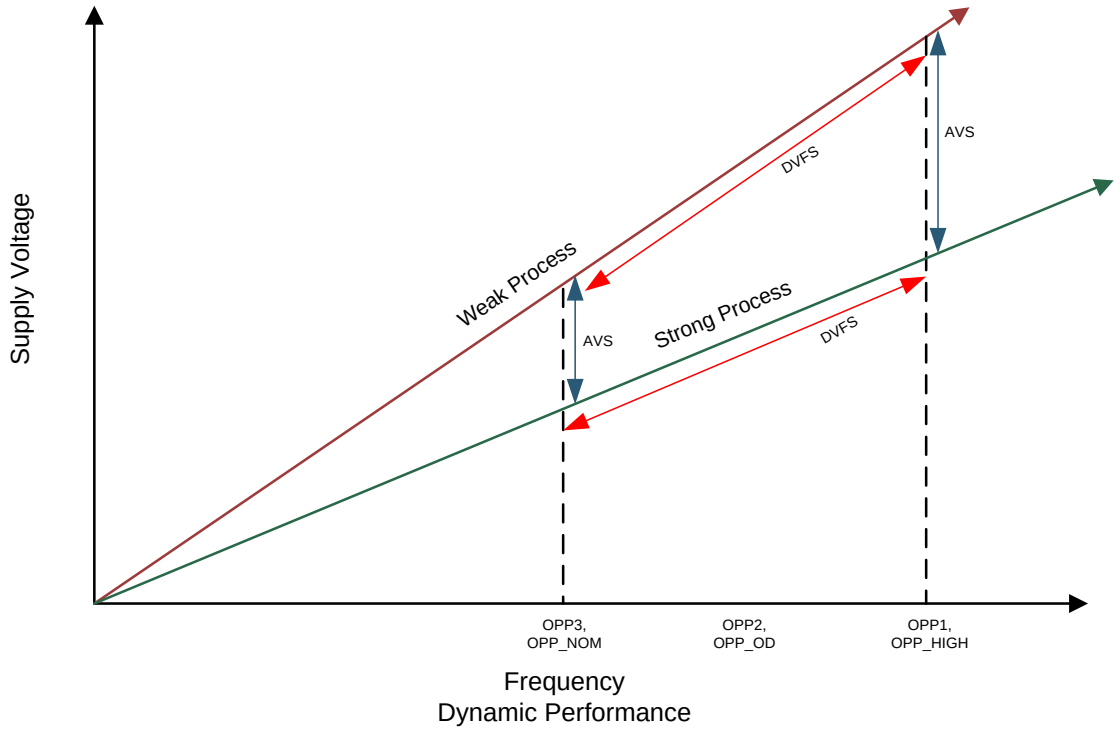
The adaptive body bias (ABB) is a feature that enables the body bias voltage of the transistor (also called NWELL voltage or VBBNW) to be adjusted in order to control transistor performance. The ABB LDO is located on the IC that supplies the body bias voltage. The ABB must be set and enabled while running at certain OPPs based on the characteristics of the device data stored on the device.

2.6 Dynamic Voltage Frequency Scaling

Dynamic voltage frequency scaling (DVFS) is the feature of the processor that allows software to change OPP (for example from OPP_NOM to OPP_OD) in real-time without requiring a reset. DVFS enables software to change SoC processing performance based upon the desired processing tasks to achieve the best performance or lowest power possible. DVFS is not typically found in automotive applications because of less emphasis on battery-life management and because of the many frequency combinations that require extensive EMI testing. The delta in supply voltage could exceed 200 mV.

NOTE: Dynamic Voltage Scaling (DVS) refers to a combination of both AVS and DVFS.

Figure 3 shows the difference between AVS and DVFS by demonstrating the shift in voltage to improve the power-dissipation because of process-variance as opposed to operating frequency.



DVFS adjust the supply voltage to the required level for a given operating point (OPP). **AVS** adjusts the supply voltage to the required level based on the process variation of the silicon.

Figure 3. Dynamic Voltage Frequency Scaling (DVFS) Versus Adaptive Voltage Scaling (AVS)

3 Parameters Influencing the Required Supply Voltage and Power-Dissipation

The following parameters influence the power-requirements of the processor and the peripherals of the processor:

- The use of AVS is essential to help lower power consumption, and therefore improve thermal performance in a system. Using AVS allows for the processor to operate at the lowest possible voltage for a given performance point.

  Example: A nominal or strong device is allowed to operate at a voltage below the nominal voltage level because the nominal voltage level listed in the device datasheet assumes a weak device.

- Selecting the correct OPP for a given performance limit. is imperative.

  Example: If the processor is required to operate at a maximum frequency of 1000 MHz, then OPP_NOM is a sufficient operating point to satisfy this requirement.

DESCRIPTION	MAXIMUM FREQUENCY (MHz)		
	OPP_NOM	OPP_OD	OPP_HIGH
MPU_CLK	1000	1176	1500

- The use of DVFS allows for power savings in a situation in which high performance is only required for a short period of time.

  Example: A complex algorithm or intensive graphic-processing tasks may require a processor in order to temporarily use a higher than nominal operating frequency. To support the faster switching, a higher supply voltage may be required. To support this on-demand, or dynamic, requirement, the power-supply must be programmable or adjustable to implement DVFS.

DOMAIN	CONDITION	OPP_NOM			OPP_OD			OPP_HIGH			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX DC	MAX
VDD_MPU	Boot (before AVS is enabled)	1.023 V	1.06 V	1.11 V	NA	NA	NA	NA	NA	NA	NA
	After AVS is enabled	AVS voltage – 3.5%	AVS voltage	1.11 V	AVS voltage – 3.5%	AVS voltage	AVS voltage + 5%	AVS voltage – 3.5%	AVS voltage	AVS voltage + 2%	AVS voltage + 5%

- The process variance and resulting process variation of the individual silicon.

  Example: Strong silicon is associated with high dynamic performance. However, this dynamic performance comes with an increase in power consumption. The more dynamic performance that a die has, the higher the leakage power. With ever-shrinking process nodes, the process variance is gaining importance.
- Process node or geometry

  Example: Smaller geometries lead to lower off-resistances and higher leakage currents. Some process nodes have higher leakage, some have high active power numbers. However, operating at the lowest voltage possible will always help reduce both leakage & active power.
- Gate count

  Example: The more complex and the more cores a processor supports, the higher the gate count and number of leakage paths.
- Required margins. Aging, temperature, load transients, and other effects affect the minimum required voltage. Depending on the implementation, the voltage margin should account for all possible effects or should be able to adjust for the effects dynamically (depending on the AVS class).

  Example: For AVS Class-0, a margin is built into the minimum supply voltage level programmed in the device to account for these additional margins (such as aging, temperature, and load transients).

One of the benefits of higher AVS-classes is the ability to adjust the voltages based on temperature changes and aging. This adjustment would be accomplished by a self-check in silicon, which translates to the device adjusting its own external voltage by using the I^2C or SPI bus.

4 Implementing AVS and DVFS

To support voltage scaling, both the processor and the power supply must be designed to support it. The processor must recognize unique voltage demands per domain (VDD_MPU, VDD_GPU, VDD_CORE, VDD_DSP, or others) per operating performance point (OPP_NOM, OPP_OD, or others). In case of different OPPs, each OPP will have a minimum voltage stored in a register. An I^2C interface is used for communication between the processor and the external power supply. An SPI or GPIO can be used for this communication as well. For Class 2 and Class 3 scaling, the required IP and hardware blocks for the self-calibration must implemented in the processor.

The general approach to implementing AVS or DVFS is to evaluate the performance characteristics of the processor on the automated test equipment (ATE) during standard production testing and to permanently store the voltage demand on the individual IC. The storage could be an EPROM, eFuse, or similar.

The power-supply must also be adjustable in order to change the output voltage on demand. The easiest implementation is with a PMIC that supports this change in output voltage. Typically **it** can be implemented by digital voltage control through the I^2C or SPI.

NOTE: Devices are associated with a specific companion PMIC. The companion PMIC has typically been validated, tested, and optimized to work with the particular processor. Processor-specific data manuals call out a specific PMIC as the only supported option because the recommended PDN and decoupling characteristics listed in the processor data manual are generated by simulating and testing the combination of the device and PMIC. Although customers are required to perform their own power integrity analysis, using discrete solutions or PMICs that were not design as companions for a given device is strongly discouraged for this reason.

A potential discrete power-supply design would require a resistor network in the feedback path, which is controlled through GPIO-controlled FETs. However, both the number of feasible voltage steps, as well as the tolerances of resistors, can easily negate the benefit of AVS. All of these variances should be added as a margin to the nominal voltage, as well as to the AVS-adjusted voltage. Cost and board-space for FETs and resistors, as well as the availability of GPIOs, are further limiting factors for a discrete solution. In the end, this solution is typically less desirable than no voltage scaling.

The power-supply is programmed to power up with the nominal voltage that the processor domain requires for the desired worst-case (weak silicon) boot-OPP. Voltage specifications for boot time are generally provided in the processor data sheet. After booting, the processor communicates the AVS-voltage per domain to the supply, which adjusts the output voltage accordingly. In case of a change of operating performance point (OPP), the processor notifies the supply of a change in supply voltage, then the supply sets the outputs to the nominal output voltages again, and finally lowers these voltages to the appropriate AVS-levels for the new OPP.

The TPS659038-Q1 and TPS659039-Q1 devices which are designed to supply Jacinto6, TDA2x, OMAP5, or other graphic-processors used in automotive systems for ADAS applications or infotainment applications, offer a total of up to seven buck-regulators, four of which support AVS. The supplies enabling AVS (or DVFS) have two voltage registers, one for the nominal voltage, which is used for booting, and an independent one used for AVS voltages or DVFS voltages. Figure 4 shows a simplified example configuration of a PMIC supplying a processor, such as of the Jacinto-6-family. MPU, GPU, IVA and DSP_EVE support various operating points, therefore AVS and DVFS may be required, while CORE has only one operating point and would therefore only require AVS.

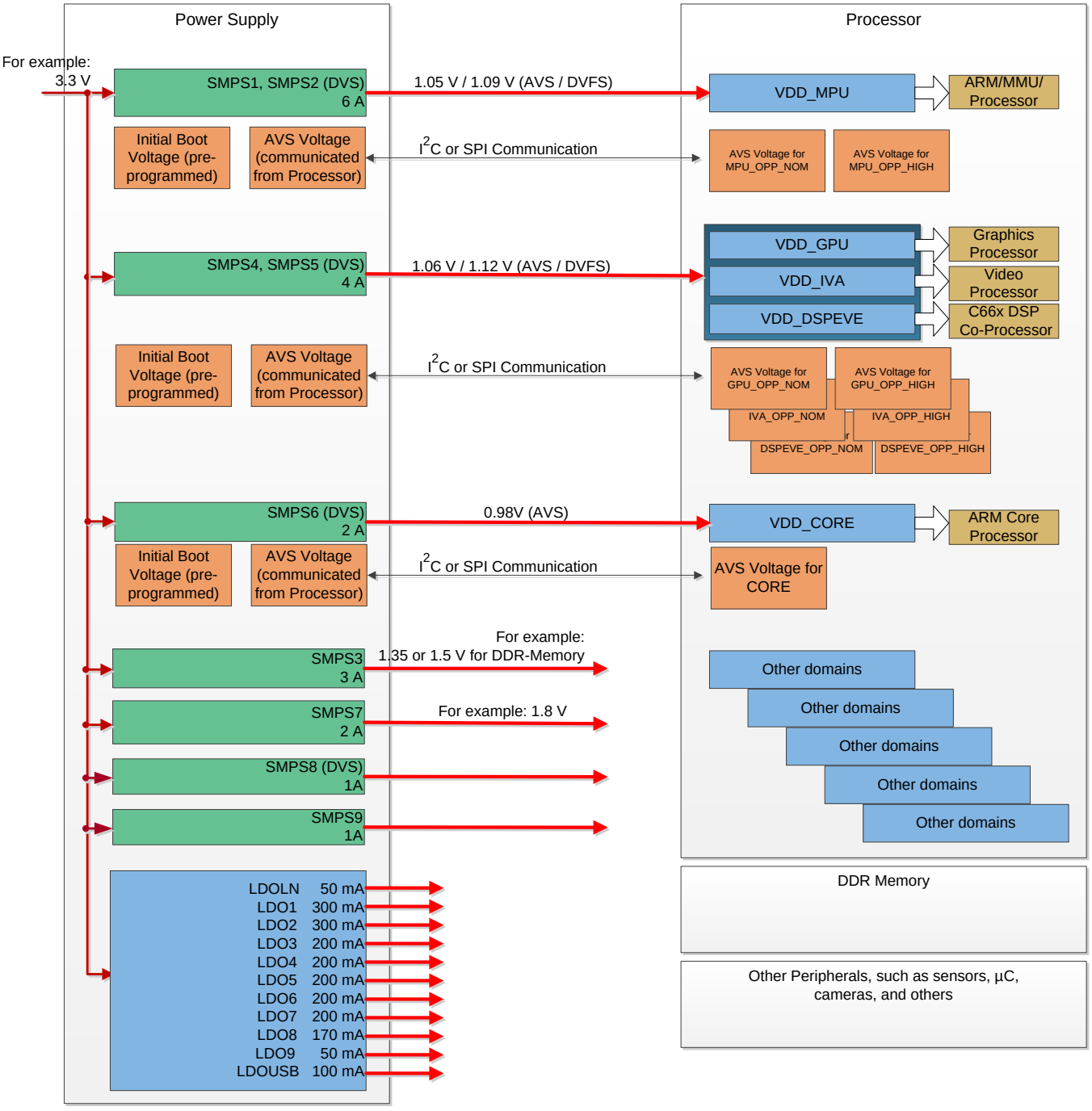


Figure 4. Example Implementation With the PMIC TPS659038-Q1

At power-up, each rail ramps up to the nominal voltage that iss set in the voltage register in the boot-sequence. After the processor is powered up, it reads its own AVS registers and commands the PMIC to lower the respective voltages (if applicable). The PMIC then changes the output-voltage to the new value with a predefined programmed slope until it gets a new voltage request, and is then powered down or a reset is applied. In case of a reset event, the nominal boot-voltage is read out of the boot-register and applied.

5 Conclusion

The adaptive voltage scaling (AVS) method is a powerful technique that supports the optimization of power-consumption for modern processors. To meet strict system requirements for the power dissipation of the processor, AVS may be required. In order to implement DVFS or AVS, both the processor and the power supply must be carefully designed for communication and regulation in order to account for the device operating point or process variation. Companion PMICs such as the TPS659038-Q1 and TPS659039-Q1 device are highly integrated devices that enable and simplify this function. Such specific companion PMICs are listed in the processor-specific data sheet as the supported option for PCB design.

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