Application Note

Capacitance Requirements for High Speed Signals

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ABSTRACT

This application note addresses the capacitive loads presented by electrostatic discharge (ESD) protection diodes to high-speed signals. With the industry trend towards smaller chipset sizes with higher data rates, the chipset's tolerance to transient voltages has decreased, increasing the need for ESD protection diodes. Higher data rates are very sensitive to parasitic capacitance, as a large capacitance can cause impedance mismatches. A large capacitance can distort the signal and cause the data to become corrupted or unreadable. For high speed signals, the ESD protection diodes need to have an ultra-low capacitance to not disrupt the signal transmission. With this dynamic, it becomes important to understand how much capacitance a high-speed signal can tolerate and still maintain proper signal integrity.

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Trademarks

1 Introduction

High-speed signals are typically routed by impedance matched transmission lines. This can be in the form of traces on a printed circuit board (PCB) or a cable connecting a source to a sink. ESD protection diodes are usually placed on a PCB very near to the connector where ESD is anticipated. The transmission line architecture of most high speed signals on a PCB is in the form of differential signal pairs. A simplified model of this is shown in Figure 1-1. Each unit length of the transmission line is comprised of an inductor, resistor, and capacitor. In an equivalent circuit with small enough unit lengths, the losses become negligible enough to consider only the inductance and capacitance as shown in Figure 1-2. The equation for the characteristic impedance, Z_0, then simply becomes:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{1}$$

The inductance in an ESD protection diode which is in series with the differential line is usually nonexistent (this is especially true for the device that has one protection pin for each protected line) while the parallel capacitance is somewhere on the order of 0.1 pF to 1 pF. This arrangement presents mostly capacitance to the node of the transmission line, so that the characteristic impedance becomes much lower at that point.

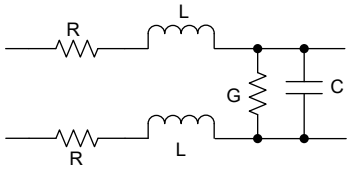

Figure 1-1. Segment of Two-Wire Transmission Line

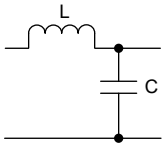

Figure 1-2. Equivalent Circuit for a Two-Wire Transmission Line

2 Why Impedance Mismatches Matter

Any mismatch in impedance at the node where the ESD protection diode connects to the transmission line has an impact on the signal integrity. The effect from a mismatch in impedance on a voltage-varying signal propagating down a transmission line is to reflect back some voltage towards the source, of which some voltage can then reflect back again if there is another change in impedance. This back and forth reflection continues through the line wherever there are any impedance mismatches. Depending on the distance between the impedance mismatches, the signal may be attenuated or amplified due to any part of the signal that has been reflected back and forth being added to the signal propagating down the line. If the impedance mismatches are big enough, then these reflections can change the voltage levels of the signal outside of the receivers input logic levels, leading to a loss of data.

Some industry specifications stipulate how much total parasitic capacitance a source or a sink can have, not including what resides in the receiver chipset. For USB 3.1 Gen 1 this is 1.25 pF for a source and for Gen 2 it is 1.1 pF. Other industry specifications do not specify the capacitance by value, but rather by the impact on the characteristic impedance of the transmission line when measured by a time domain reflectometer (TDR) using a specified rise-time. The HDMI 2.0 specification stipulates no single excursion beyond 100 Ω ±25% for a duration of 250 ps when measured with a TDR rise-time of less 200 ps. Impedance for some Texas Instruments ESD diodes are shown in Figure 2-2 and Figure 2-3.

Controlling the impedance in a transmission line is paramount to maintaining good signal integrity. One of the most useful tools for verifying good signal integrity is the data eye diagram. The data eye diagram is comprised of every unit interval in a multi-bit pseudo-random bit sequence (PRBS) signal superimposed on one another. Figure 2-1 show six example transitions mapped by the eye diagram.

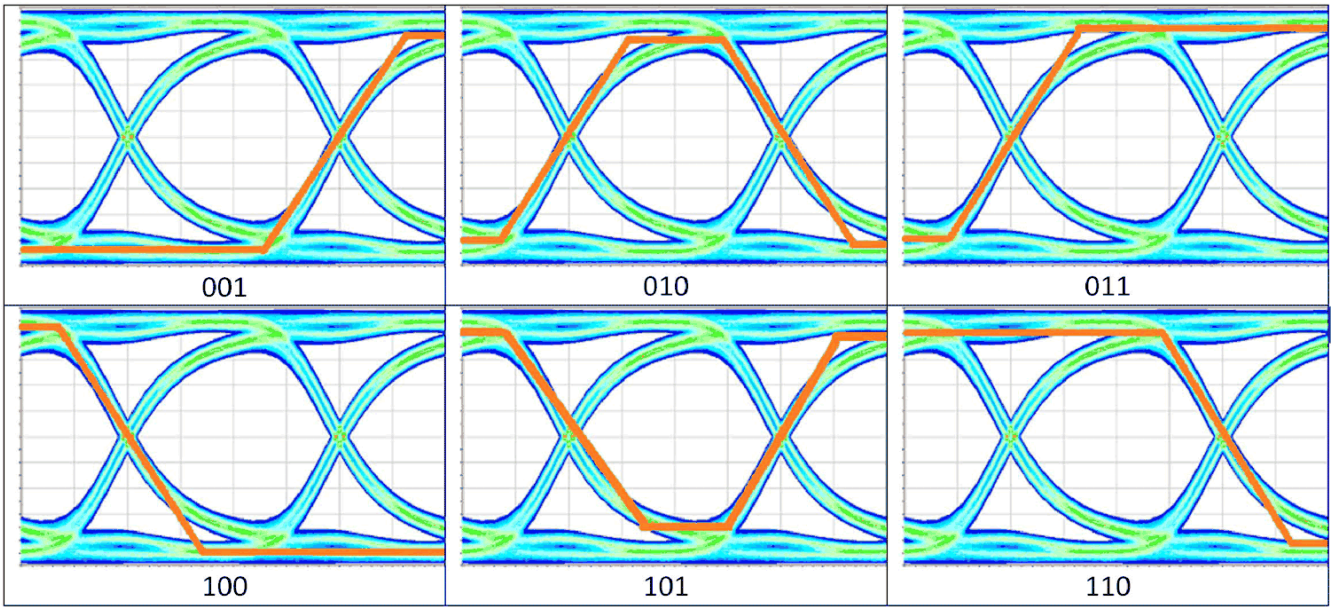

Figure 2-1. Binary Code in an Eye Diagram

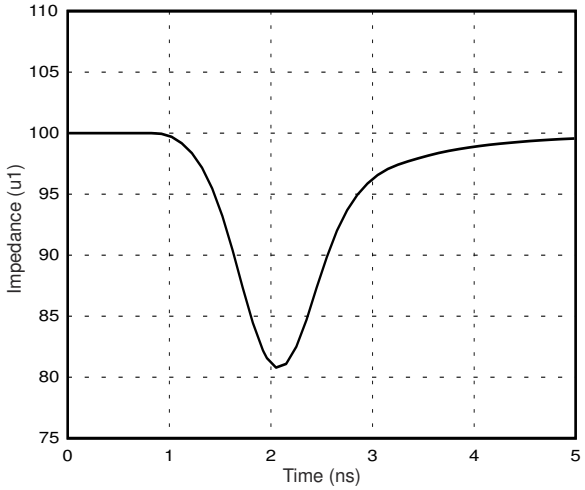

Figure 2-2. Impedance of TPD1E04U04DPY from 192-ps Rise-Time TDR

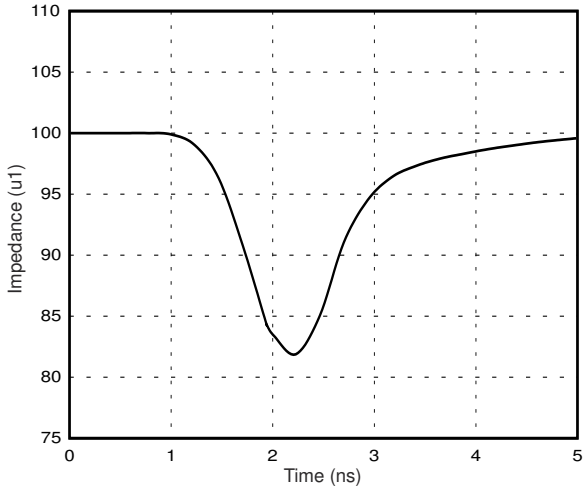

Figure 2-3. Impedance of TPD4E02B04DQA from 192-ps Rise-Time TDR

3 USB 3.0 Gen 1

Figure 3-1 shows a full-channel USB 3.1 Gen 1 compliant model without the addition of an ESD protection diode. The resultant eye diagram can be seen in Figure 3-2. Figure 3-3 shows the eye diagram for the same circuit utilizing the TPD4E02B04 ESD protection diode by Texas Instruments at the source connector. The schematic model is shown in Figure 3-4.

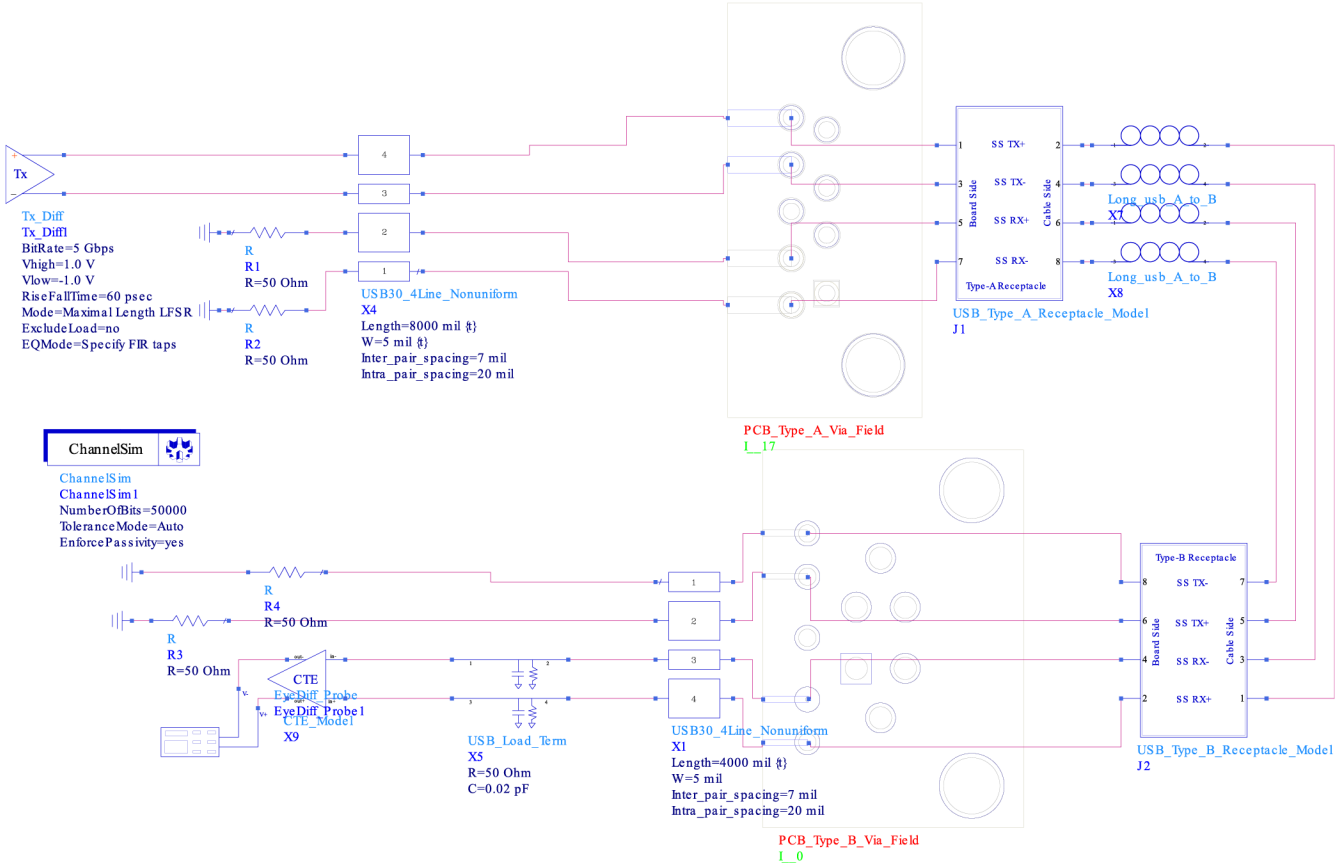

Figure 3-1. USB 3.0 Gen 1 Full-Compliance Schematic without ESD Protection

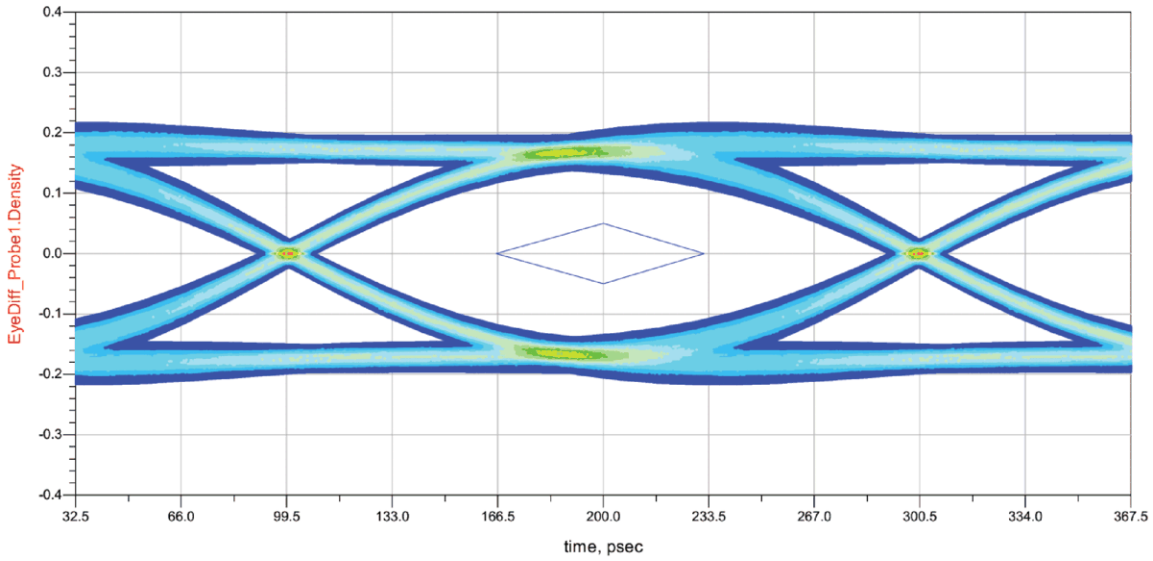

Figure 3-2. USB 3.0 Gen 1 Eye Diagram without ESD Protection

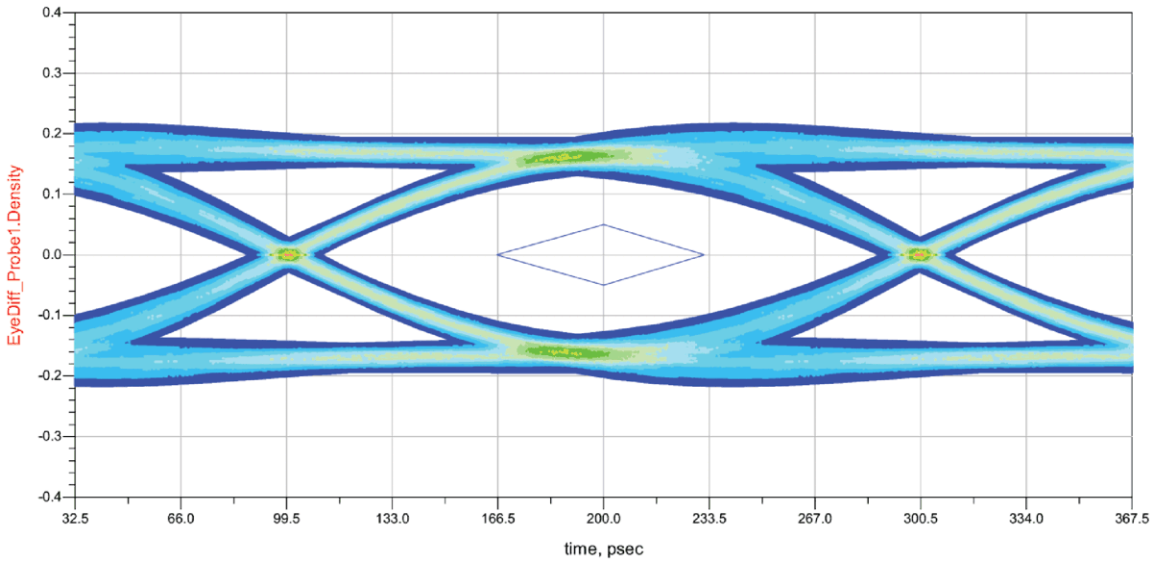

Figure 3-3. USB 3.0 Gen 1 Eye Diagram with TPD4E02B04DQA ESD Protection

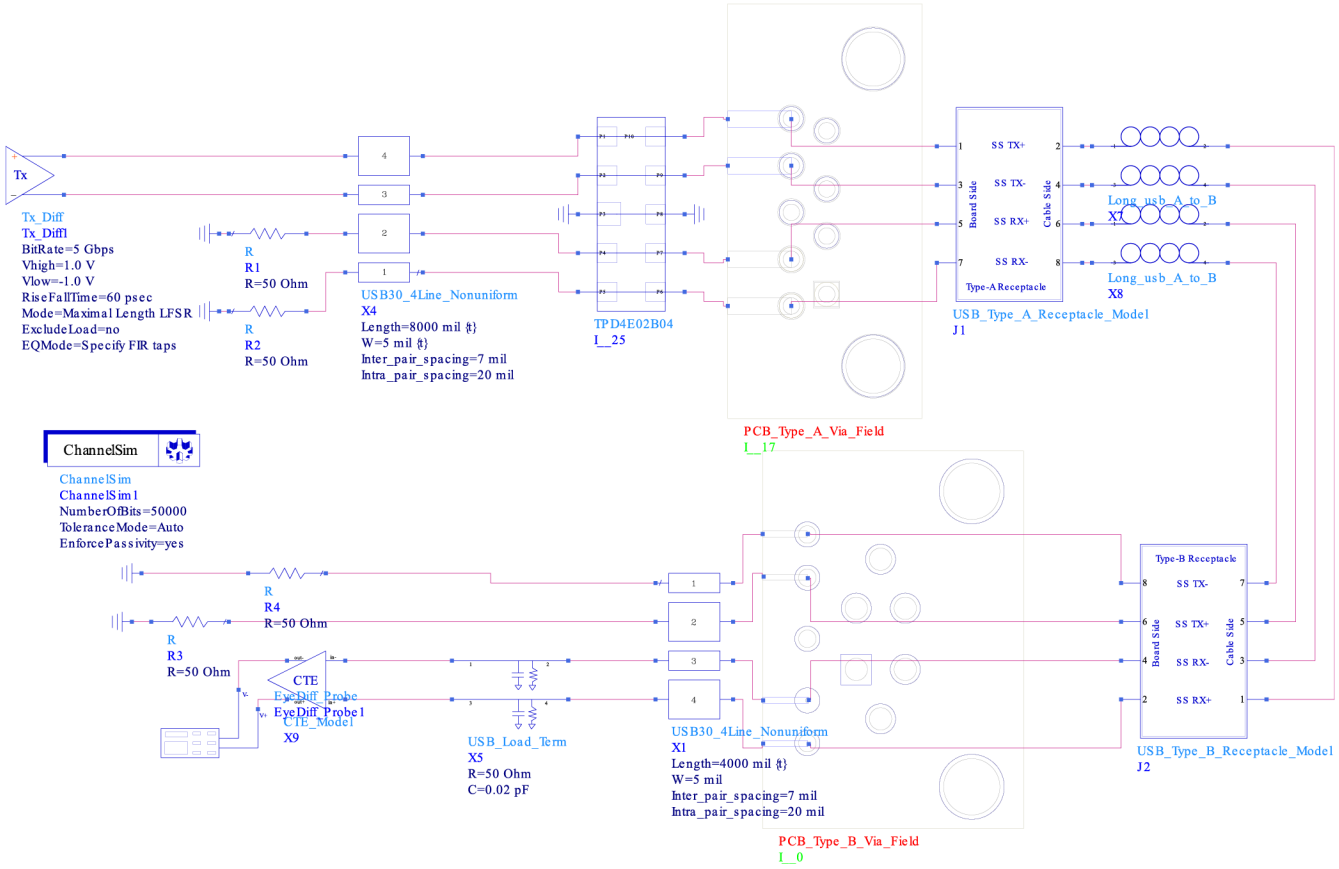

Figure 3-4. USB 3.0 Gen 1 Full-Compliance Schematic with ESD Protection

Table 3-1 shows the eye diagram measurements with and without ESD protection:

Table 3-1. Eye Diagram Measurements with and without ESD Protection

	No ESD Protection	TPD4E02B04	Change
Rise Time	81.96 ps	86.18 ps	+4.22 ps
Fall Time	81.89 ps	86.11 ps	+4.22 ps
Eye Height	266 mV	243 mV	–23 mV
Eye Width	182.8 ps	177.7 ps	–5.1 ps
Jitter(PP)	17.2 ps	22.8 ps	+5.6 ps
Jitter(RMS)	2.969 ps	3.836 ps	+0.867 ps

The additional capacitance of an ESD protection diode has an impact on rise and fall-times by slowing them down. This negatively impacts the rest of the table values as well. However, the low-capacitance of TPD4E02B04 only minimally impacts the eye diagram, making it an excellent choice for ESD protection in a USB 3.0 Gen 1 system. TPD4E02B04 is also successful in a USB 3.1 Gen 2 application.

4 USB 3.1 Gen 2

While USB 3.1 Gen 1 supports a data rate of 10 Gbps and requires the ESD protection diode capacitance to be <0.5pF, USB 3.1 Gen 2 supports a data rate of 20 Gbps and requires the ESD protection diode capacitance to be <0.3pF. Figure 4-1, Figure 4-2 and Figure 4-3 map out the data eye without an ESD protection diode, with the TPD4E02B04 protection diode, and with a 0.5-pF protection diode.

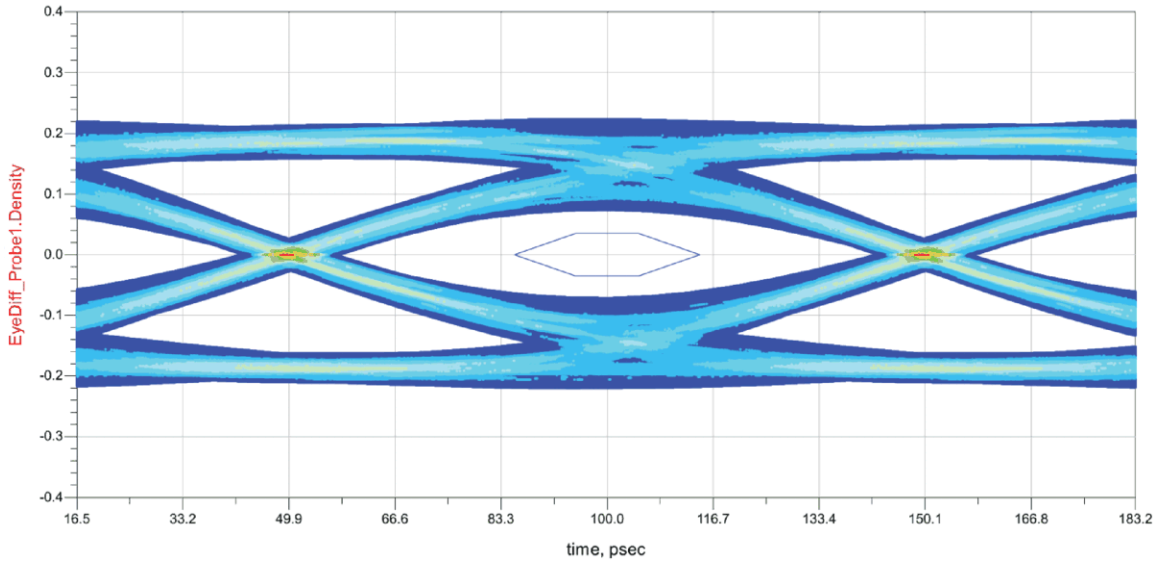

Figure 4-1. USB 3.1 Gen 2 Eye Diagram without ESD Protection

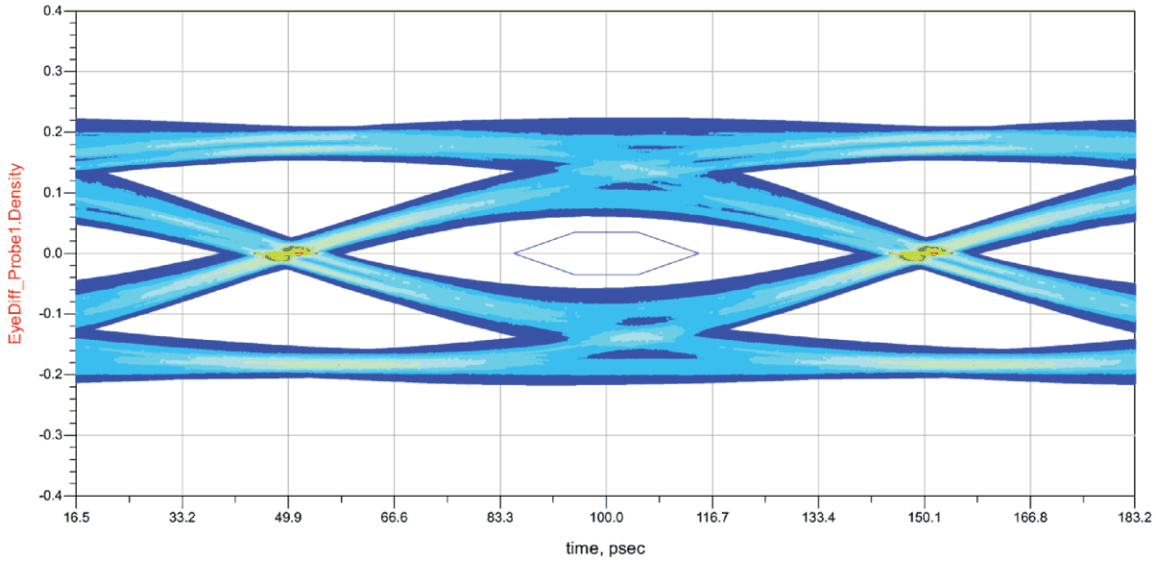

Figure 4-2. USB 3.1 Gen 2 Eye Diagram with TPD4E02B04DQA ESD Protection

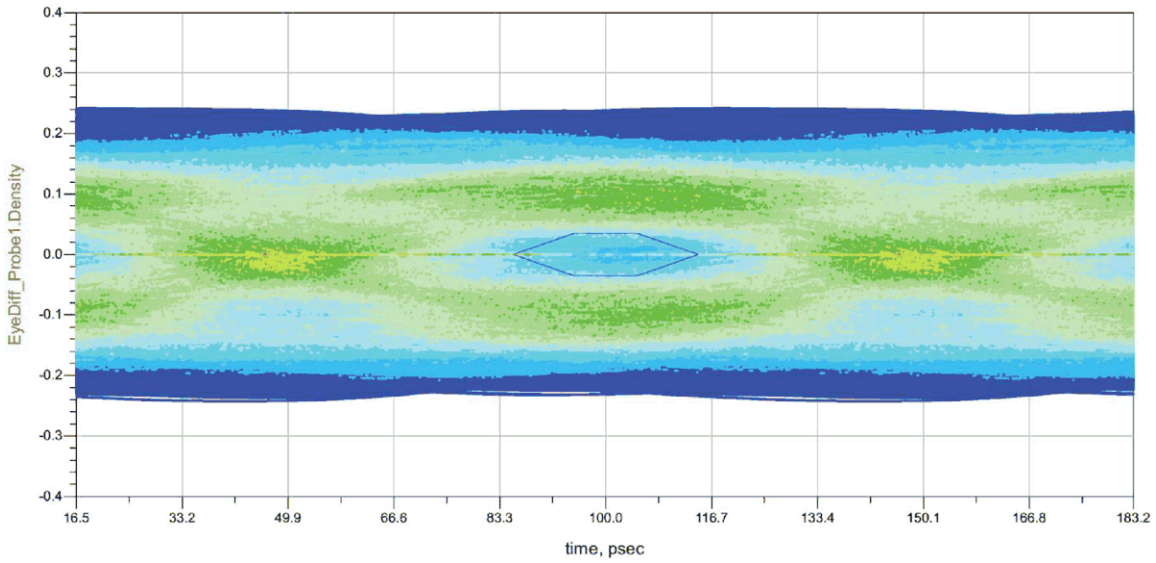

Figure 4-3. USB 3.1 Gen 2 Eye Diagram with 0.5-pF ESD Protection

Table 4-1 lists the eye diagram measurements with and without ESD protection.

Table 4-1. Eye Diagram Measurements with and without ESD Protection

	No ESD Protection	TPD4E02B04	0.5-pF ESD Protection
Rise Time	63.55 ps	67.11 ps	NA
Fall Time	63.77 ps	66.15 ps	NA
Eye Height	132.3 mV	112 mV	NA
Eye Width	84 ps	81.93 ps	NA
Jitter(PP)	15.6 ps	18.07 ps	NA
Jitter(RMS)	2.725 ps	3.167 ps	NA

The 20-Gbps signal is still able to maintain signal integrity with the low capacitance of the TPD4E02B04 while providing ESD protection for the Gen 2 USB 3.1 transmitter. When using an ESD protection diode with a capacitance of 0.5 pF, the results show an eye diagram that does not have distinct data. This visualizes the effect of high capacitance on a high speed data signal.

Various PCB designs have many different specification needs. Listed below are some additional devices to TPD4E02B04 that meet the ultra-low capacitance needs of high-speed signals while utilizing less PCB space. Even more devices can be found online with the *Product Selection Tool*. These devices come with a variety of channel coverages, package sizes, Bi/uni directional capabilities, surge ratings, and clamping voltages.

Table 4-2. ESD Protection Device Quick Select

	TPD4E02B04	TPD1E01B04	TPD1E05U06
Vrwm (V)	3.6	3.6	5.5
Package Type	USON	DPL, DPY	SOT-5X3,DPL
Package Size (L x W) (mm)	2.5x 1	0.6x 0.3, 1.0 x 0.6	1.6x0.8, 1.0x0.6
Bi-/uni-directional	Bi-directional	Bi-directional	Uni-directional
Number of Channels	4	1	1
Clamping Voltage	6.6	7.0	18
IO Capacitance (typ) (pF)	0.25	0.18	0.4
IEC61000-4-5 (A)	2.0	2.5	2.5
IEC61000-4-2 contact (±kV)	12	15	12

5 Summary

Today's high-speed signals push the envelope of technology. Texas Instruments ESD protection devices help the system-level designer keep pace while providing IEC 61000-4-2 Level 4 ESD protection. With a large family of ultra-low capacitance ESD protection diodes designed to be easy to layout on PCB, Texas Instruments offers the correct ESD protection for a wide range of applications up to 20 Gbps.

6 References

- Texas Instruments, *Reading and Understanding an ESD Protection Data sheet*, application note.
- Texas Instruments, *ESD Protection Layout Guide*, application note.
- Texas Instruments, *TI ESD Protection and the HDMI CTS*, application note.

7 Revision History

Changes from Revision * (July 2016) to Revision A (August 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated publication for technical clarity	1

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