Application Report
SLVA830–October 2016

Electric Power Steering Design Guide With DRV3205-Q1

ABSTRACT

This document introduces the DRV3205-Q1 motor-driver solution and describes how to design this device into an electric power-steering system using the advantage of all the diagnosis and protection features.

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1 Introduction

The automotive market is ever evolving and always looking for more protections and diagnostics with reliable and space-saving solutions in safety-critical market niches, such as electric power steering (EPS) and electronic braking systems (EBS). Electric power steering and powertrain markets analyses reveal the need for new motor driver concepts with added functionalities, such as enhanced fault diagnosis and protection features that require constant monitoring of the system behavior. Texas Instruments' DRV3000 product family is a family of brushed and brushless DC motor drivers that have unique performance requirements, and that were designed and developed specifically for supporting the development of automotive applications. Diagnostic and protection capabilities are standard features of the DRV3000 family, such as supply overvoltage detection, motor current-sense amplifiers, and motor overcurrent detection that can be fulfilled under the space constraining and harsh conditions that the automotive environment produces: high temperature, low-voltage start-stop, and cold-cranking.

This design guide introduces the DRV3205-Q1 motor driver solution and explains how to design the device into an EPS system to take advantage of all the diagnosis and protection features. The guide is not part of the semiconductor device specifications. Refer to *DRV3205-Q1 Three-Phase Automotive Gate Driver With Three Integrated Current Shunt Amplifiers and Enhanced Protection, Diagnostics, and Monitoring* (SLVSCV1) for a more detailed explanation of the functionalities and specifications of the device. To help customers achieve functional safety goals, go to www.ti.com or contact a local TI representative for safety manuals and safety analysis documents.

2 Electric Power Steering (EPS)

This section describes one of the most commonly used automotive-critical motor applications, electric power steering (EPS), and describes how to build an EPS system using the DRV3205-Q1.

2.1 Definition

Electric power steering uses an electric motor to assist steering a vehicle when the driver turns the steering wheel which is a replacement of the traditional mechanical and hydraulic system. The benefits of an EPS system are less CO_2 emissions, higher fuel efficiency, quicker operation, and enhanced user experience.

The main components of an EPS system are the steering column, an electronically controlled steering motor, and an electronic sense-and-control mechanism. The inputs of the system are provided by the driver at the steering wheel interface. Torque sensors are responsible for detecting the movement (direction, speed, and angle) of the steering wheel and for sending this data to a microcontroller. The data is processed and a signal is sent to the motor driver to assist the driver with steering the wheel. This motor can be driven by the DRV3205-Q1 device which generates the current-assist torque in response to driver demands.

2.2 Failure Modes

Failures in the EPS system that could lead to severe potential effects are loss of torque control and unintended motor torque. These failures are defined as follows:

Loss of torque control — During this failure, the EPS system is unable to assist in steering the vehicle possibly because of a short or an open circuit in the motor coil, a damaged motor driver, or failures in the microcontroller.

Unintended motor torque — During this failure, either the EPS system steers without input from the driver or the assisted torque is significantly deviated from driver's demand. This failure can be caused by a browned-out MCU, failures in the digital logic, and other causes.

These two failures can have unwanted consequences because of the very short reaction time that the driver needs to respond to the failure. Additionally, because the driver is constantly using the steering wheel during driving, the driver is exposed to the possibility of these failures occurring at any time. Because of this, the EPS design requires components which feature sophisticated protection, monitoring, and diagnostics.

The electrical parts of the EPS systems that require a high level of monitoring and diagnostics are:

- Electronic control unit that controls the EPS system
- Motor that generates assisted torque
- Current sensors that monitor the motor phase current
- Power supply and battery that supply all components of the EPS system
- Communication interface between the EPS system and other control units
- Sensors that read the input signals (torque and angle) and provide them to motor driver

2.3 System Architecture

The electrical part of an EPS system consists of a main microcontroller, power supply, motor driver, and power transistors for operating the motor. Additionally, CAN or Flexray communication is used to interface with the control units in the vehicle. Motor position and speed are typically controlled with an encoder or resolver. Torque is controlled through voltage or current feedback from the power stage of the motor.

A common architecture in an EPS system includes a gate driver with integrated diagnostics and monitoring as shown in Figure 1. In this case, the DRV3205-Q1 device directly provides much of the safety related tasks in the system, and can help protect against failures in the MCU and power supply. The device includes individual supply monitors for each of the voltage rails (I/O and analog reference supplies). The device also monitors the health of the MCU using an integrated watchdog timer. The MCU is often programmed with secure communication links and driver diagnostic software to help ensure that the system is checked on power-up. Latent fault detection is included in the systems by injecting faults internally by the DRV3205-Q1 device. Because the gate driver is the final block before the power FETs, this architecture provides a localized shutdown integrated with the monitoring and diagnostics.

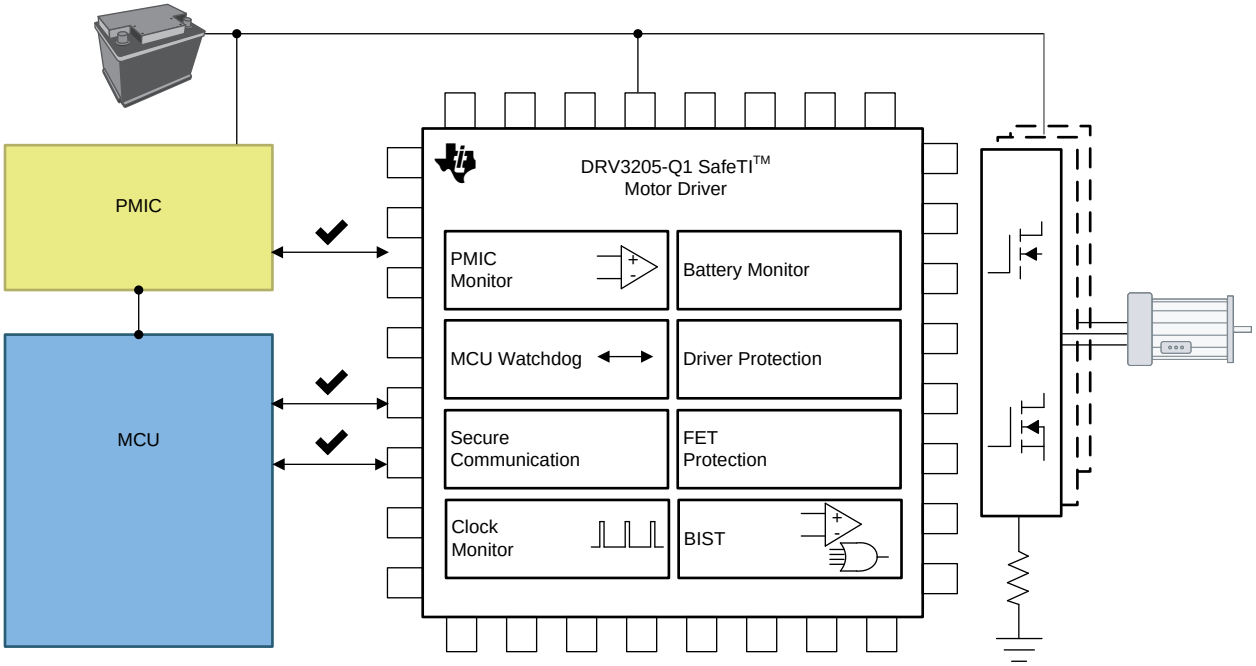


Figure 1. System Architecture

To increase redundancy in this type of architecture, the DRV3205-Q1 device has several companion devices which include similar sets of monitoring and diagnostic features. For example, Texas Instrument's TPS65381A-Q1 multi-rail power supply and TMS570 series MCU can be used to monitor each other and themselves as shown in Figure 1. In this fashion, each device serves to monitor and protect the system by providing redundancy. This redundancy eliminates the need for additional on-board monitors and can simplify the design complexity.

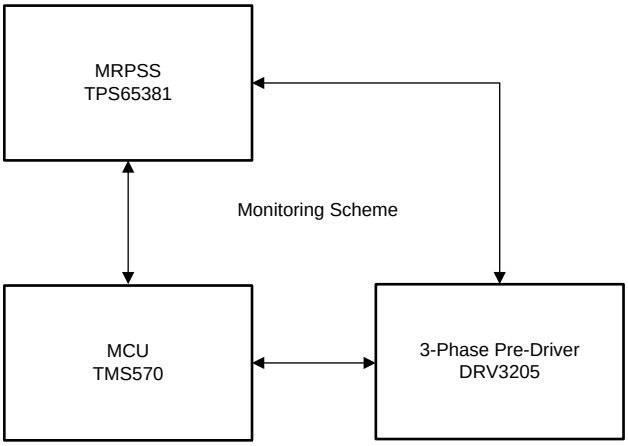


Figure 2. Redundant Monitoring Scheme

3 How to Design an EPS System With DRV3205-Q1

3.1 Introduction to DRV3205-Q1

This section is a brief overview of TI's DRV3205-Q1 device. For additional information, refer to *DRV3205-Q1 Three-Phase Automotive Gate Driver With Three Integrated Current Shunt Amplifiers and Enhanced Protection, Diagnostics, and Monitoring* (SLVSCV1).

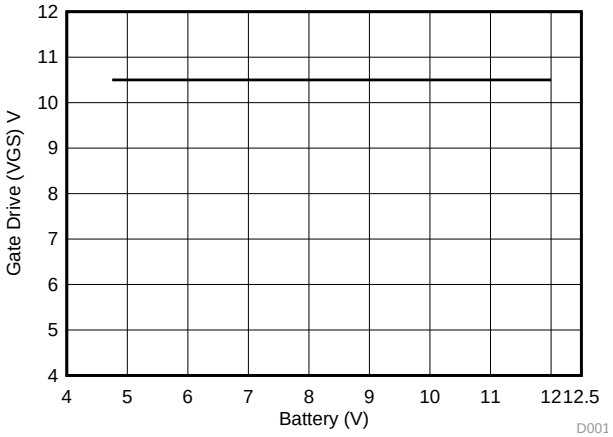
The DRV3205-Q1 device is a 4.75-V to 45-V automotive gate-driver device for three-phase motor-driver applications. This device reduces the external component count in the system by integrating three high-accuracy and temperature-compensated half-bridge drivers, a boost converter, three bidirectional current-shunt amplifiers, and several types of protection and monitoring circuits. The DRV3205-Q1 device provides application-level protection including overcurrent, shoot-through, and overtemperature protection. The device also includes monitoring circuits for the internal clock, undervoltage and overvoltage of the supply, the boost regulator, the I/O supply, and the analog reference supply, a watchdog monitor for MCU, and VDS and VGS monitors for the external MOSFETs. To verify the integrity of these monitors, the DRV3205-Q1 device implements built-in self-test (BIST) functionality which is run during system diagnostics to provide latent fault detection.

Fault conditions are indicated by the ERR pin and specific fault information can be read back from the SPI registers. The protection circuits are highly configurable to allow adaptation to different applications and support limp home operation.

The gate driver uses a boost converter to generate the appropriate gate to source voltage bias for the high-side N-channel MOSFETs during low supply conditions, as shown in Figure 3. The ability to operate the motor down to 4.75 V is very important for start-stop and cold-crank where the application must keep running through the crank. The boost converter provides a voltage in addition to the supply to power the full gate-to-source-voltage bias for the low-side N-channel MOSFETs. The high-side and low-side peak gate-drive currents are adjustable through the SPI registers to finely tune the switching of the external MOSFETs without the use of external components, as shown in Figure 4.

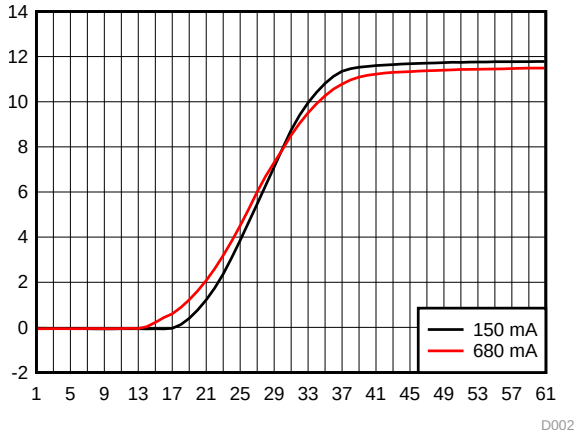
The VDS and VGS sensing of the external power MOSFETs allows for the DRV3205-Q1 device to detect motor short-to-ground and short-to-battery conditions and respond appropriately. Integrated masking and deglitch timers are provided to prevent false trips related to switching or transient noise. Individual MOSFET overcurrent conditions can be monitored directly using the sense resistors of each phase, with a tunable threshold. Each one of these faults is reported through SPI status registers and the ERR pin. A dedicated VSH pin is provided to accurately sense the drain voltage of the high-side MOSFET.

Three internal current shunt amplifiers allow for the implementation of common motor-control schemes that require sensing of the half-bridge currents. To reduce possible torque ripple on the system, the DRV3205-Q1 device implements high accuracy and lower error differential amplifiers with low offset and low drift over temperature. The amplifier gain and reference voltage is adjustable through the SPI registers.



Six FETs switching, 100% duty cycle, Q_{FT} = 42 nC

Figure 3. Battery Voltage vs VGS Showing the Operation of the Gate Driver at Low Supply Voltage



Six FETs switching, 100% duty cycle, Q_{FT} = 42 nC

Figure 4. Scope Plot Showing Slew Rate (VDS) Control Through SPI to Optimize EMI and Switching Losses

3.2 Block Diagram of an EPS System With DRV3205-Q1

Figure 5 shows a block diagram of an EPS system using the DRV3205-Q1 device.

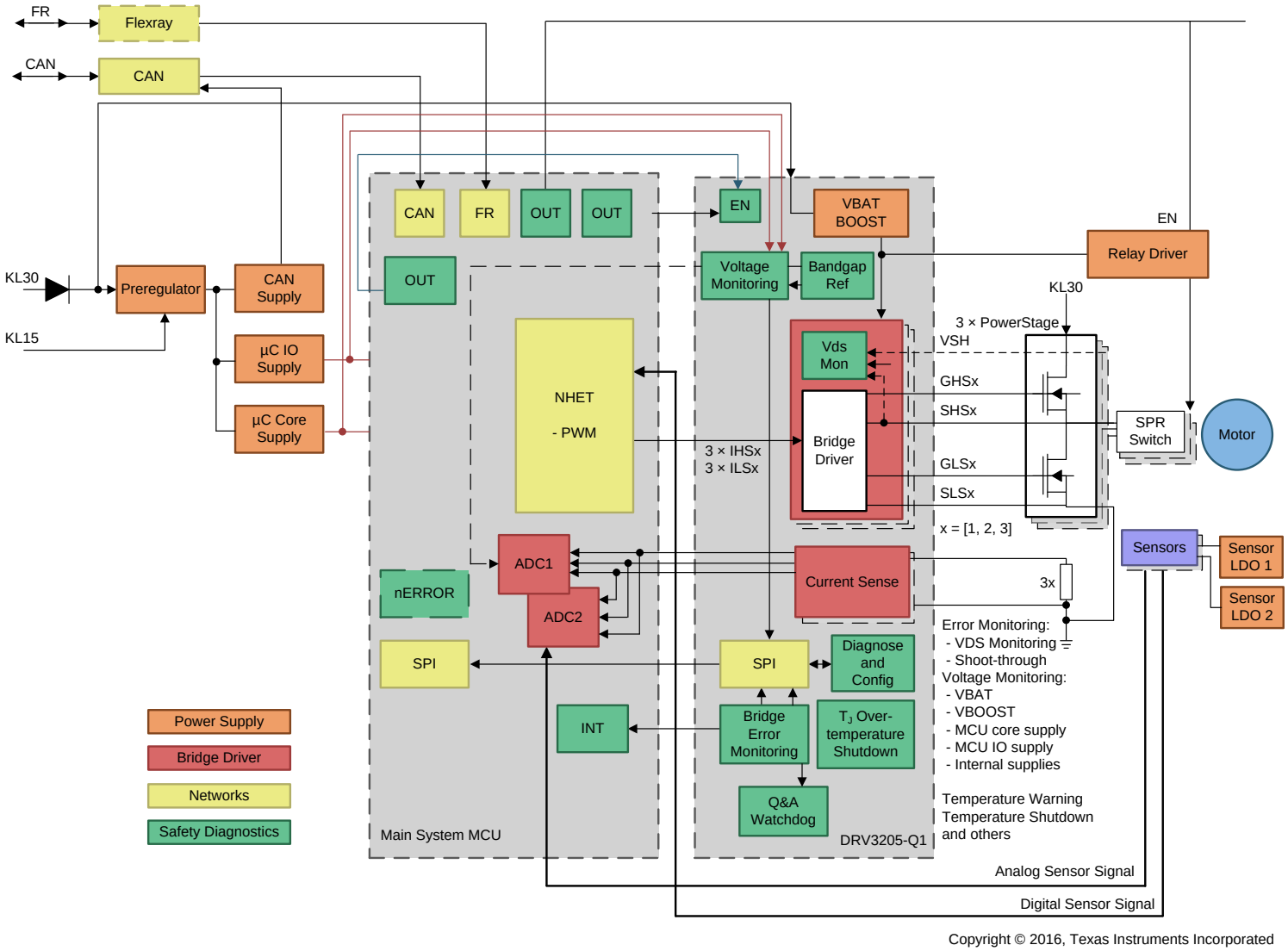


Figure 5. Block Diagram of an EPS System With DRV3205-Q1

3.3 Protection Features of DRV3205-Q1

The DRV3205-Q1 architecture includes many protection and diagnostic mechanisms that detect and respond effectively to failures when used correctly. These protections and diagnostic mechanisms are listed as follows:

- VDS sensing circuitry to prevent the external FETs from damage because of high currents and protect the system from ground and battery shorts on the motor leads
- Analog and digital monitors to prevent shoot-through in external FETs
- Three high-accuracy, low-side current-sense amplifiers with programmable gain to monitor the current flowing through each phase
- Low-side shunt resistor monitoring to prevent high-current events
- Redundant clock monitors to prevent logic failure
- Overvoltage and undervoltage monitoring and protection of MCU logic and analog supplies
- Battery undervoltage and overvoltage protection
- Overtemperature warning and protection
- Multilevel protection scheme to protect external MOSFETs from high VGS voltages
- A comparator that compares the output of gate drivers with the PWM commanded signal to confirm that they match
- Reverse battery protection support
- Watchdog that monitors the external MCU and helps confirm the correct active state
- Secure SPI communication to prevent configuration errors
- Configuration monitors to prevent internal register corruption

These modules communicate with an external MCU through a SPI that provides detailed fault reporting, diagnostics, and device configurations. The DRV3205-Q1 device classifies errors into two categories and acts differently depending on this classification.

3.4 Implementation of Protection Features in EPS Systems With DRV3205-Q1

The two severe potential effects of failures in EPS systems, loss of torque control and unintended motor torque, are explained in Section 2.2. Table 1 lists and Figure 6 shows the different possible scenarios that increment the risk of these failures and show how to detect these scenarios using the protection features of the DRV3205-Q1 device mentioned in Section 3.3.

Table 1. Implementation of Protection Features of DRV3205-Q1 to Detect Hazards in EPS Systems

System-Level Protection Features of DRV3205-Q1		Possible System-Level Failures Detected by DRV3205-Q1	Potential effects of failure in motor control application (for example EPS application)	Block Diagram (Figure 6)
Power supply (VS) undervoltage warning, undervoltage lockout, and overvoltage protection		Battery supply does not provide target voltage to the DRV3205-Q1 device	Loss of torque control	F1
Assisting reverse supply protection		Current flows back to the battery supply	Reverse battery condition	F2
MCU Watchdog and Secure Communication via SPI CRC		Failure in the MCU timer	Unintended motor torque	F3
		SPI does not transmit or receive the data to or from system MCU		F4
		Failure in MCU SPI logic		
		Open and short faults on serial interface		
VDDIO and ADREF under/over voltage protection		Failure of external components supplied by VREG	Unintended motor torque	F6
			Loss of torque control	
Power FET gate-drive protection:	VGS Monitors	Gates are shorted to ground or to supply	Unintended motor torque	F7
		Outputs of the gate driver mismatch the digital inputs		
	TDRIVE state machine	Gate voltage exceeds source voltage by a value that could damage power FETs	Loss of torque control	
	VDS monitors	Overcurrent events in power FETs	Unintended motor torque	F5
		Open or short failure modes of power FETs (drain-source)		
Power FET shoot-through protection		Low-side and high-side inputs of the gate driver are in the on-state at the same time	Loss of torque control	F8
		Failure in MCU PWM logic		
Low-side source monitors		Short circuit in the power FETs	Loss of torque control	F5
		Short on motor terminal		F9
Current shunt amplifiers (with plausibility check by MCU)		Short or open circuit in the external Power FETs, damaged power FETs, or short or open circuit in the motor coil cause high current events	Loss of torque control	F10

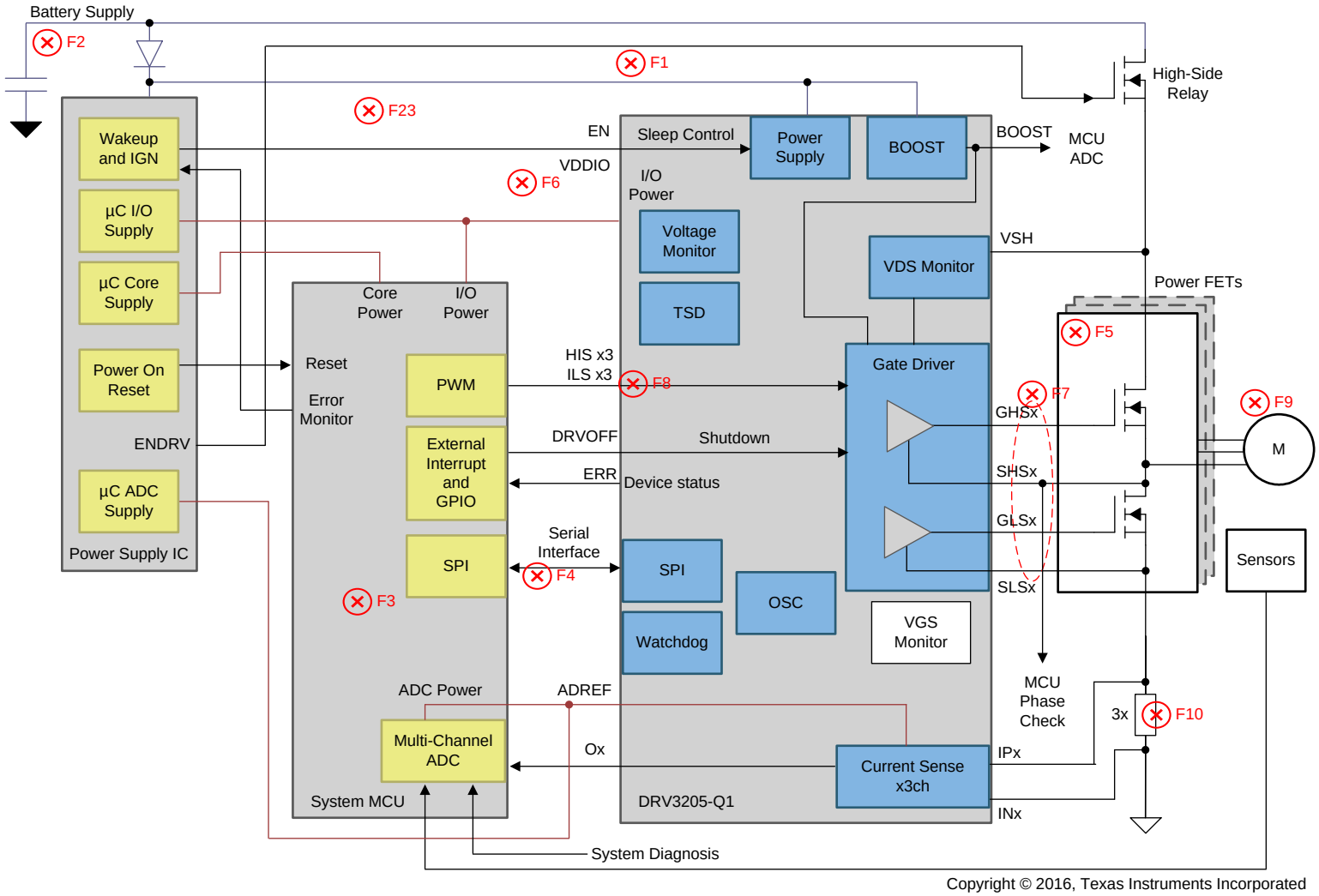


Figure 6. Possible System-Level Failures of an EPS System With DRV3205-Q1

3.5 Description of Protection Features of DRV3205-Q1

This section provides a detailed explanation of the monitoring and protection features of the DRV3205-Q1 device.

3.5.1 VDS Sensing

To protect the external FETs from overcurrent damage, VDS sensing circuitry is implemented in the DRV3205-Q1 device using two comparators for each half-bridge. One comparator is for the high-side and the other is for low-side, as shown in Figure 7. The high-side comparator is placed between the VSH and SHSx pins. The low-side comparator is placed between the SHSx and SLSx pins.

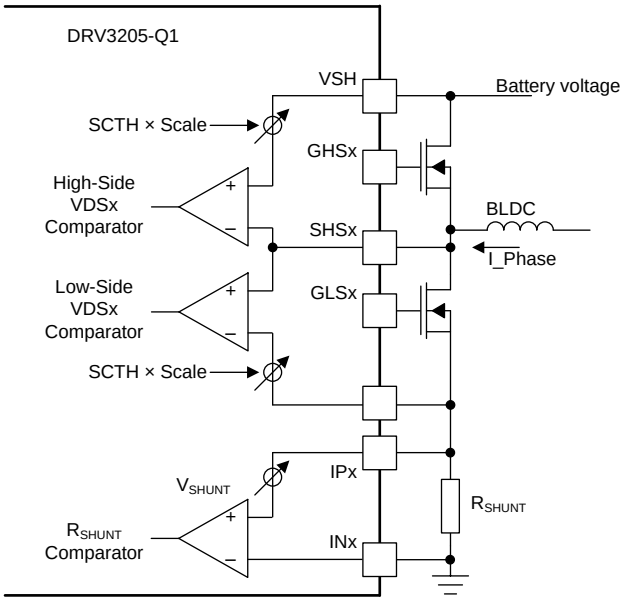


Figure 7. Predriver and Some of the FET Protection Modules in the DRV3205-Q1

A voltage threshold can be calculated and programmed depending on the on-resistance and maximum-allowed current of the external MOSFETs. Exceeding this threshold triggers the VDS overcurrent feature. The voltage threshold level (SCTH) is programmable through the SPI SCTH setting in register 0x01 (CFG0), bits [6:3], and can be changed during gate driver operation if needed.

The VDS protection logic has a SPI programmable and adjustable masking time and deglitch time to prevent false trips caused by switching voltage transients. The deglitch time is a delay inserted after the VDS sensing comparators have tripped to when the protection logic is informed that a VDS event has occurred. This deglitch time is used to prevent false detection because of normal switching transients on the comparator input pins.

Use Equation 1 to calculate the overcurrent trip level at which the VDS voltage exceeds the programmed VDS threshold value with a specific MOSFET on-resistance (RDson).

$$\text{Overcurrent trip} = \frac{\text{Vds}_{\text{Level}}}{\text{Rdson}} \tag{1}$$

Several other factors must be considered before setting the overcurrent level. Typical MOSFETs used in EPS systems have an RDson specification that varies a total of over 100% across temperature and device variation. The minimum RDson from the MOSFET data sheet must be used when calculating the upper current limit. Additionally, the DRV3205-Q1 device has an offset specification. The desired best-case trip point (lowest current to cause a VDS error) should be set to the lower limit of the offset specification with the worst-case trip point (highest current to cause a VDS error) at the high limit of the specification as shown in Figure 8.

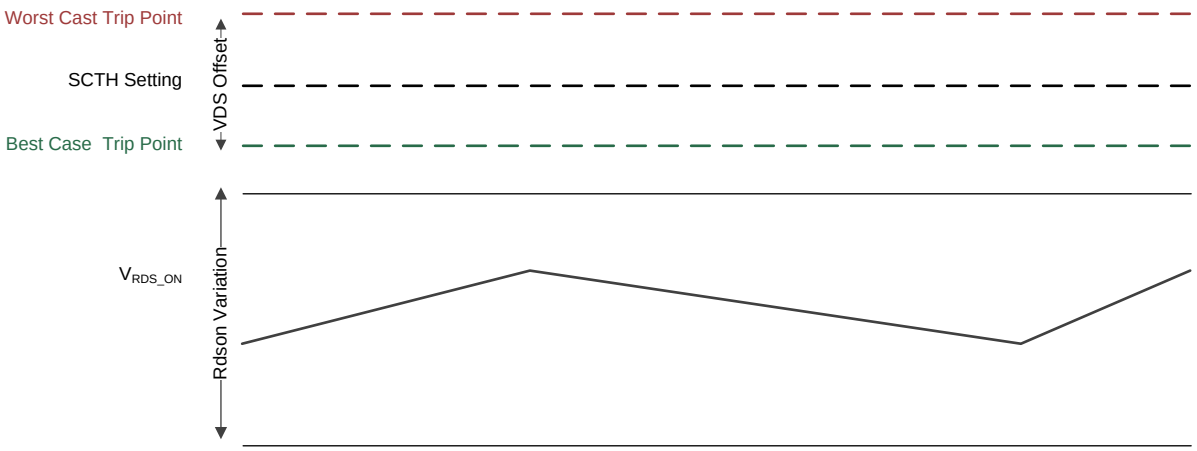


Figure 8. Variations in VDS Detection

3.5.2 Latent Fault Detection of VDS Monitors

The DRV3205-Q1 device provides several ways to detect latent faults. At power up, or by command, the device runs through an analog built-in self-test (ABIST) routine, which internally tests the comparators. Another way of diagnosing latent faults is by making the VDS protection always trip. Making the VDS protection always trip can be done either by programming a negative VDS threshold (used only for diagnostics), or by setting DRVOFF high and turning on the respective gate.

3.5.3 Gate Driver

The DRV3205-Q1 device has three high-side and three low-side gate drivers, with individually programmable source and sink currents for each gate. The gate driver is powered from the boost converter to provide the necessary gate-source voltage.

Because of the high current demand in most EPS applications, the external MOSFETs used have low RDson, high continuous current, and high total-gate charge. As the current demand increases, the parasitic effects become more apparent. To reduce these effects, protection and filtering can be added as shown in Figure 9.

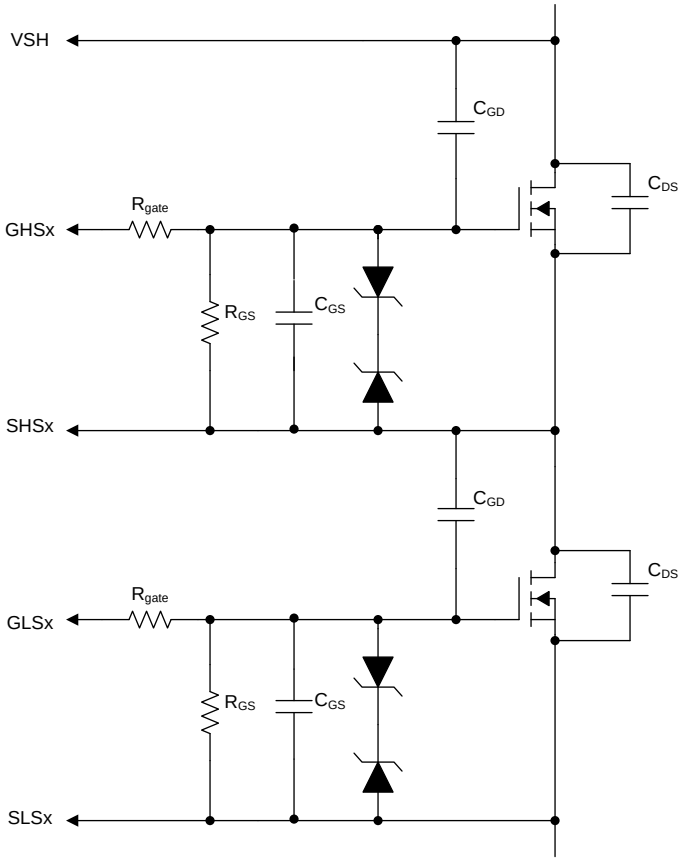


Figure 9. Example Half Bridge Configuration

- **R_{Gate}** is used to control the switching rate of the MOSFET and reduce ringing caused by parasitic inductance on the board. These are typically sized in the tens of ohms or less.
- **R_{GS}** is used to avoid capacitive coupling on the gate, typically sized in the hundreds on kilo-ohms
- **C_{GS}** is used to control the switching rate of the MOSFET and reduce ringing by increasing the required gate charge
- **C_{GD}** is used to control the switching rate of the MOSFET and reduce ringing by extending the Miller region
- **C_{DS}** is used to dampen ringing for EMI reduction and remove large magnitude transients
- **Schottky Diodes** can be added to avoid negative voltage transients that occur because of the parasitic effects of switching a large inductive load. Depending on the application, these may not be needed as the DRV3205-Q1 device can withstand a large magnitude pulse on these pins. For more information on these effects, refer to *DRV3205-Q1 Negative Voltage Stress on Source Pins* (SLVA805).

Depending on the target system, not all of these components may be necessary. During development it may be helpful to test the usefulness of each of these components by adding the components to the schematic and only populating if needed.

3.5.4 Boost Converter

The output current capability of the boost converter can be configured with the external R_{boost_shunt} resistor to

$$0.15\ V / R_{boost\_shunt} \quad (2)$$

NOTE: This resistor must be able to conduct the boost switching current.

In this way, the output current capability can be dimensioned to the needed current determined by the PWM switching frequency and the gate-charge of the external power FETs. It is recommended to choose a coil having a current saturation level of at least 30% above the current limit level set with the resistor R_{boost_shunt}.

The operation principle of the boost converter is based on a burst-mode fixed-frequency controller. During the on-time, the internal low-side boost FET turned on until the current limit level is detected. The off-time is calculated proportionally from a 2.5-MHz time-reference by sensing the supply voltage, VS, and the output voltage, VBOOST. Use Equation 3 to calculate the off-time.

$$t_{off} = \frac{VS}{V_{BOOST} \times f_{BOOST}} \quad (3)$$

where

- f_{boost} = 2.5 MHz

Figure 10 shows how the current appears for steady-state, operation

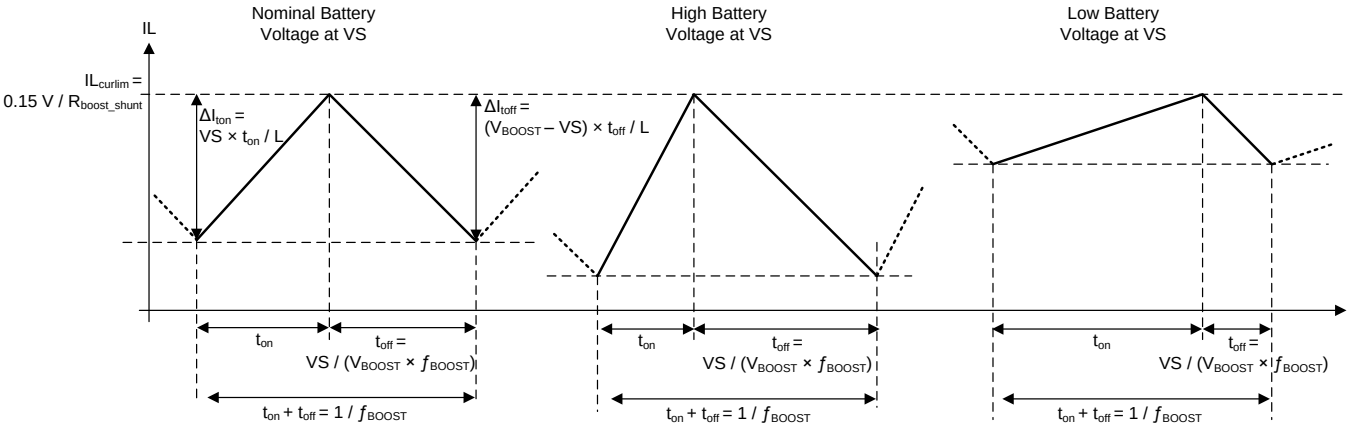


Figure 10. Coil Current Waveforms in Steady State for Nominal, High, and Low Battery Voltage

Referring to Figure 10, use the following equations to calculate the ripple current and the boost output current:

$$IL_{ripple} = \frac{VS}{L \times f_{BOOST}} \times \left(1 - \frac{VS}{V_{BOOST}}\right) = \frac{(V_{BOOST} - VS) \times VS}{L \times f_{BOOST} \times V_{BOOST}} \quad (4)$$

$$I_{BOOST} = \frac{VS}{V_{BOOST}} \times IL_{curlim} - \frac{1}{2} \times \left(\frac{(V_{BOOST} - VS) \times VS}{L \times f_{BOOST} \times V_{BOOST}}\right) \quad (5)$$

$$f_{BOOST} = 2.5\ MHz; \quad (V_{BOOST} - VS) = 15\ V; \quad IL_{curlim} = \left(\frac{0.15\ V}{R_{shunt\_boost}}\right) \quad (6)$$

As shown in Equation 5, the boost output-current capability for a given IL_{curlim} is the lowest for the minimum supply voltage VS. Therefore the boost output-current capability must be dimensioned (by setting IL_{curlim} with external R_{shunt_boost}) such that the required output current (based on PWM frequency and gate-charge of the external power FETs) can be delivered at the required minimum supply voltage for the application. Equation 7 gives IL_{curlim} as a function of I_{BOOST} and *VS*:

$$IL_{curlim} = I_{BOOST} \times \frac{V_{BOOST}}{VS} + \frac{1}{2} \times \left(\frac{V_{BOOST} - VS}{L \times f_{BOOST}} \right) \quad (7)$$

For setting the value of IL_{curlim}, the minimum application supply must be used in Equation 7 and the value of I_{BOOST} should be used as calculated in Equation 5.The minimum application supply voltage that the DRV3205-Q1 device can support is 4.75 V.

As shown in Equation 5, the boost output-current capability increases for a higher supply voltage (VS). In case the boost output-current capability is dimensioned such that it can deliver the necessary output current for the minimum supply voltage, the boost output actually delivers more current than is required for the nominal supply voltage. This additional current causes the boost voltage to increase. Therefore, a hysteretic comparator (low-level VBOOST-VS = 14 V, high-level VBOOST-VS = 16 V) determines starting and stopping of the burst pulsing. Figure 11 illustrates this.

The nominal switching frequency during the burst pulsing is 2.5 MHz when the boost reaches the steady state. During startup of the boost, the internal time reference is made a factor 3 slower, resulting 3 times longer off-times compared to Equation 3 to allow the coil current to decrease sufficiently.

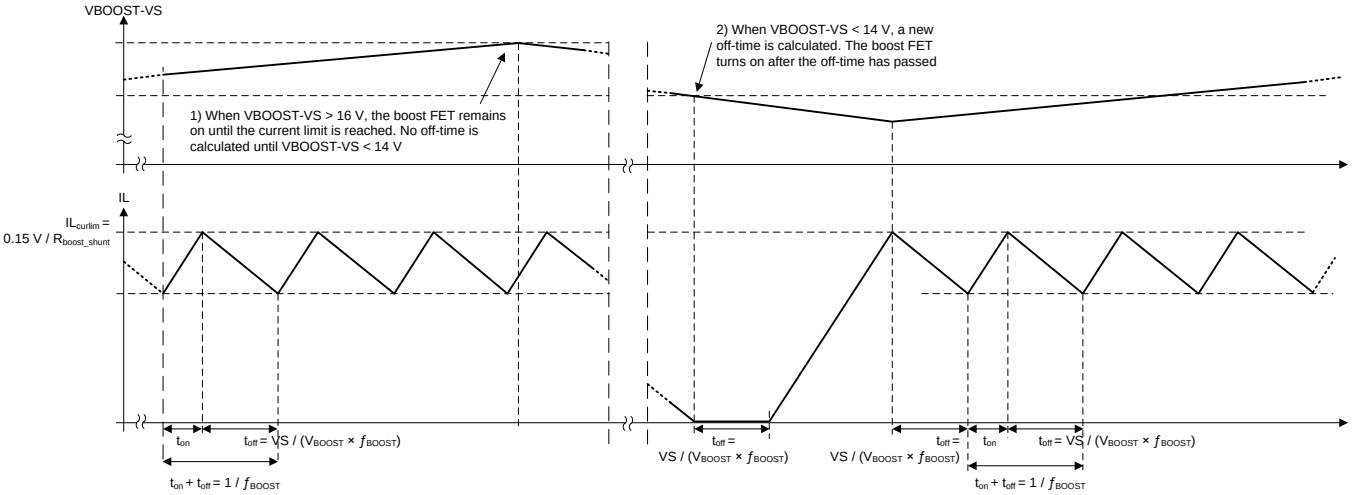


Figure 11. Boost Waveforms Showing Burst Pulsing Controlled by Hysteretic Comparator Levels

3.5.5 Low-Side Current Shunt Monitors

The low-side current shunt amplifier can also be configured as an overcurrent detection to allow the DRV3205-Q1 device to automatically shut down without MCU interaction. The advantage of this method compared to the VDS comparator for motor overcurrent detection is a much higher accuracy. The VDS monitor method detects a high voltage drop from the RDson resistance, however this range can be wide and varies over temperature. The low-side shunt is typically more accurate than the RDson resistance and is therefore more stable. Because of this stability the overcurrent threshold can be set much closer to the overcurrent limit.

The VDS monitor is well suited for detecting hard shorts such as a short of the motor phase to battery or ground. The shunt resistor monitor is good for monitoring motor current and providing shutdown based on motor over current.

3.5.6 Current-Shunt Amplifiers

The DRV3205-Q1 device includes three, bidirectional and high-performance low-side current-shunt amplifiers for accurate current measurement using low-side shunt resistors in the external half-bridges. These amplifiers are commonly used to measure the motor phase current to implement overcurrent protection, external torque control, or external commutation control through the application MCU. If individual half-bridge sensing is not required, a single current-shunt amplifier can be used to measure the sum of the half-bridge current.

The most important features of the current-sense amplifiers are as follows:

- High Performance—Low input-referred offset and low offset drift over temperature.
- Directionality—This feature supports bidirectional current sensing.
- Amplifier gain—Four SPI-programmable gains are available (8, 12, 16, and 32 V/V).
- Reference Voltage—Programmable bias voltage through SPI.

Use the simple procedure that follows to configure the current-sense amplifiers:

Step 1. Determine the peak current that the motor will demand. This demand depends on the motor parameters and the application requirements.

Step 2. Determine the available voltage output range for the current shunt amplifiers. This range is the ± voltage around the amplifier bias voltage (RO).

Step 3. Determine the sense-resistor value and amplifier gain settings. The sense-resistor value and amplifier gain have common tradeoffs. The larger the sense resistor value, the better the resolution of the half-bridge current. This tradeoff comes at the cost of additional power dissipated from the sense resistor. A larger gain value allows for the use of a smaller resolution, but at the cost of increased noise in the output signal and a longer settling time.

3.5.6.1 Current Sense Filtering

To read the phase current, the low-side MOSFET must be turned on for the particular phase. Because of the low side source ringing, the voltage across the shunt resistor can ring when the switch is opened causing a delay before a valid reading can be captured. A higher voltage can also cause the input amplifier to saturate with adverse effects. Additionally, changes in the common mode because of the switching on other phases can further create noise across the shunt resistor, causing errors in the measurement.

To reduce the effects on the amplifier, a series of filters can be implemented. Figure 12 shows an example configuration with common and differential mode filters. The filtering on the input should be selected to balance the tradeoff of lower bandwidth with better noise performance.

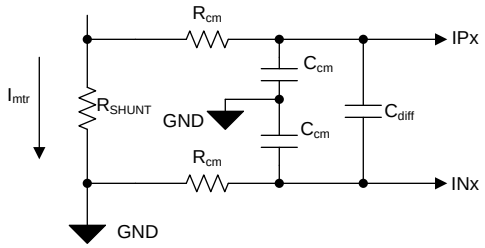


Figure 12. Example Shunt Resistor Filtering

3.5.7 MCU Watchdog Timer

The DRV3205-Q1 device can be configured to monitor the health of the MCU using a question-and-answer watchdog timer. By periodically checking the MCU, the DRV3205-Q1 device can shut down the external MOSFETs and bring the system to a safe state. The question and answer watchdog operates at on a periodic basis by sending specific message sequences through SPI. Upon the request of the MCU, the DRV3205-Q1 device provides a token (or question) to the MCU over SPI, latched in the WDT_TOKEN_VALUE register. The MCU performs a fixed series of arithmetic operations on the token value and returns the resulting token value answers to the ASIC over SPI by writing to the WDT_ANSWER register. The DRV3205-Q1 device verifies that the MCU returns the token value responses (answers) within the specified timing windows, and that the token value responses are correct.

For details on how to configure and run the watchdog timer, refer to *Q&A Watchdog Timer Configuration for DRV3205-Q1* (SLVA831).

3.5.8 Reverse Battery Protection Support

A car battery that is installed with the terminal connections reversed, or an attempt to jump start the car with the leads connected backward, could damage the EPS if it is not protected. Several techniques are available that can be used to provide reverse battery protection when designing an EPS.

One technique is to use a power NMOS and an NPN BJT to achieve reverse battery protection. If the battery is connected in reverse then the body diode of the NMOS will not conduct current, nor will the NMOS turn on, thereby protecting the system from the reverse polarity condition. When the battery is connected correctly, the circuit permits current to flow with very little power lost due to the low RDson of the NMOS.

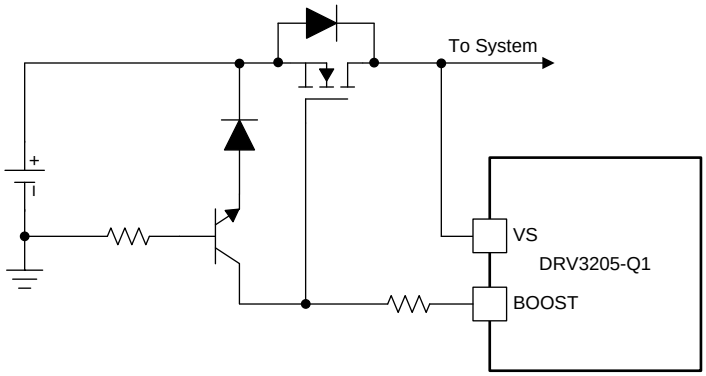


Figure 13. Example Reverse Batter Protection

For the NMOS to turn on, the gate voltage must be higher than the source voltage. This cannot be accomplished with the battery alone so the gate must be tied to an overdrive voltage. This technique usually requires additional circuitry to produce a suitable gate-to-source voltage to turn on the NMOS, often in the form of a charge pump or boost regulator.

The DRV3205-Q1 device is well suited for this type of reverse battery topology because the integrated boost regulator provides the necessary overdrive voltage to turn on the power NMOS. No additional external circuitry is required to supply the overdrive voltage, so both cost and PCB real estate is saved.Figure 14 shows an alternate configuration.

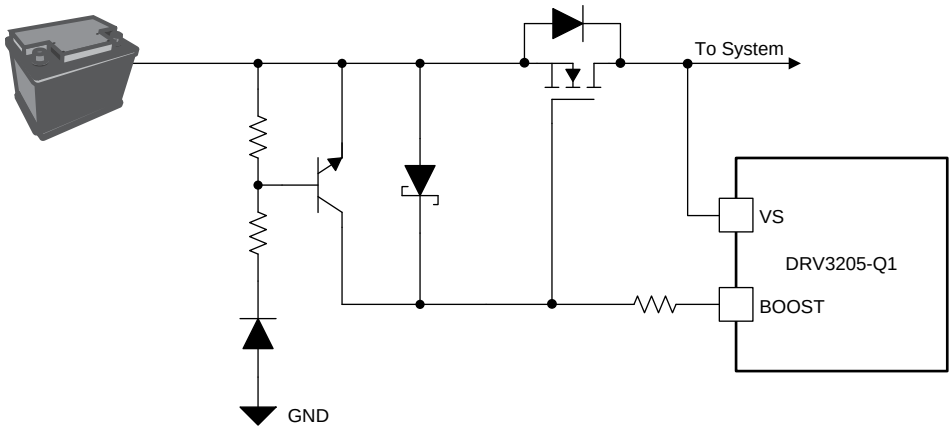


Figure 14. Alternate Reverse Batter Protection Example

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