Application Report
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Power Supply Design for NXP i.MX 7 Using the TPS65023

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ABSTRACT

This document details the design considerations of a power management unit solution for the NXP i.MX 7 processor using the TPS65023 power management IC (PMIC).

The TPS65023 has an input range from 2.5 to 6 V. The device has three low-dropout (LDO) regulators and three step-down converters that provide the 1-, 1.35-,1.8-, 3-, and 3.3-V rail signals in the appropriate power-on and power-off sequence that is required by the i.MX 7. For an i.MX 6 power solution please refer to the VVDN design on RadiumBoards website.

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1 Introduction

This reference design applies to the NXP i.MX 7 Solo and Dual family of applications processors. This report provides all the required external components necessary to achieve the required output and sequence to power on and off the i.MX 7 processor. This reference design provides a solution for Vin being 5 V, DDR3L requiring 1.35 V, and NVCC power domain requiring 1.8 V. However if DDR3, LPDDR2, or LPDDR3 is desired, the necessary output can be achieved through a resistor divider, which is detailed in this document.

2 Power Requirements

Figure 1 shows a block diagram of the TPS65023 and i.MX 7 processor interfaces. A circuit schematic detailing the TPS65023 and the sequencing circuit is shown in Figure 3.

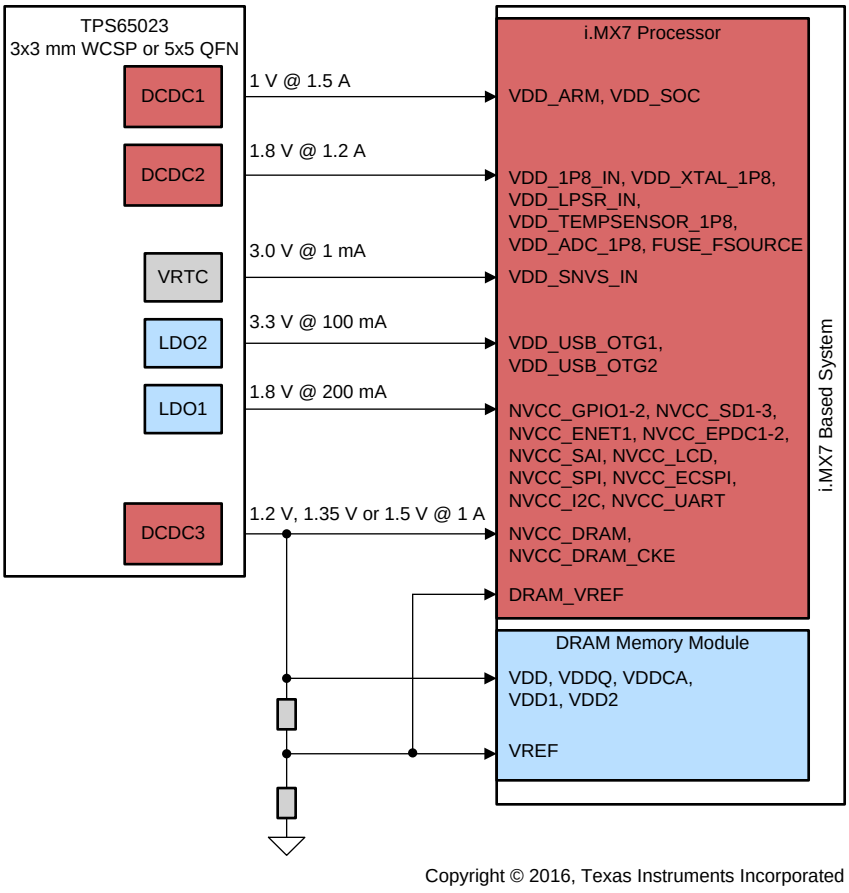

Figure 1. TPS65023 Power Solution Block Diagram

The i.MX 7 power requirements are listed on Table 1 provided by the i.MX 7 Dual Family of Applications Processors Data Sheet and the i.MX 7 Solo Family of Applications Processors Data Sheet.

Table 1. i.MX 7 Power Requirements

TPS65023					i.MX 7		
POWER-UP SEQUENCE	POWER-DOWN SEQUENCE	POWER SUPPLY	Iout [mA]	OUTPUT VOLTAGE [V]	POWER SUPPLY	NOMINAL RATING [V]	MAX CURRENT [mA]
2	2	DCDC1	1500	1.0	VDD_ARM, VDD_SOC	Minimum: 0.95 Typ: 1 Maximum: 1.155	1500
2	2	DCDC2	1200	1.8	VDD_1P8_IN, VDD_XTAL_1P8, VDD_LPSR_IN, VDD_TEMPSENSOR_1P8, VDD_ADC_1P8, FUSE_FSOURCE	1.8 V ± 5%	600
3	1	DCDC3	1000	1.35	NVCC_DRAM, NVCC_DRAM_CKE	Minimum: 1.283 Typ: 1.35 Maximum: 1.45	1000
3	1	LDO1	200	1.8	NVCC_GPIO1-2, NVCC_SD1-3, NVCC_ENET1, NVCC_EPDC1-2, NVCC_SAI, NVCC_LCD, NVCC_SPI, NVCC_ECSPI, NVCC_I2C, NVCC_UART	1.8 V ± 8.33%	100[(1)]
3	1	LDO2	100	3.3	VDD_USB_OTG1, VDD_USB_OTG2	3.3 V ± 9.09%	100
1	3	VRTC	1	3.0	VDD_SNVS_IN	3.0 V ± 20%	1

(1) NVCC rail requirements are estimated to be well below 100 mA. LDO1 can provide up to 100 mA and is reflected in the table, which depends on the processor requirements.

The TPS65023 fulfills all the power requirements with three step-down converters and three LDO regulators. In order to meet the power sequence requirements, a simple sequencing circuit is used, which is detailed in Figure 3.

Even though all the rail requirements are met, combining VDD_ARM and VDD_SOC limits the processor speed to 800 MHz. This combination also limits low-power mode by maintaining VDD_ARM on during low power mode. Because the i.MX 7Solo family runs at an 800-MHz frequency, the i.MX 7Dual family will also have to run at 800-MHz frequency with this design.

2.1 Power-On Sequence

The required power-on sequence specified by the i.MX 7 datasheet is as followed.

1. VDD_SNVS_IN – supplied by VRTC
2. VDD_SOC and VDD_ARM – supplied by DCDC1
3. NVCC_DRAM and NVCC_DRAM_CKE – supplied by DCDC3

The first step is turning on VDD_SNVS_IN with VRTC. In the TPS65023 one of the three LDO regulators is designated as VRTC with an output of 3 V. VRTC defaults to turning on when the TPS65023 powers on, which means VDD_SNVS_IN will always be the first rail on.

The second step comes in the sequencing circuit. A slider switch is used in the schematic; however, the switch can be replaced with an outside enable signal going HIGH. By setting the signal HIGH it will set diode D1 to be forward bias, whereas, diodes D2 and D3 are reverse bias. With diode D1 in forward bias, EN_1 signal goes HIGH and turns on DCDC1 and DCDC2. DCDC2 turns on at this time because there are no sequence requirements necessary for what DCDC2 powers. The threshold voltage for the enable input is 1.3 V. With DCDC1 at 1 V, DCDC1 is unable to set the enable pin high, which is why DCDC2, at 1.8 V, is used to turn on the remaining enable pins.

When DCDC2 reaches 1.8 V, DCDC2 output goes through an RC (R14 and C14) delay before enabling DCDC3 and the remaining two LDO regulators. Once reaching operating level, DCDC3 goes through a resistor divider and RC delay before going to the PWRFAIL_SNS pin, which will set the internal comparator for the PWRFAIL signal.

The power-on sequence is complete. The proper connections for the power-on sequence are detailed in the schematic shown in Figure 3.

2.2 Power-Off Sequence

From the i.MX 7 datasheet, the processor must be powered off in the reverse order of the power-on sequence.

1. NVCC_DRAM and NVCC_DRAM_CKE – supplied by DCDC3
2. VDD_SOC and VDD_ARM – supplied by DCDC1
3. VDD_SNVS_IN – supplied by VRTC

To begin the turn off sequence, the switch is turned off or the enable signal is set to LOW making diodes D2 and D3 forward biased. PWRFAIL_SNS becomes LOW pulling PWRFAIL LOW. EN_2 becomes LOW and causes the output of DCDC3 and the LDOs to ramp down.

In the meantime D1 is now reverse bias, allowing for C13 to discharge into R11, which creates a delay longer than the ramp down of DCDC3 and the LDO regulators. At this point steps DCDC3 and DCDC1 are shut off in the correct order. VRTC is tied to Vin and, therefore, will power down when Vin starts ramping down. This power down sequence ensures that VRTC is the last rail on fulfilling all the requirements for the power-off sequence.

The proper connections for the power off sequence are shown in Figure 3.

2.3 Adjusting the Step-Down Output

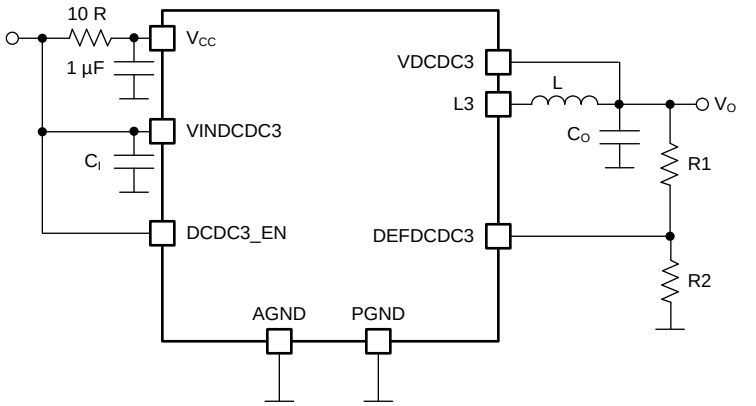

Figure 2. External Resistor Divider

The DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins are used to set the output voltage for each step-down converter. By using an external resistor divider, the output voltage can be set from 0.6-V up to the input voltage $V_{(bat)}$. The total resistance (R1 + R2) of the voltage divider must be kept in the 1-MΩ range to maintain a high efficiency at light loads.

$$V_{(DEFDCDCx)} = 0.6\ V \quad (1)$$

$$V_{OUT} = V_{DEFDCDCx} \times \frac{R1 + R2}{R2} \quad (2)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{DEFDCDCx}} \right) - R2 \quad (3)$$

2.4 Adjusting the Sequencing Circuit

In the schematic shown in Figure 3, the sequence circuit is designed with a DCDC3 output of 1.35 V. If DDR3, LPDDR2, or LPDDR3 is desired over DDR3L then the resistor divider (R16 and R17) needs to be changed accordingly to provide 1 V to PWRFAIL_SNS.

3 Schematic

Figure 3 shows the circuit schematic as well as detailing the external components necessary for the TPS65023 to achieve the 1-, 1.35-, and 1.8-V power rails required by the i.MX 7. The sequencing circuit is also detailed to achieve the proper power-on and power-off sequence. A slider switch is depicted in the schematic; however, any switching mechanism can be used, for example, an external enable signal.

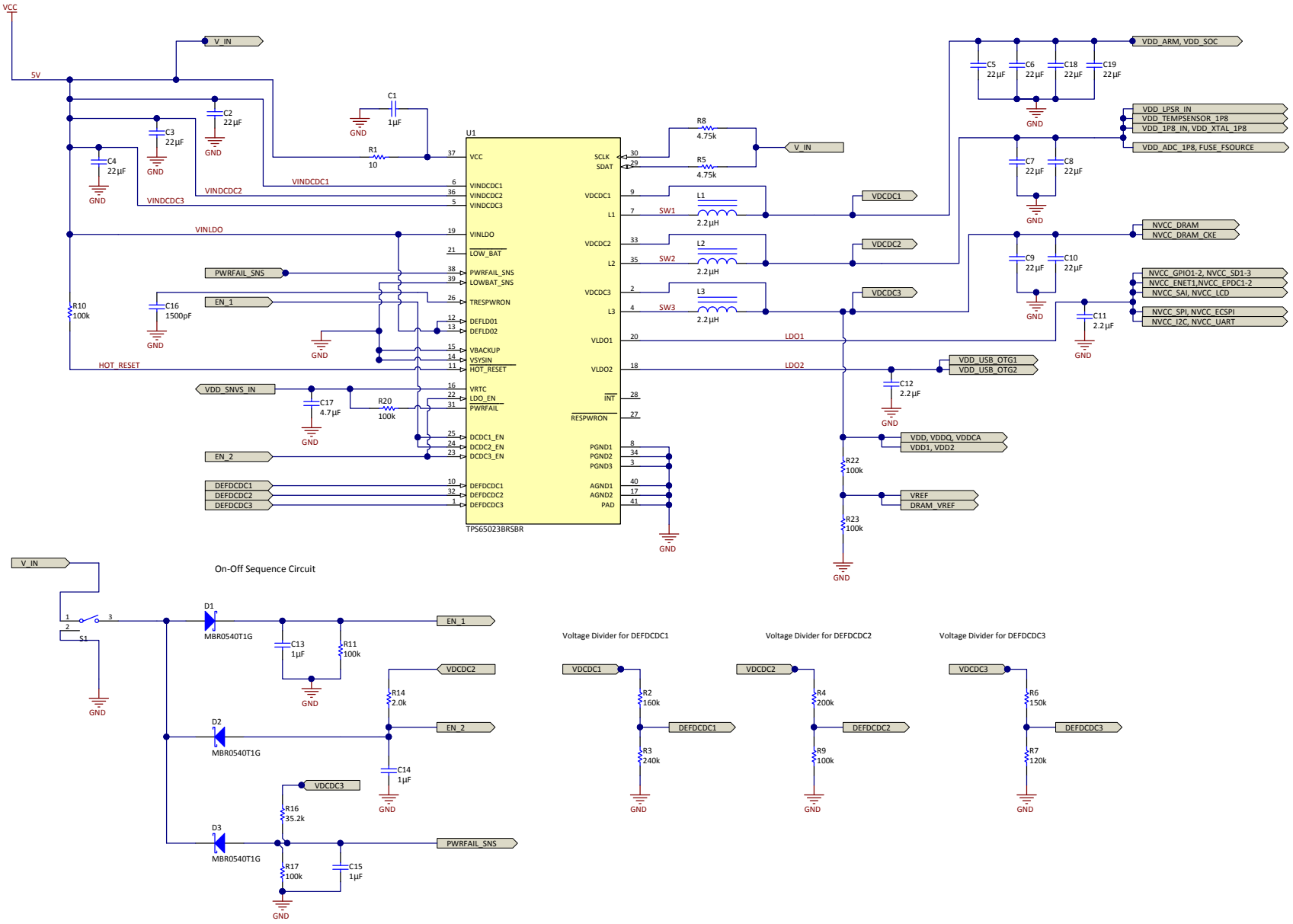

Figure 3. TPS65023 Power and Sequencing Circuit for i.MX 7 Powering Requirements

4 Bill of Materials (BOM)

The BOM is displayed in Table 2.

Table 2. Bill of Materials

COUNT	REFDES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
4	C1, C13-C15	1 µF	Capacitor, ceramic, 16 V, X5R, 20%	0603	885012106017	Wurth
11	C2-C10, C18, C19	22 µF	Capacitor, ceramic, 10 V, X5R, 20%	0603	C1608X5R1A226M080AC	TDK
2	C11, C12	2.2 µF	Capacitor, ceramic, 10 V, X5R, 20%	0603	C0603C225M8PACTU	Kemet
1	C16	1500 pF	Capacitor, ceramic, 10 V, X5R, 10%	0201	GRM033R61A152KA01D	Murata
1	C17	4.7 µF	Capacitor, ceramic,10 V, X5R, 20%	0402	GRM155R61A475M	Murata
3	D1-D3		Diode, Schottky, 40 V, 0.5 A	SOD-123	MBR0540T1G	MCC Semi
3	L1-L3	2.2 µH	Inductor, shielded, ferrite, 1.72 A, 0.059 ohm, SMD	VLCF4020	VLCF4020T-2R2N1R7	TDK
1	R1	10	RES, chip, 5%, 0.063 W	0402	CRCW040210R0JNE	Vishay
1	R2	160 K	RES, chip, 1%, 0.063 W	0402	CRCW0402160KFKED	Vishay
1	R3	240 K	RES, chip, 1%, 0.063 W	0402	CRCW0402240KFKED	Vishay
1	R4	200 K	RES, chip, 1%, 0.063 W	0402	CRCW0402200KFKED	Vishay
2	R5,R8	4.75 K	RES, chip, 1%, 0.063 W	0402	CRCW04024K75FKED	Vishay
1	R6	150 K	RES, chip, 1%, 0.063 W	0402	CRCW0402150KFKED	Vishay
1	R7	120 K	RES, chip, 1%, 0.063 W	0402	CRCW0402120KFKED	Vishay
7	R9-R11, R17, R20, R22, R23	100 K	RES, chip, 1%, 0.063 W	0402	CRCW0402100KFKED	Vishay
1	R14	2 K	RES, chip, 5%, 0.063 W	0402	CRCW04022K00JNED	Vishay
1	R16	35.2 K	RES, chip, 0.1%, 0.1 W	0603	RT0603BRD0735K2L	Yageo
1	U1		Power Management IC for Li-Ion Powered Systems	RSB0040B	TPS65023BRSBR	TI

5 Waveforms

The following waveforms demonstrate the power-on and power-off sequence of the TPS65023 as required by the i.MX 7.

Figure 4 shows the power-on sequence where DCDC1 and DCDC2 turn on at the same time.

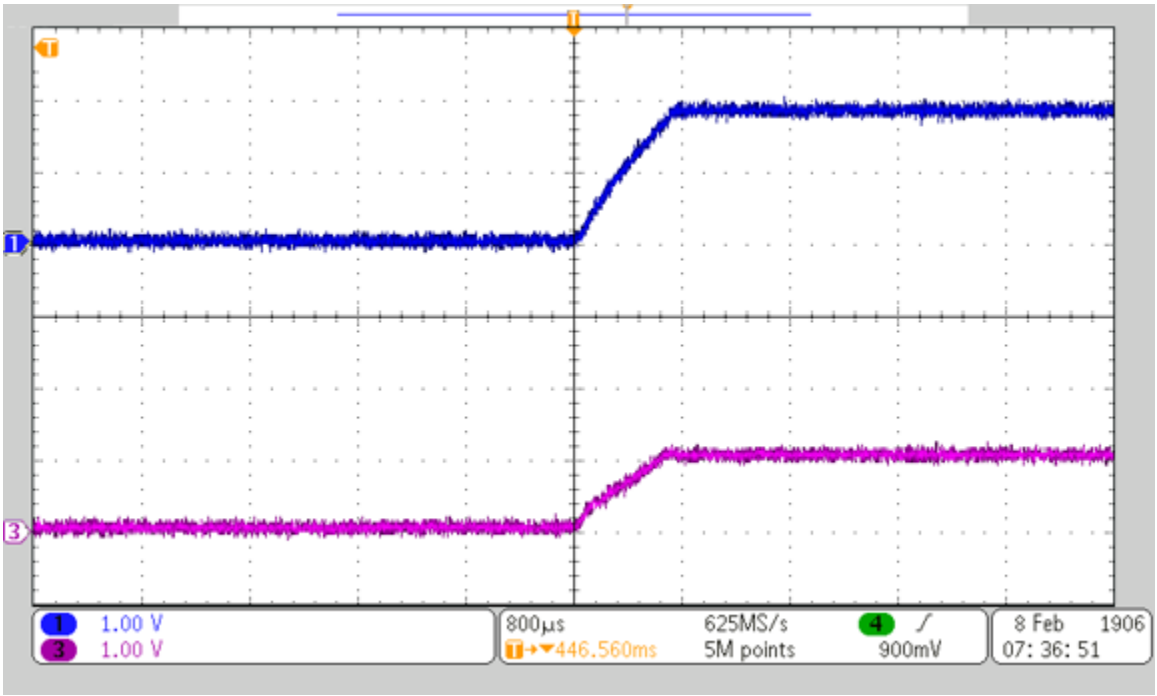

Figure 4. Power-On Sequence for DCDC1 and DCDC2

Figure 5 shows the start of the power-on sequence where DCDC2 turns on first, then the LDO regulators, and finally DCDC3. Only one of the LDO regulators is captured; however, both LDO regulators share the same enable pin.

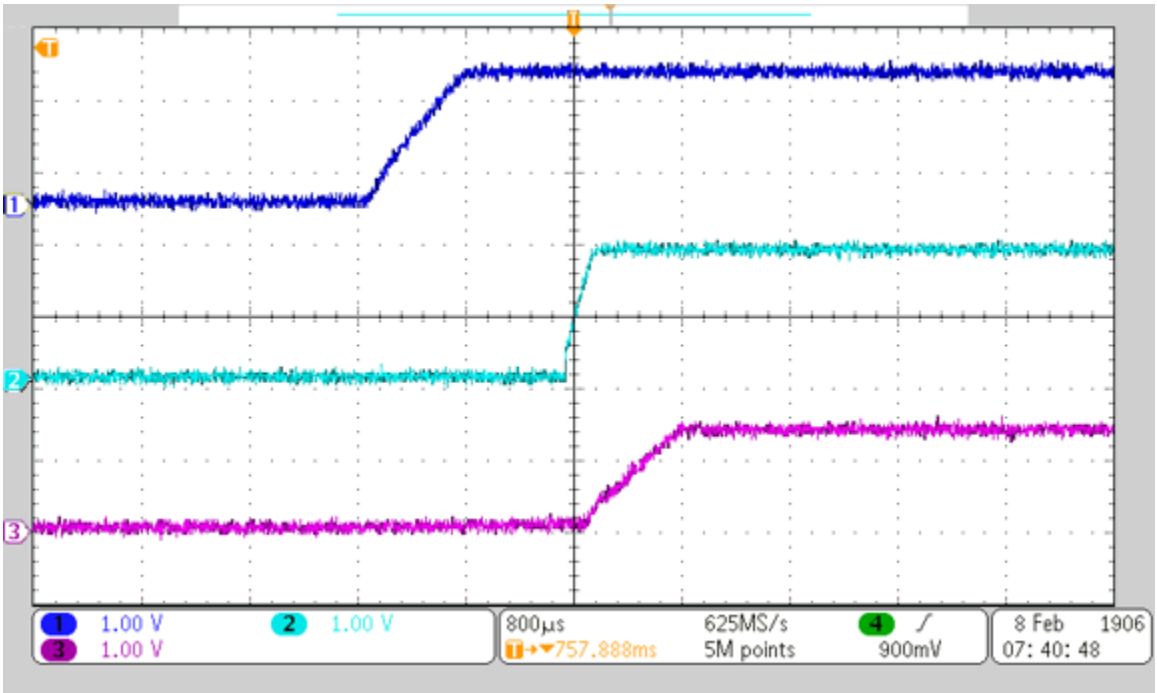

Figure 5. Power-On Sequence for DCDC2, LDO Regulators, and DCDC3

Figure 6 shows the power-off sequence for each output showing that DCDC1 and DCDC2 turn off at the same time, only after DCDC3 turns off. DCDC3 has an output load of 300 Ω.

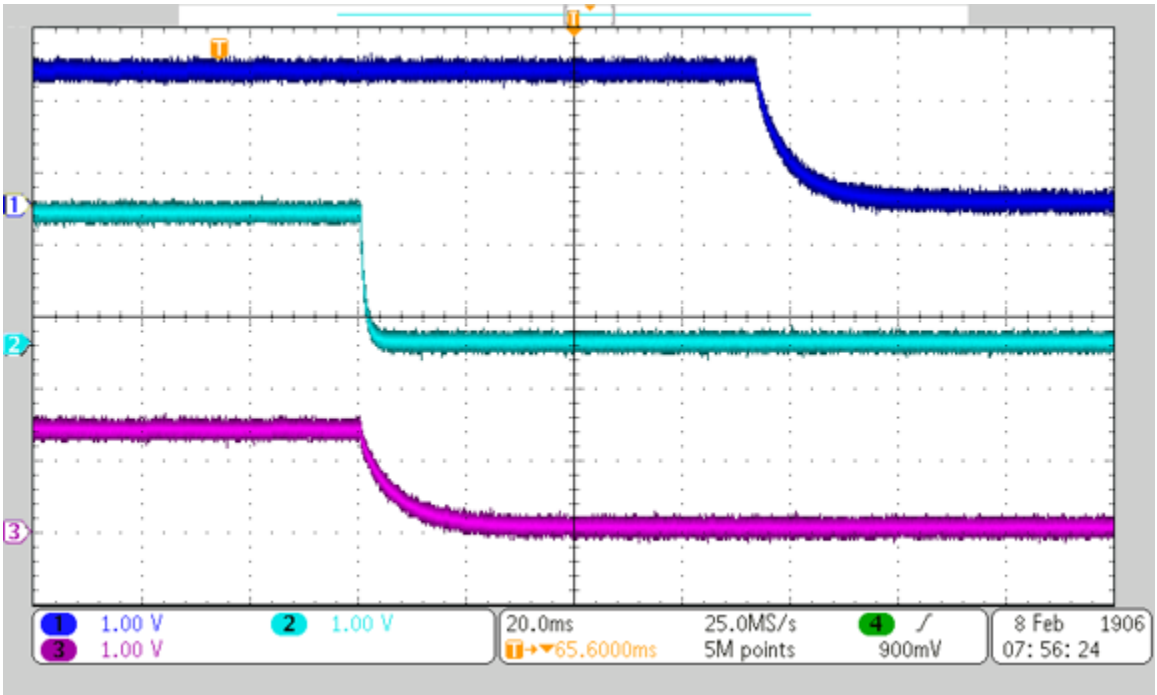

Figure 6. Power-Off Sequence for DCDC 1, DCDC2, and DCDC3. DCDC3 has Output Load of 300 Ω

Figure 7 shows the power-off sequence where DCDC3 and the LDO registers turn off at the same time and then DCDC2 turns off. DCDC3 and LDO have an output load of 300 Ω.

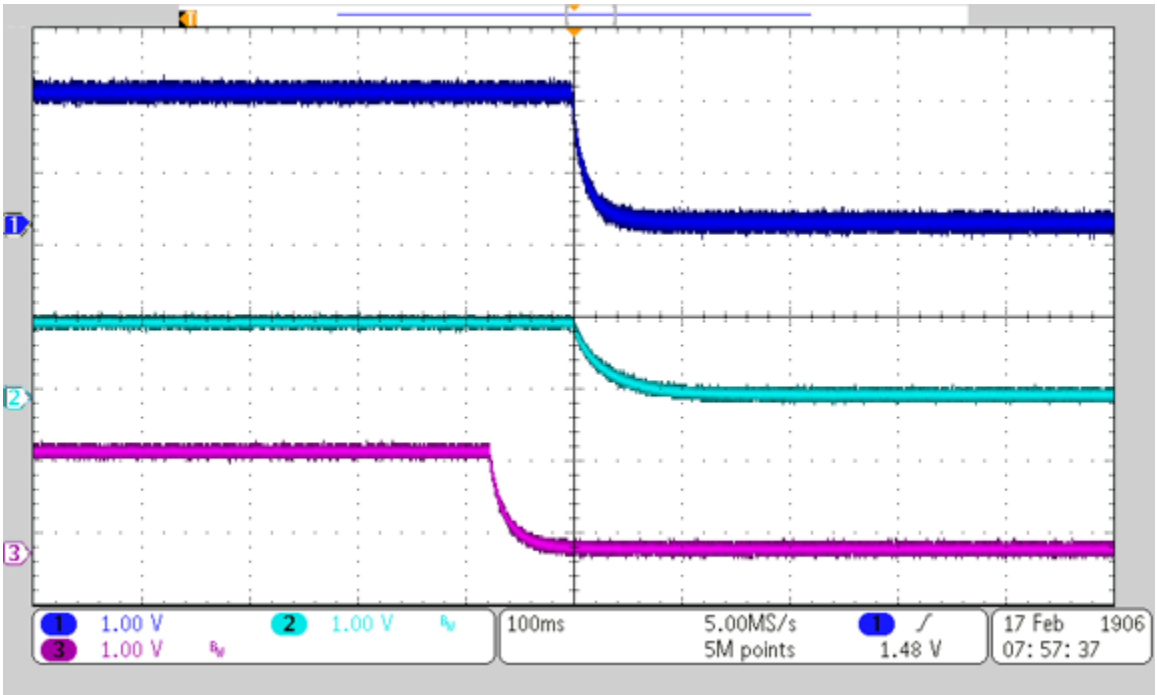

Figure 7. Power-Off Sequence for DCDC2, LDO Regulators, and DCDC3. DCDC3 and LDOs Have Output Load of 300 Ω

6 Transient Response

Table 3 provides the transient requirements and results for each step down. Transient requirements are provided by the i.MX 7 Dual Family of Applications Processors Data Sheet and the i.MX 7 Solo Family of Applications Processors Data Sheet.

Table 3. Transient Requirements and Results

DCDC1 TYP. VOLTAGE: 1.0-V			
	DCDC1 (mV)	DCDC1 RESULTS	i.MX7 REQUIREMENTS
Minimum	50	5%	5%
Maximum	54.4	5.44%	15.55%
DCDC2 TYP. VOLTAGE: 1.8-V			
	DCDC2 (mV)	DCDC2 RESULTS	i.MX7 REQUIREMENTS
Minimum	52	2.89%	5%
Maximum	54.4	3.02%	5%
DCDC3 TYP. VOLTAGE: 1.35-V			
	DCDC3 (mV)	DCDC3 RESULTS	i.MX7 REQUIREMENTS
Minimum	62	4.59%	4.96%
Maximum	61.2	4.53%	7.41%

Figure 8 shows the transient response of DCDC1 with a load going from 450 to 1500 mA in 1 µs. The transient response shows that DCDC1 fits within the necessary range of 1 V ± 5%.

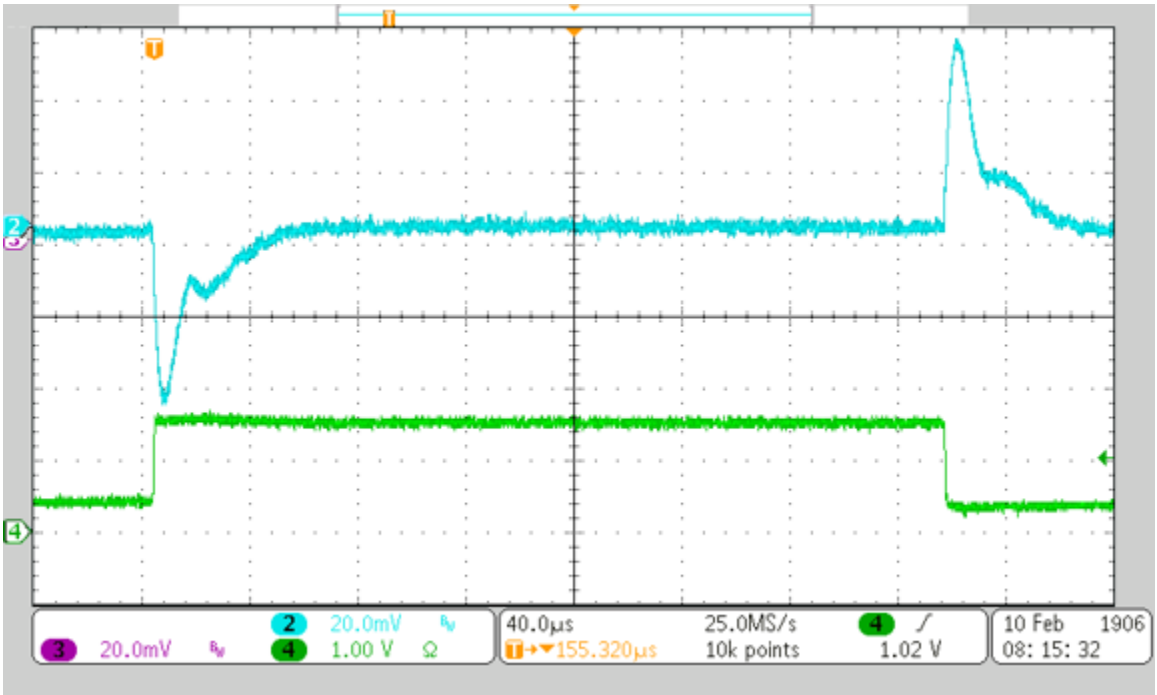

Figure 8. Transient Response for DCDC1

Figure 9 shows the transient response of DCDC2 with a load going from 360 to 1200 mA in 1 µs. The transient response shows that DCDC2 fits within the necessary range of 1.8 V ± 5%.

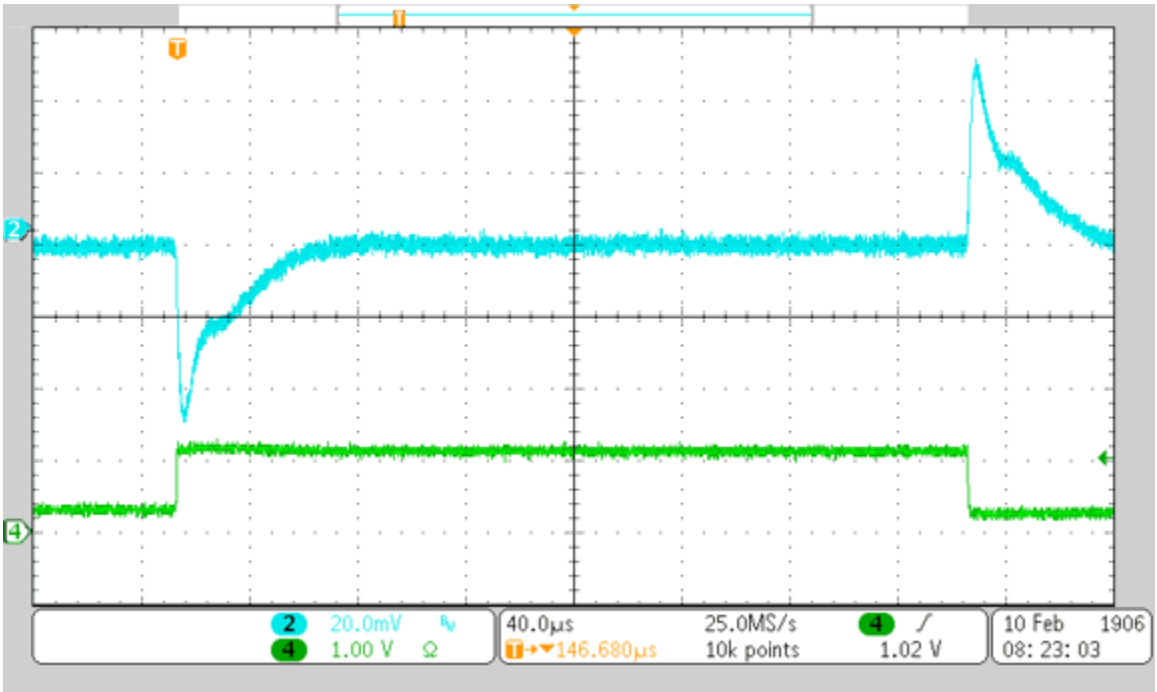

Figure 9. Transient Response for DCDC2

Figure 10 shows the transient response of DCDC3 with a load going from 300 to 1000 mA in 1 µs. The transient response shows that DCDC3 fits within the necessary range of 1.283 ≤ 1.35 ≤ 1.45.

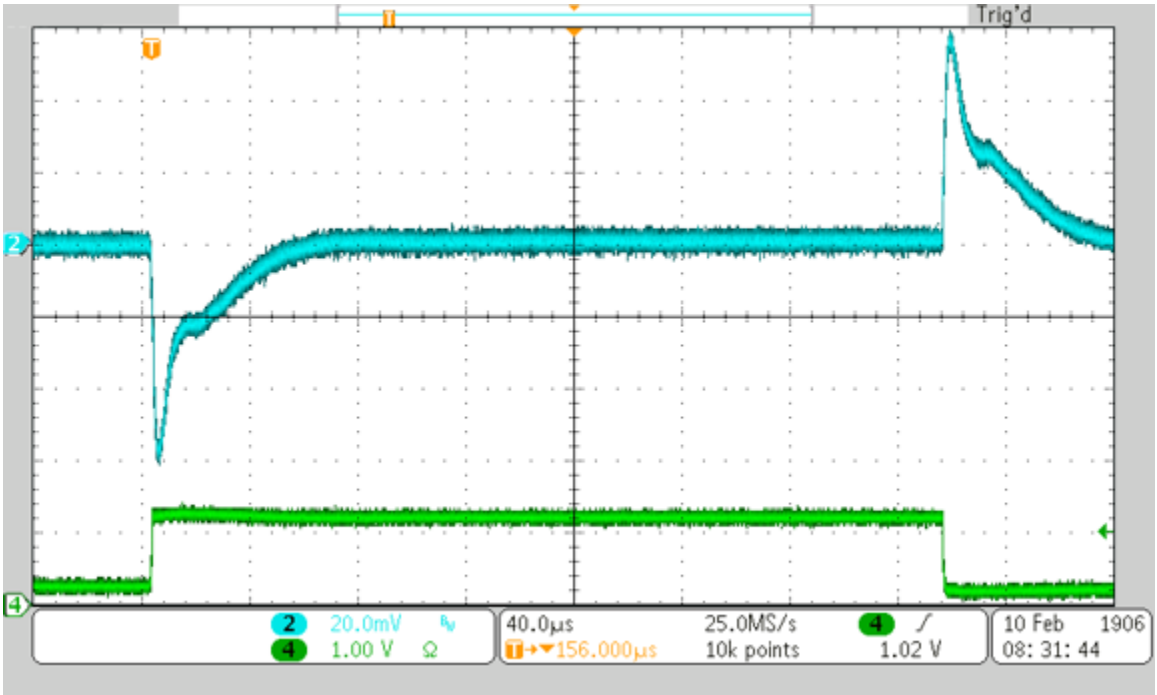

Figure 10. Transient Response for DCDC3

7 Efficiency Curve

The following efficiency curves show the efficiency for each of the converters over the possible range of output currents.

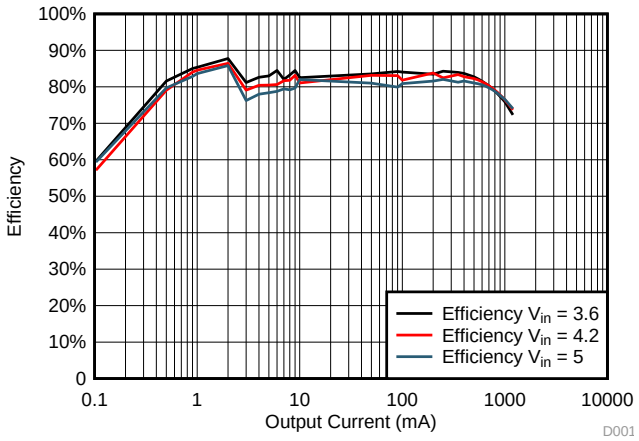

Figure 11. DCDC1 Efficiency

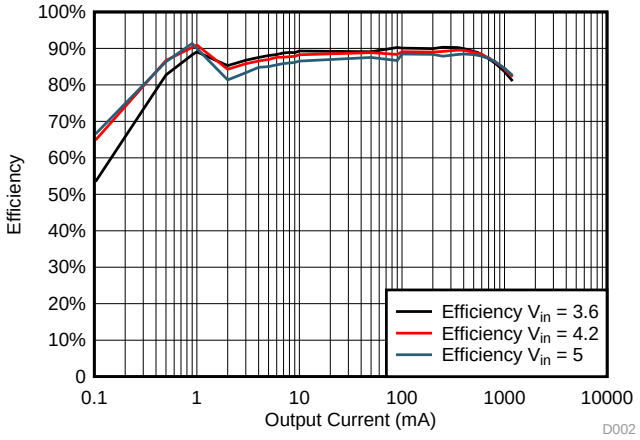

Figure 12. DCDC2 Efficiency

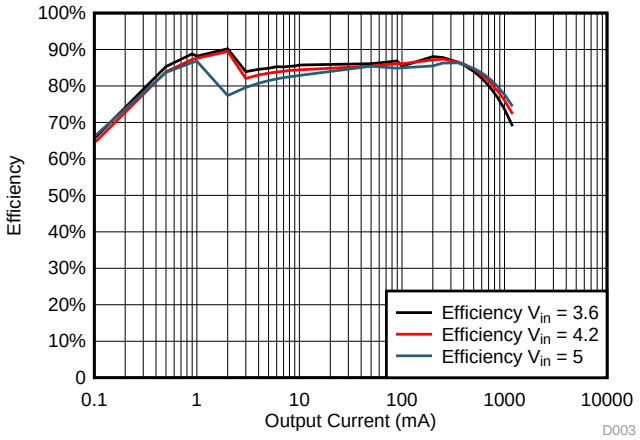

Figure 13. DCDC3 Efficiency

8 Layout

8.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. If the layout is not carefully done, the regulators may show poor line, load regulation, or both along with stability issues and electromagnetic interference (EMI) problems. It is critical to provide a low-impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitors must be placed as close as possible to the IC pins as well as the inductor and output capacitor.

For the TPS65023x, connect the PGND pins of the device to the PowerPAD™ land of the PCB, and connect the analog ground connections (AGND) to the PGND at the PowerPAD. It is essential to provide a good thermal and electrical connection of all GND pins using multiple vias to the GND-plane. Keep the common path to the AGND pins, which return the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The VDCDCx line must be connected right to the output capacitor and routed away from noisy components and traces (for example, the L1, L2, and L3 traces).

8.2 Layout Example

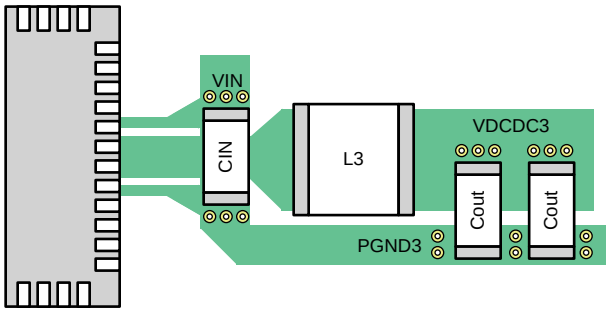

Figure 14. Layout Example of a DC-DC Converter

9 Conclusion

The TPS65023 provides a low-cost, comprehensive power solution for the i.MX 7 Solo and Dual family of application processors. This design demonstrates the ability to use external components to adjust the output of the TPS65023 to provide the required voltage rails for the i.MX 7. There is a schematic for a simple sequencing circuit that fits the power-on and the power-off sequence required by the i.MX 7. If DDR3, LPDDR2, or LPDDR3 is desired instead of DDR3L, the output voltage of DCDC3 can be adjusted by changing the resistor value in the resistor divider and in the sequencing circuit. All in all, the TPS65023 is a solution with the flexibility and ability to meet the various power requirements demanded by the i.MX 7.

10 References

1. Texas Instruments, *TPS65023x Power Management IC for Li-Ion and Li-Polymer Powered Systems*, TPS65023, TPS65023B Data Sheet (SLVS670)
2. NXP Semiconductors, *i.MX 7Dual Family of Applications Processors Data Sheet* (IMX7DCEC), Rev. 2, 06/2016
3. NXP Semiconductors, *i.MX 7Solo Family of Applications Processors Data Sheet* (IMX7SCEC), Rev. 2, 06/2016

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (May 2017) to C Revision	Page
• Changed the *TPS65023 Power and Sequencing Circuit for i.MX 7 Powering Requirements* schematic	6

Changes from A Revision (February 2017) to B Revision	Page
• Changed *Freescale* to *NXP*	2

Changes from Original (November 2016) to A Revision	Page
• Changed caption of Figure 6.	1
• Changed caption of Figure 7.	1
• Changed caption of Figure 6.	9
• Changed caption of Figure 7.	10

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