Application Report
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TPS55165-Q1 Layout Guidelines

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ABSTRACT

The TPS55165-Q1 device is widely used in the automotive applications. The layout of the printed-circuit board (PCB) is critical to achieve low EMI and stable power-supply operation. This application report provides guidance on how to route the TPS55165-Q1 buck-boost converter. Using this application report as a guide, the TPS55165-Q1 buck boost converter will work stably and achieve low EMI performance.

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Trademarks

1 Introduction

The TPS5516x-Q1 family of devices are high-voltage synchronous buck-boost DC-DC converters. The TPS55165-Q1 device provides a stable power-supply output from a wide varying input power supply such as an automotive car battery. The buck-boost overlap control ensures automatic transition between stepdown and step-up mode with optimal efficiency. The TPS55165-Q1 output voltage can be set to a fixed level of 5 V or 12 V. The TPS55160-Q1 and TPS55162-Q1 devices have a configurable output voltage ranging from 5.7 V to 9 V that is set by an external resistive divider.

This buck-boost converter uses four internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This feature enables the device to keep high efficiency over a wide input voltage and output power range. To avoid ground shift problems caused by the high currents in the switches, separate ground pins (GND and PGND) are used. The reference for all control functions are the GND pins. The power switches are connected to the PGND pins.

The layout of the printed-circuit board (PCB) is critical to achieve low EMI and stable power-supply operation. This application report provides the TPS55165-Q1 buck-boost converter layout guideline. Under the guidance of this application report, the TPS55165-Q1 can perform well with a 4-layer board.

For the TPS55165 board layout, a 2-layer board is not recommended. A 2-layer board will make the layout quite difficult. Especially when there are some signal wires which break the GND copper plane on the bottom layer, the high frequency current has to go back to the PGND pin with a bigger loop. As a result, the circuit cannot work normally, and the board will have stability issues.

2 Device Overview

2.1 Minimize the Input and Output AC Current Loop

Figure 1 shows the TPS55165-Q1 pin configuration. Pin 1 is the power ground pin. The source of the internal low-side FETs are connected to this pin. The PGND pin is closer to the power input VINP pin than it is from the VOUT pin. So when it is working in the boost or buck-boost mode, the output side AC loop causes the issue more easily if the output side decoupling capacitor is not properly placed.

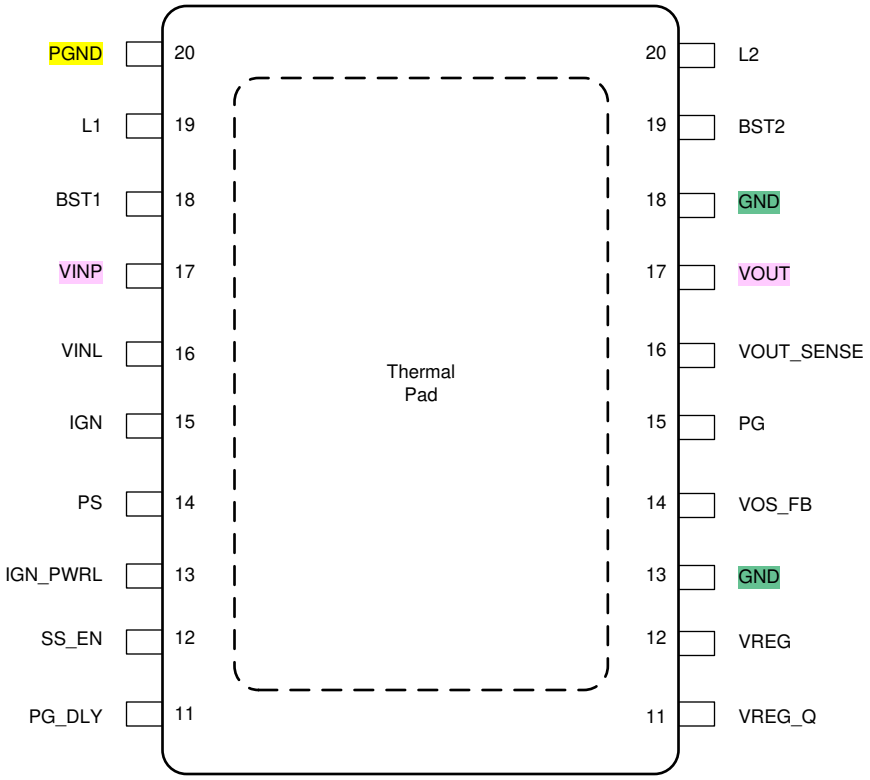

Figure 1. TPS55165-Q1 Pin Configuration

2.2 Minimize the Input and Output AC Current Loop With More Vias

A 4-layer board will make the layout quite easy. At least two layers of whole GND copper plane can be put under the silicon. As the *TPS5516xQ1-EVM Evaluation Module for 1-A Single-Inductor Buck-Boost Converter User Guide* indicates, the input and output high-frequency AC current goes back to the PGND pin through vias. Put as many vias as possible at the input capacitors, output capacitors, and the thermal pad of the silicon, so that the equivalent parasitic inductance is low enough to ensure the circuit can work stably.

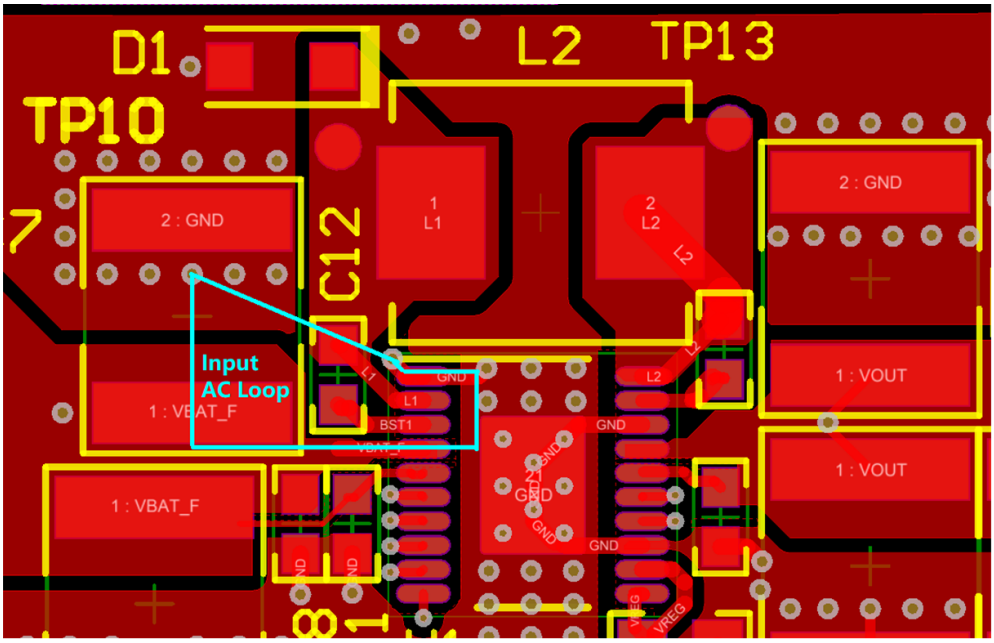

Figure 2. Input Critical AC Loop Under Buck or Buck-Boost Mode

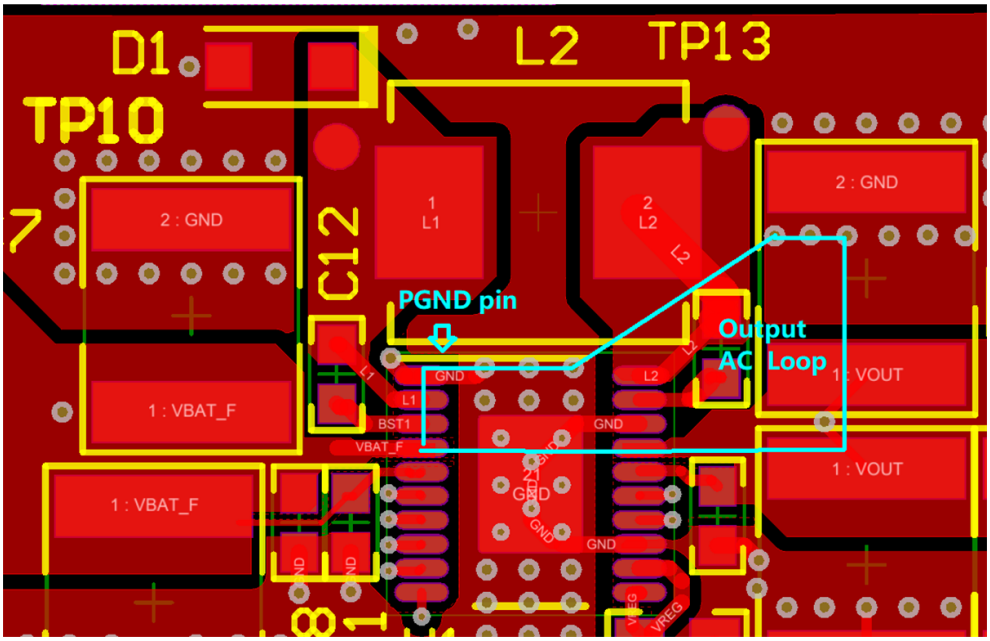

Figure 3. Output-Critical AC Loop Under Boost or Buck-Boost Mode

2.3 Minimize the Critical AC Current Loop by Proper Routing and Placement

Very small AC loop can also be achieved by proper routing. Figure 4 gives out an example. The main inductor connects with the IC through vias. Thus, the input and output high-frequency noise current can return to the PGND pin directly on the top layer with a very small loop.

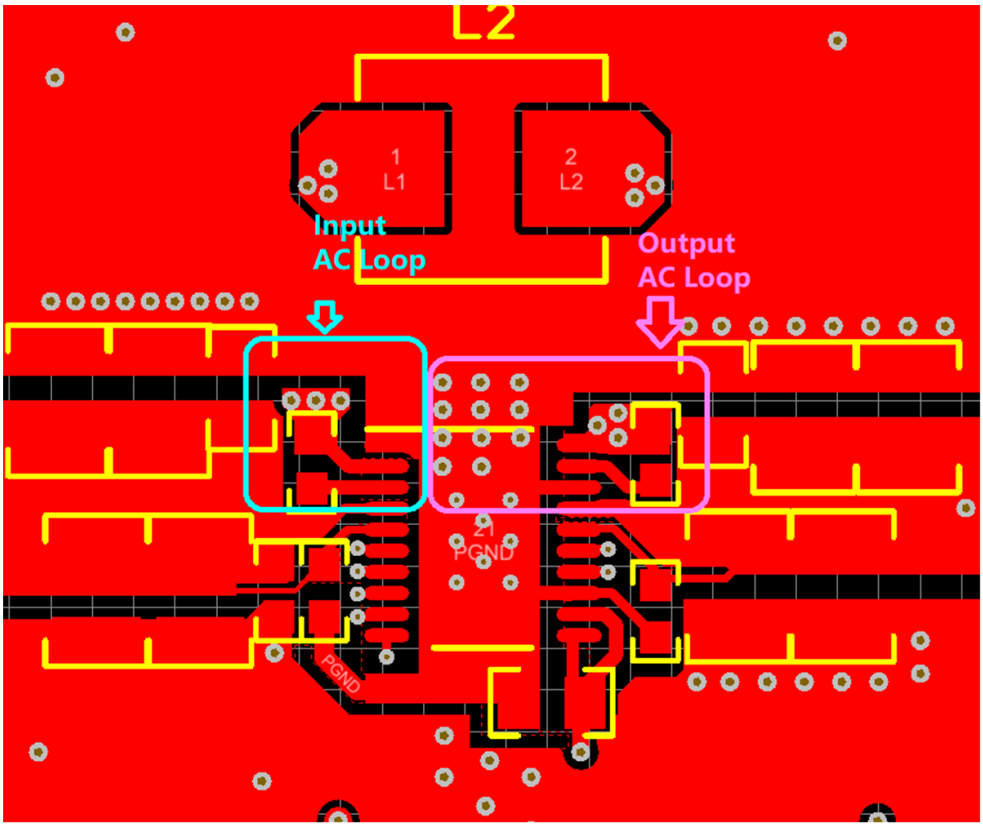

Figure 4. Four-Layer Board With Small Critical AC Loop

These noisy critical loops can be further decreased by moving the main inductor and the bootstrap capacitors to the bottom layer, see Figure 5. This new placement will make the top layer routing quite simple. Layer 2 and layer 3 can be a whole GND copper plane, the bottom layer can route SW and some signal trace. If the EMI performance is highly critical, then the SW and the other signal net can be routed on layer 3, the bottom layer can be a whole GND copper plane.

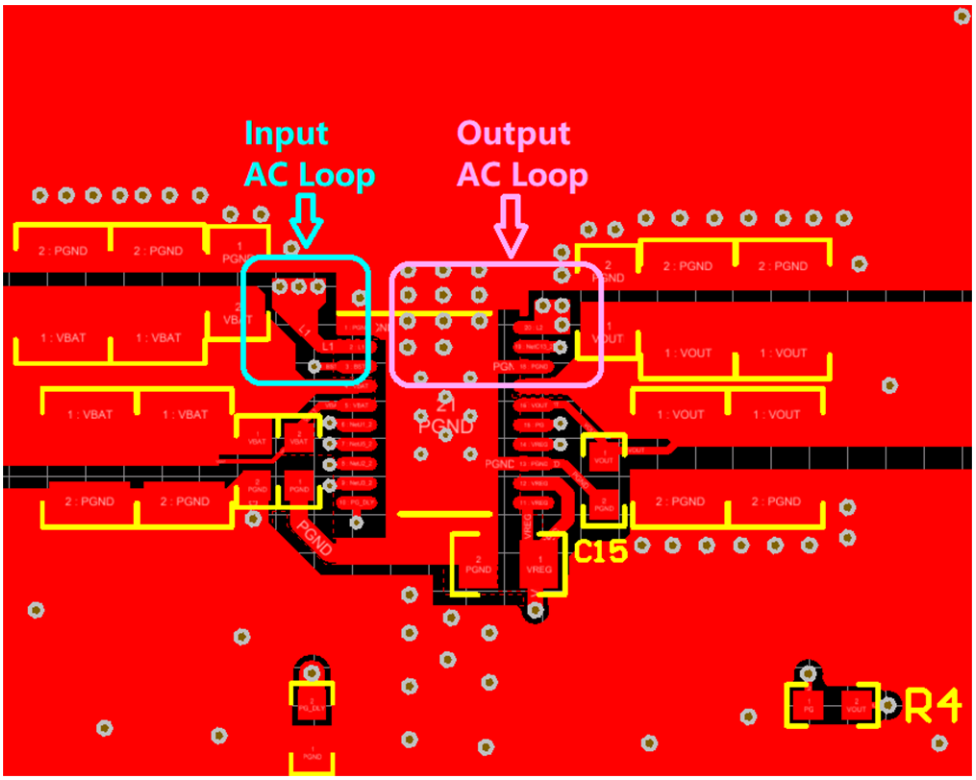

Figure 5. Further Improvement to Decrease the Critical AC Loop

2.4 Separate the PGND and GND

The power switches are connected to the PGND pin. The control circuits are connected to the GND pins. No power current is allowed to follow into the GND (AGND) pin, or the GND pin will be contaminated by the noisy power current and leads to stability issues. Figure 6 shows an example of the GND pin connection. Two GND pins are single-point connected to the PGND pin via the thermal pad. The PGND pin is directly connected with the input and output capacitors with a big copper plane on the top layer. There is no power current flowing through the GND pin, so the GND pin is very quiet.

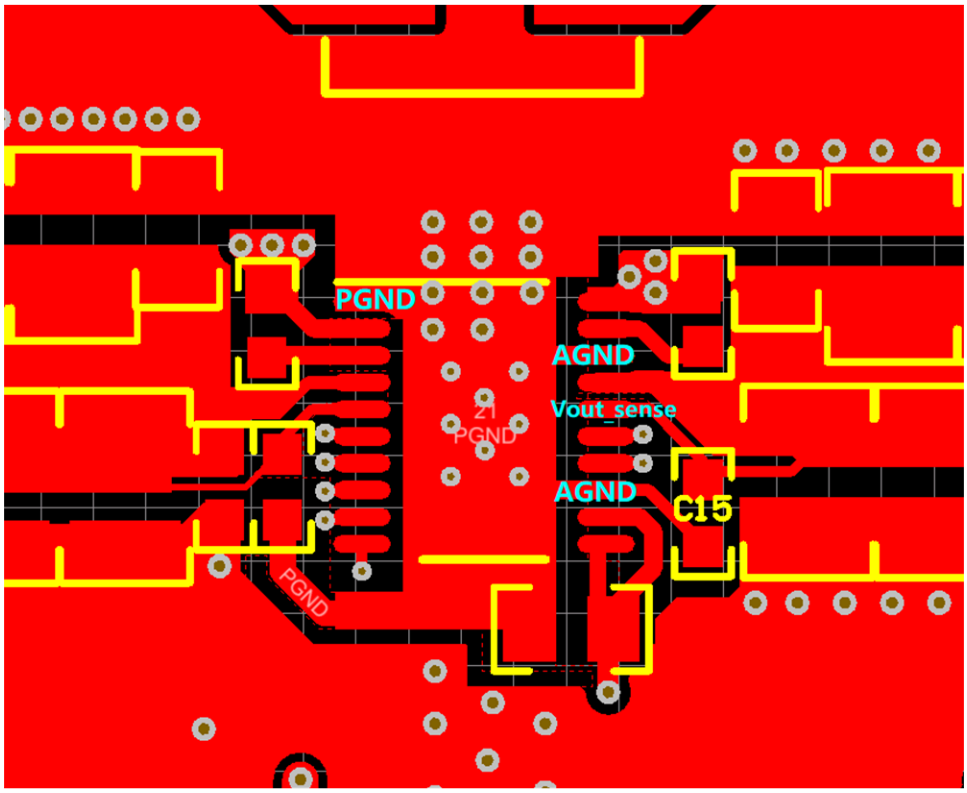

Figure 6. GND Pin Connection

2.5 VOUT_SENSE Pin Connection

The C15 ceramic capacitor is the decoupling capacitor for the VOUT_SENSE pin, this pin is very sensitive. Figure 6 shows the correct way to connect this decoupling capacitor. The VOUT_SENSE net of C15 is connected to the output capacitors with a separate trace, the GND net of C15 is connected to the GND pin of the TPS55165 device nearby. This connection makes sure the sampled out output voltage is a quiet and clean signal.

2.6 VREG and VREG_Q Pin Connections

The C14 ceramic capacitor is the decoupling capacitor for the VREG and VREG_Q pins. VREG voltage is the internal gate-drive supply for the buck-boost power stages. VREG_Q is to generate a reference for the internal control circuit. So the GND net of C14 should be connected with both PGND and AGND net. Figure 7 illustrates an example of the C14 connection.

The GND net of C14 is connected with the PGND pin and AGND pin via thermal pad. A polygon cutout is added between the PGND copper plane and the thermal pad, so that there are no power current flows through C14 while it still connects with PGND and AGND with a very low impedance.

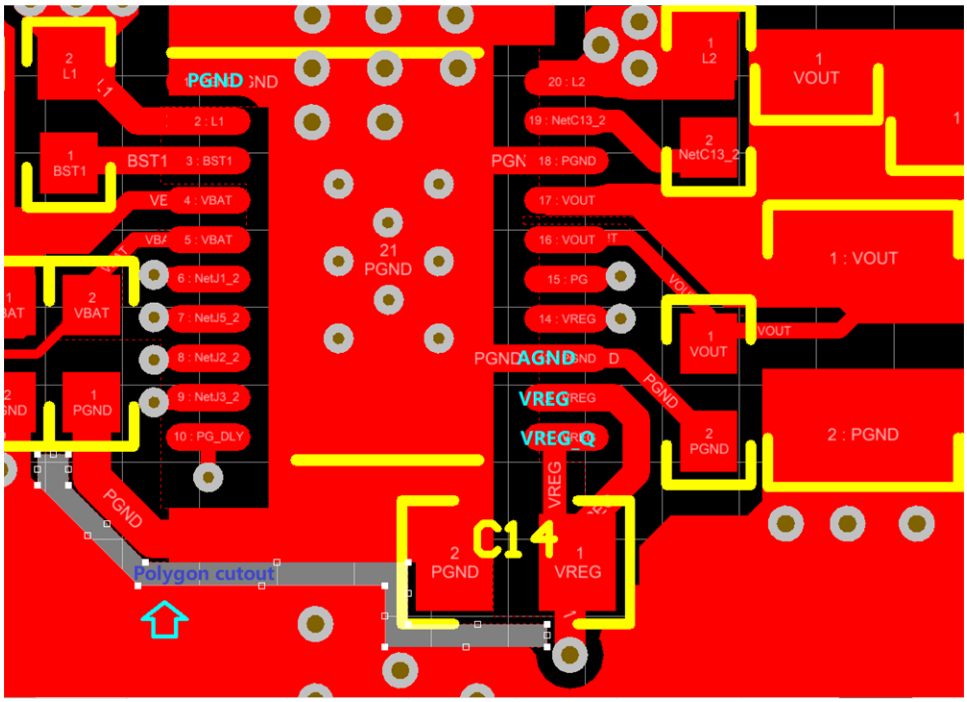

Figure 7. VREG and VREG_Q Connection

3 Summary

This application report describes how to route the TPS55165-Q1 buck boost converter with a 4-layer printed circuit board. Following the placement, connection, and routing instructions in this report ensure the TPS55165-Q1 buck-boost converter will work stably and achieve low EMI performance. A 2-layer board is not recommended in the TPS55165-Q1 application.

4 References

1. Texas Instruments, *TPS5516x-Q1 36-V, 1-A Output, 2-MHz, Single Inductor, Synchronous Step-Up and Step-Down Voltage Regulator Data Sheet*
2. Texas Instruments, *TPS5516xQ1-EVM Evaluation Module for 1-A Single-Inductor Buck-Boost Converter User Guide*

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