Functional Safety Information

TPS7B4250-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS7B4250-Q1 (SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

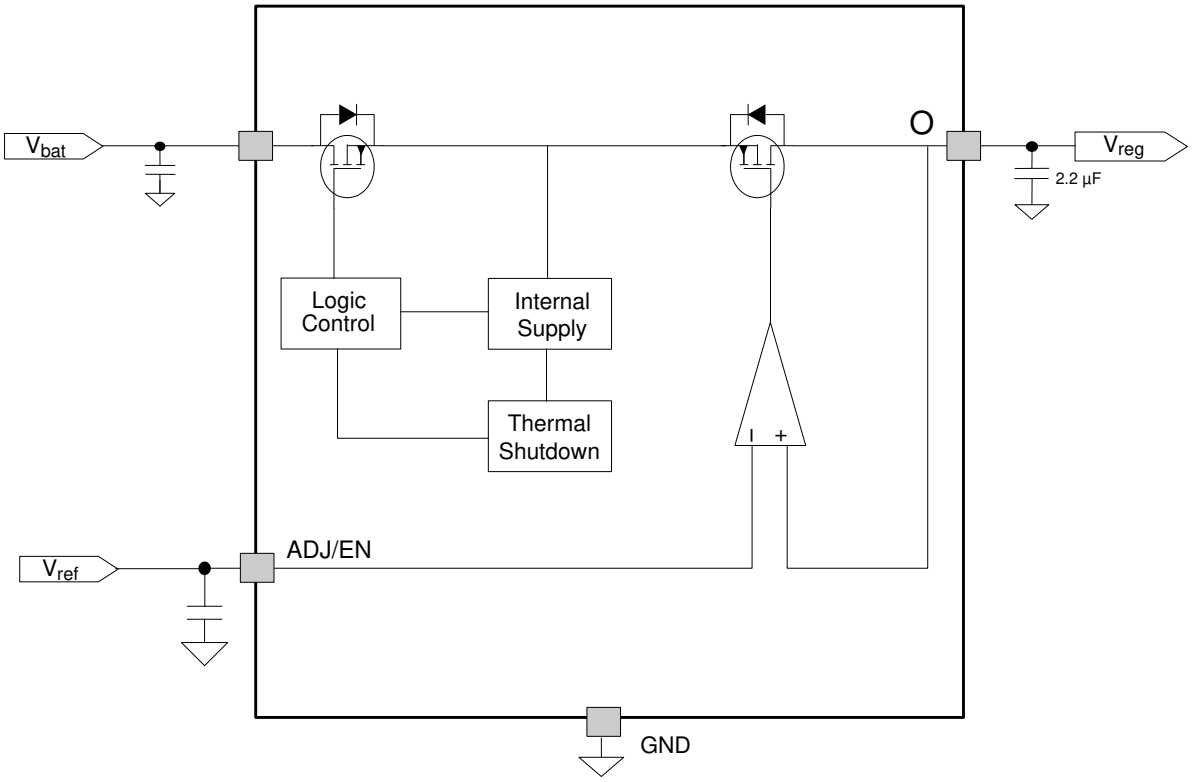

Figure 1-1. Functional Block Diagram

The TPS7B4250-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS7B4250-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	4
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 100 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator ≤ 1 Watt (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B4250-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No OUTPUT (output low)	50%
OUTPUT high (following input)	5%
OUTPUT not in specification	40%
Short circuit, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B4250-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V_{IN} (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS7B4250-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B4250-Q1 data sheet.

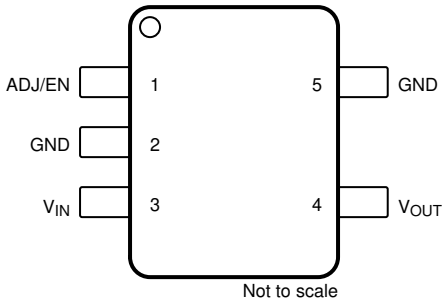

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ADJ/EN	1	The device is disabled, resulting in no output voltage.	B
GND	2	No effect. Normal operation.	D
V_{IN}	3	Power is not supplied to the device. System performance depends on upstream current limiting.	B
V_{OUT}	4	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
GND	5	No effect. Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ADJ/EN	1	$V_{ADJ/EN}$ is undetermined; therefore, regulation is not possible.	B
GND	2	The device is still functional with degraded transient performance.	C
V_{IN}	3	Power is not supplied to the device, resulting in no output voltage.	B
V_{OUT}	4	The device output is disconnected from the load.	B
GND	5	The device is still functional with degraded transient performance.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ADJ/EN	1	GND (pin 2)	The device is forced off.	B
GND	2	V_{IN} (pin 3)	Power is not supplied to the device. System performance depends on upstream current limiting.	B
V_{IN}	3	V_{OUT} (pin 4)	The device has protection for out to in short circuit. Potential damage when V_{IN}exceeds 22 V because this value violates the V_{OUT} absolute maximum.	B/A
V_{OUT}	4	GND (pin 5)	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{IN}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ADJ/EN	1	Potential damage when V_{IN} is greater than 22 V because this value violates the absolute maximum for $V_{ADJ/EN}$.	B/A
GND	2	Power is not supplied to the device. System performance depends on upstream current limiting.	D
V_{IN}	3	No effect. Normal operation.	B
V_{OUT}	4	The device has protection for out to in short circuit. Potential damage when $V_{IN}$is greater than 22 V because this value violates the absolute maximum for V_{OUT}.	B/A
GND	5	Power is not supplied to the device. System performance depends on upstream current limiting.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2019) to Revision A (April 2023)	Page
• Changed document to follow current standards and added FIT and pin FMEA information	2

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265