*Application Report*

# *Stability Analysis and Design of D-CAP2 and D-CAP3 Converter – Part 2: How to Select Feedforward Capacitor*

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**ABSTRACT**

In the previous application report SLVAF11, the method to select output capacitor for D-CAP2/D-CAP3 converters without feedforward capacitor ($C_{ff}$) is introduced. On the basis, the method to select $C_{ff}$ is further studied in this application report. First, the necessity to add a $C_{ff}$ for stability in D-CAP2/D-CAP3 converters with high output voltage is analyzed. Then the impacts of $C_{ff}$ on the converter loop are introduced. Combining the $C_{ff}$ impacts and D-CAP2/D-CAP3 loop characteristics, a method to select $C_{ff}$ for stability is proposed by ensuring -20dB/decade slope at converter loop gain crossover frequency. Compared with other $C_{ff}$ selection methods, the bode plot test results without $C_{ff}$ are not needed in the proposed method, which could help with the overall converter application design. Finally, an example is provided as guidance and the proposed method is verified by experiments.

To be noted, the method proposed in this application report can only be used as a reference material. Due to the simplification in deduction and non-ideal factors in reality, the calculated results will have difference with bench test.

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## 1 Introduction

D-CAP series control schemes are widely used in notebook, server, EP power and many other areas due to the advantages of good dynamic performance and less external components [1-2]. The zero formed by output capacitor ESR is used for loop compensation in the original D-CAP control [3- 4]. For some application with small ESR output capacitor, the zero generated by the internal *ripple injection* circuit can be used for compensation instead of the ESR zero in D-CAP2/D-CAP3 control. In the previous application report SLVAF11, it is introduced that a simplified method for D-CAP2/D-CAP3 converter stability design is to ensure the *ripple injection* zero inside bandwidth [5]. On the basis, the output capacitor selection limits are deducted for application design. However, the bandwidth will decrease with increasing output voltage in D-CAP control loop and the *ripple injection* zero is hard to be kept inside bandwidth. In this condition, the feedforward capacitor, that can provide an additional pair of zero and pole in the loop, can be used to ensure system stability. The detailed analysis and selection method of feedforward capacitor $C_{ff}$ are introduced in this application report.

## 2 Why We Need $C_{ff}$ in High Output Voltage D-CAP2/3 Converter for Stability

The bode plots of D-CAP2/D-CAP3 converters are shown as Figure 2-1. After the LC double poles frequency $\omega_0$ related with inductance and output capacitance, the slope of loop gain can be approximately seen as changing from 0 to -40dB/decade. With the zero injected by the internal *ripple injection* circuit, the slope becomes –20dB/decade at 0dB, which could bring sufficient phase margin [7].

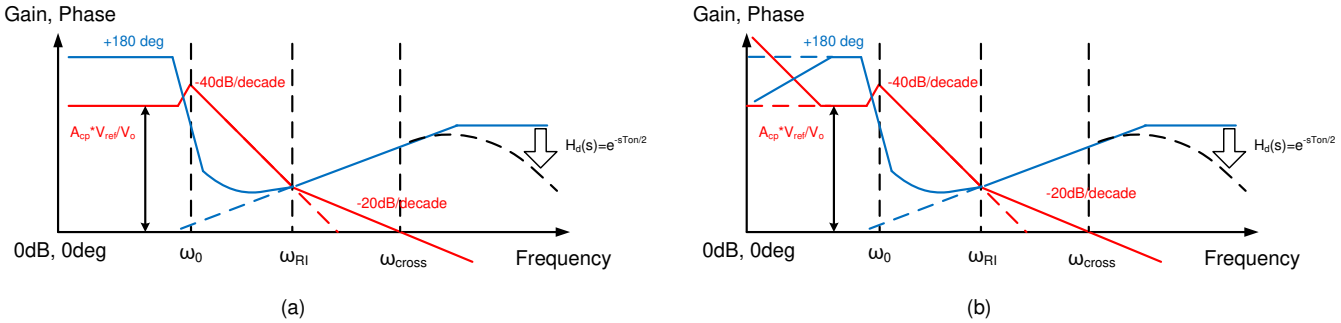


**Figure 2-1. Bode Plot of (a) D-CAP2 (b) D-CAP3 Converter**

For a stable D-CAP2/3 converter, if output voltage is increased with no other changes, the system will tend to become unstable, as shown in Figure 2-2. Since the gain before double poles frequency equals to $A_{cp}*V_{ref}/V_o$, system gain and crossover frequency $\omega_{cross}$ will decrease with increasing $V_o$. If $\omega_{cross}$ becomes lower than the frequency of *ripple injection* zero $\omega_{RI}$, system will have a -40dB/decade slope at 0dB, which may cause insufficient phase margin.

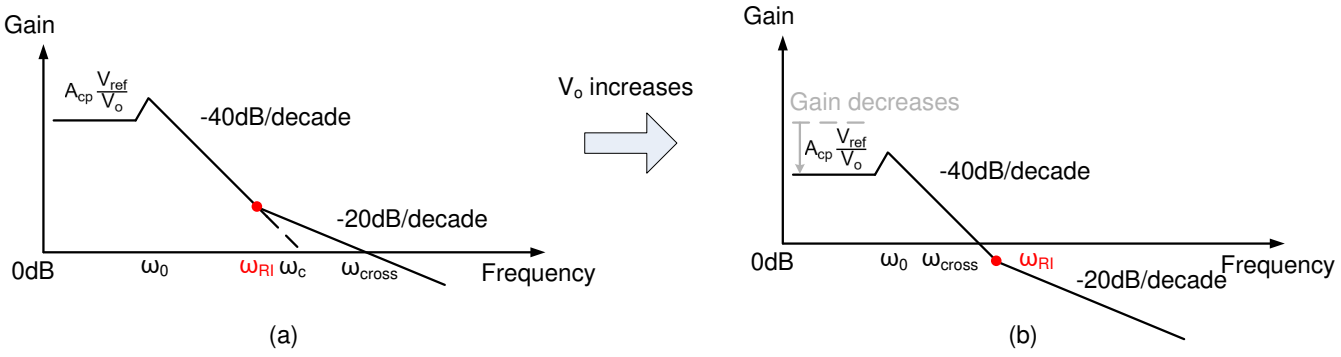


**Figure 2-2. Loop Gain of a D-CAP2 Converter (a) low $V_o$ with -20dB/Decade Crossing (b) high $V_o$ with -40dB/Decade Crossing**

For some D-CAP2/3 converters similar to TPS548D22, the ripple injection zero frequency $\omega_{RI}$ is adjustable with external configuration (sometimes named as *ramp time constant*, the *ramp* here is the *ripple injection*, time constant is the reciprocal of angular frequency). For TPS548D22, the $V_{ref}$ can also be adjusted for different output voltage to change $\omega_{cross}$. Those features can both help to adjust the relation of $\omega_{cross}$ and $\omega_{RI}$ and achieve -20dB/decade crossing.

But for most D-CAP2/3 devices to achieve easy design, the ripple injection zero frequency and reference voltage are fixed. So the LC double poles frequency $\omega_0$ must be increased for bandwidth improvement to ensure -20dB/decade slope at 0dB, as shown in Figure 2-3. However, it can be seen from Equation 1 that the inductance and output capacitance must be reduced to increase LC double poles frequency, which will cause large output ripple and noise. That causes the contradiction between output ripple and stability for D-CAP2/3 converters.

$$\omega_0 = \sqrt{\frac{1+r_L/R_L}{LC_o}} \approx \sqrt{\frac{1}{LC_o}} \quad (1)$$

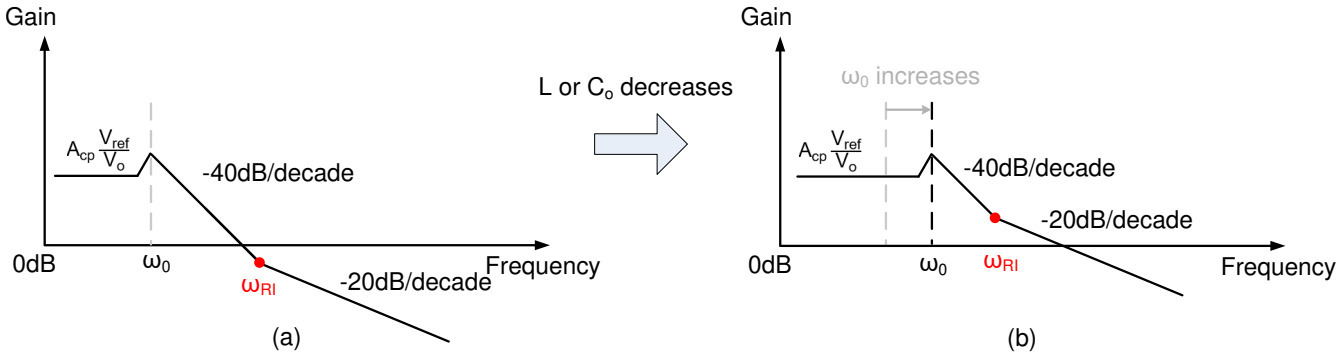


**Figure 2-3. Loop Gain of a D-CAP2 Converter (a) High $V_o$ with -40dB/Decade Crossing (b) Reducing L or $C_o$ for -20dB/Decade Crossing**

In application report SLVAF11, TPS568230 was used as an example to illustrate the stability design method for a 1.5 V $V_o$ low output voltage application. Here the case with 5 V $V_o$ is shown to reflect the contradiction between output ripple and stability in high output voltage application.

The condition for analysis is: $V_{in}$=12 V, $V_o$=5 V, $I_{outmax}$=8 A, $f_{sw}$=600kHz. First, the range of inductance can be got as 1.52uH-3.04uH, according to the principle to limit inductor current ripple as 20%-40% of $I_{outmax}$.

Select inductor 744311220 L=2.2uH. Based on the previous proposed selection method of output capacitor, we could get the limits of $C_o$ as 4.7uF-22.3uF. With the upper limit $C_o$=22.3uF, the output voltage ripple is too large to meet the requirement for lots of application.

It is obvious that reducing L or $C_o$ is just a trade-off solution between output voltage ripple and stability. Compared to that, adding feedforward capacitor $C_{ff}$ is a better solution to ensure converter stability.

# 3 Effects of Feedforward Capacitor on the Loop

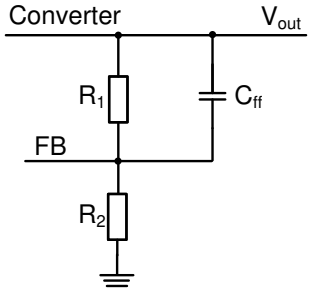


**Figure 3-1. Scheme of Feedback Divider Including Feedforward Capacitor**

The effects of adding feedforward capacitor in the feedback divider are studied in the application report [6]. A feedback divider including $C_{ff}$ is shown as Figure 3-1. $C_{ff}$ will introduce a pair of zero and pole in the converter loop. The angular frequency of the introduced zero and pole are:

$$\omega_z = \frac{1}{R_1 \times C_{ff}} \tag{2}$$

$$\omega_p = \frac{1}{C_{ff}}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{3}$$

The effects of the zero and pole introduced by $C_{ff}$ are shown as Figure 3-2.

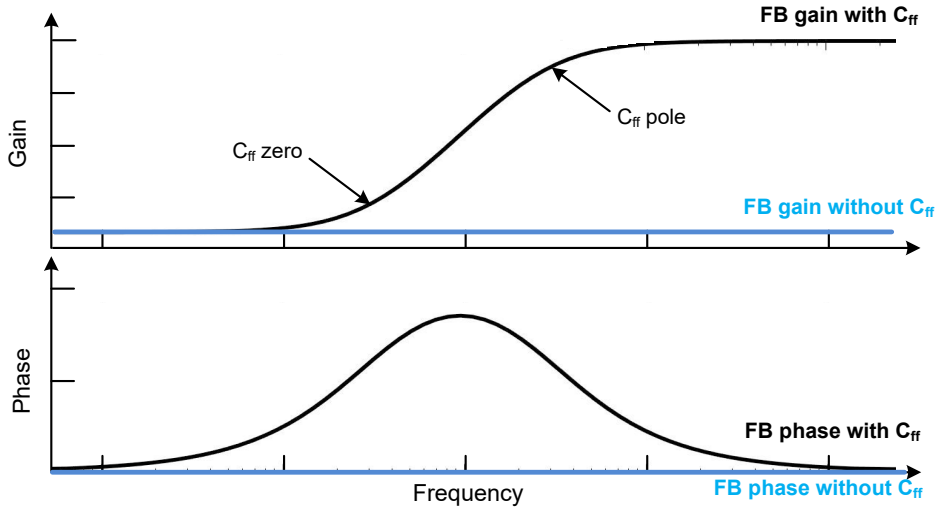


**Figure 3-2. Bode Plot of Transfer Function of FB Divider Including $C_{ff}$**

$C_{ff}$ has both effects on the loop gain and phase. The loop gain is increased to boost bandwidth and optimize transient response. Also, the phase is boosted to increase the phase margin for system stability.

In application notes [2,8], some methods have been proposed to use $C_{ff}$ for phase margin enhancement. But in those methods, the bode plot results without $C_{ff}$ are always needed to get recommended $C_{ff}$ value. That feature makes those $C_{ff}$ selecting methods more applicable in the solution validation process but not in the application design process.

A new method to choose $C_{ff}$ is proposed in this application report. The bode plot results without $C_{ff}$ are not needed to get the recommended $C_{ff}$ value in this method, which makes it more applicable in application design.

## 4 $C_{ff}$ Choose Method

This method is implemented by letting the gain cross 0dB with -20dB/decade slope [7]. To be noted, -20dB/decade gain at 0dB is not a necessary condition for stability. So this method just provides an allowable range for $C_{ff}$ and it doesn't mean the converter will be unstable if $C_{ff}$ exceeds this range.

For the case as Figure 4-1(a) when the *ripple injection* zero frequency $\omega_{RI}$ is larger than bandwidth, we can add the $C_{ff}$ zero $\omega_z$ inside bandwidth, then the loop gain can cross 0dB with -20dB/decade, as shown in Figure 4-1(b).

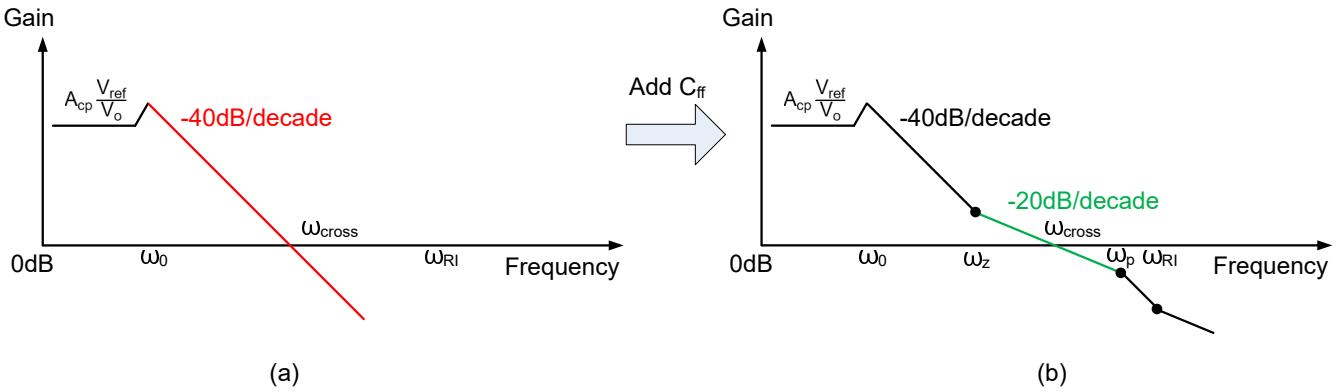


**Figure 4-1. Correct Method to Use $C_{ff}$ by Only Adding the $C_{ff}$ Zero Inside Bandwidth**

In the case as Figure 4-2, the zero and pole introduced by $C_{ff}$ are both added inside bandwidth and the system stability can still be ensured. Although the slope of loop gain becomes -40dB/decade again after the pole $\omega_p$, the loop gain increasement with $C_{ff}$ makes the bandwidth increased and the $\omega_{RI}$ becomes smaller than bandwidth. A -20dB/decade crossing is achieved and system will have enough phase margin.

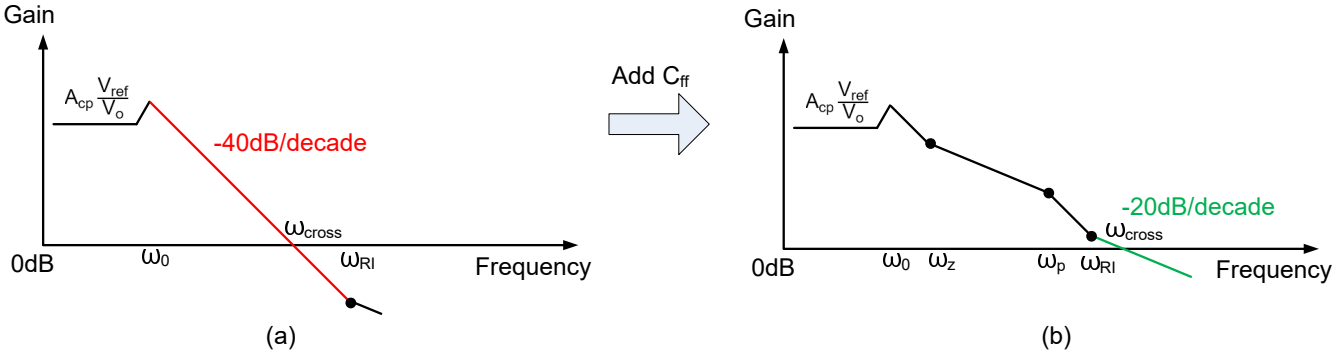


**Figure 4-2. Correct Method to Use $C_{ff}$ by Adding Both the $C_{ff}$ Zero and Pole Inside Bandwidth**

In the case as Figure 4-3, both the zero and pole introduced by $C_{ff}$ are inside bandwidth, but the ripple injection zero frequency $\omega_{RI}$ is still larger than the bandwidth. At this condition, the loop gain will still cross 0dB with -40dB/decade, which can't ensure the system phase margin.

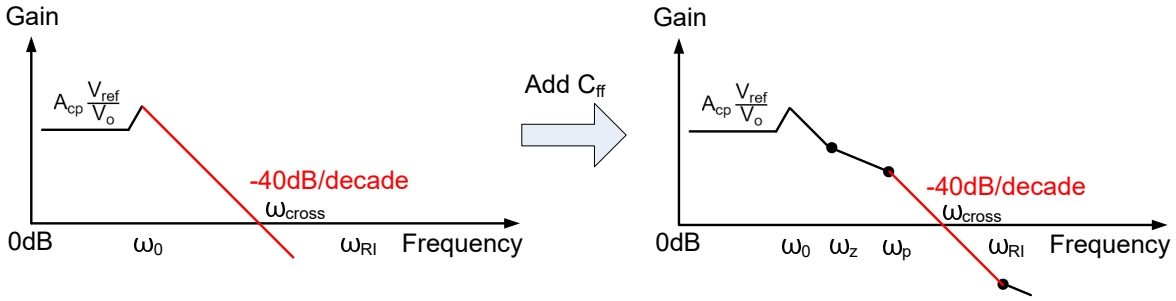


**Figure 4-3. Incorrect Method to Use $C_{ff}$ by Adding Both the $C_{ff}$ Zero and Pole Inside Bandwidth**

Above all, we can conclude two restrictions to achieve a stable state with -20dB/decade crossing after adding feedforward capacitor:

**A. $\omega_z<\omega_{cross}$; B. avoiding the condition as Figure 4-3.**

First we could deduct the limit for restriction A. Based on Figure 4-4, we can know that $\omega_z<\omega_{cross}$ can be achieved by ensuring $\omega_z<\omega_c$. The expression of $\omega_c$ is as equation (4). With equations (2) and (4), the lower limit of $C_{ff}$ is derived as equation (5).

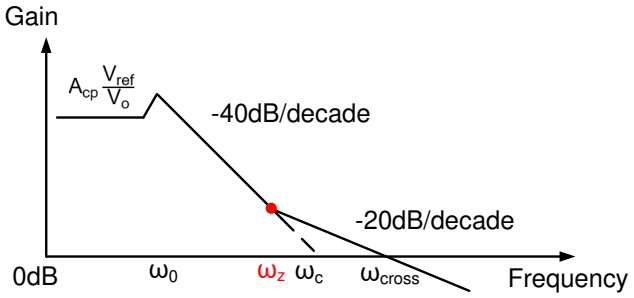


**Figure 4-4. D-CAP2 Converter Loop Gain When Adding $\omega_z< \omega_{cross}$**

$$\omega_c=\sqrt{A_{cp}\frac{V_{ref}}{V_o}}\times\omega_0 \tag{4}$$

$$C_{ff}>\frac{1}{R_1\omega_0}\sqrt{\frac{V_o}{A_{cp}V_{ref}}} \tag{5}$$

To get the limits for restriction B, we could know that Equation 6 corresponds the condition as Figure 4-3. Then the restriction B to avoid that condition corresponds to Equation 7.

$$20\lg(A_p)>0dB \quad \text{and} \quad \omega_{RI}>\omega_{cross} \tag{6}$$

$$20\lg(A_p)\le 0dB \quad \text{or} \quad \omega_{RI}\le\omega_{cross} \tag{7}$$

where $A_p$ is the amplitude of gain at $\omega_p$.

To get the expressions of $A_p$ and $\omega_{cross}$, we can first get the relation between gain and frequency as Equation 8 through Equation 10.

$$\frac{20\lg\left(A_{cp}\frac{V_{ref}}{V_o}\right)-20\lg(A_z)}{\lg(\omega_0)-\lg(\omega_z)}=-40dB/decade \tag{8}$$

$$\frac{20\lg(A_z)-20\lg(A_p)}{\lg(\omega_z)-\lg(\omega_p)}=-20\text{dB/decade} \tag{9}$$

$$\frac{20\lg(A_p)-0}{\lg(\omega_p)-\lg(\omega_{cross})}=-40\text{dB/decade} \tag{10}$$

Substituting Equation 2 through Equation 3 into Equation 8 through Equation 10, the expressions of $A_p$ and $\omega_{cross}$ can be received as Equation 11 and Equation 12.

$$A_p=\frac{A_{cp}V_{ref}\omega_0^2}{V_o\omega_z\omega_p} \tag{11}$$

$$\omega_{cross}=\omega_p\sqrt{A_p} \tag{12}$$

Substituting Equation 11 and Equation 12 into Equation 7, we can get Equation 13 as equation for restriction B.

$$C_{ff}\le\sqrt{\frac{V_oLC_o(R_1+R_2)}{A_{cp}V_{ref}R_1^2R_2}}\quad\text{or}\quad\omega_{RI}\le\sqrt{\frac{A_{cp}V_{ref}(R_1+R_2)}{V_oLC_oR_2}} \tag{13}$$

Combine the Equation 5 for restriction A and Equation 13 for restriction B, Equation 14 and Equation 15 are the limits for $C_{ff}$.

$$C_{ff}>\frac{1}{R_1\omega_0}\sqrt{\frac{V_o}{A_{cp}V_{ref}}},\quad\text{if}\,\omega_{RI}\le\sqrt{\frac{A_{cp}V_{ref}(R_1+R_2)}{V_oLC_oR_2}} \tag{14}$$

$$\frac{1}{R_1\omega_0}\sqrt{\frac{V_o}{A_{cp}V_{ref}}}<C_{ff}\le\sqrt{\frac{V_oLC_o(R_1+R_2)}{A_{cp}V_{ref}R_1^2R_2}},\ \text{if}\,\omega_{RI}>\sqrt{\frac{A_{cp}V_{ref}(R_1+R_2)}{V_oLC_oR_2}} \tag{15}$$

At the meantime, the bandwidth after adding $C_{ff}$ should also be limited under $1/3*f_{sw}$. Since it is hard to give a unified method for the estimation of bandwidth and phase margin after adding $C_{ff}$, it is suggested to verify with the help of simulation model or bench loop test results.

## 5 Application Design Example of D-CAP2/D-CAP3 Converter with $C_{ff}$

Figure 5-1 is the design flow chart for D-CAP2/D-CAP3 converter with $C_{ff}$. All the inductance and capacitance used in choosing $C_{ff}$ are effective value considering degrading.

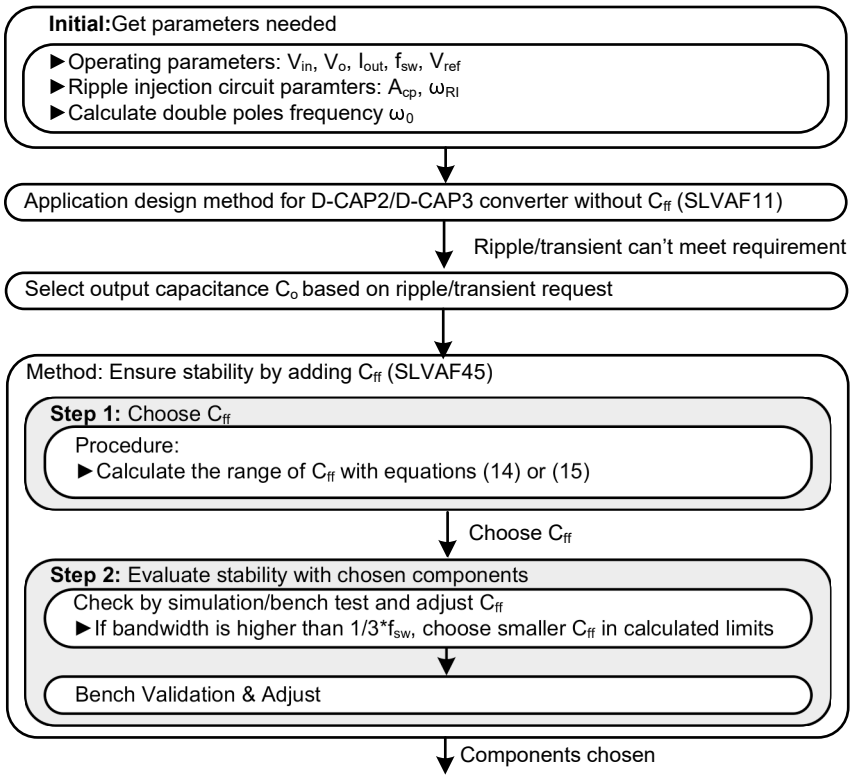


**Figure 5-1. Design Flow Chart of D-CAP2/D-CAP3 Converter with $C_{ff}$**

Here TPS568230 is used as an example to illustrate the design method for a 5V $V_o$ application. The condition of example is $V_{in}$=12 V, $V_o$=5 V, $I_{outmax}$=8 A, $f_{sw}$=600kHz.

First select voltage divider resistors $R_1(R_{top})$=220 kΩ and $R_2(R_{bottom})$=30 kΩ to achieve 5 V output with 0.6 V reference voltage. Then, same as the analysis mentioned in section 2, the range of inductance can be got as 1.52 uH-3.04 uH, according to the principle to limit inductor current ripple as 20%-40% of $I_{outmax}$. And we can select 744311220 inductor and its effective inductance with 8 A current is about 1.8 uH.

About 180uF output capacitance are used to meet output ripple requirement. Here the 885012108012 MLCC are used. With about 52.5% degrading at 5 V bias for the 47 uF capacitance, the effective capacitance of each MLCC is about 22.35 uF. Capacitance of 8 parallel MLCCs are 178.8 uF.

Then the method is used to select $C_{ff}$. As $A_{cp}$=29.3 and $\omega_{RI}$=270 k for TPS568230, we can get $C_{ff}$>44 pF according to Equation 14 and Equation 15. Here we can choose 120 pF $C_{ff}$.

# 6 Experimental Verification

The bode plot test result with 180 uF output capacitors and no $C_{ff}$ is shown in Figure 6-1 for comparison. It could be seen that the phase margin is 17.228 degree. The crossover frequency is about 18.54 kHz.

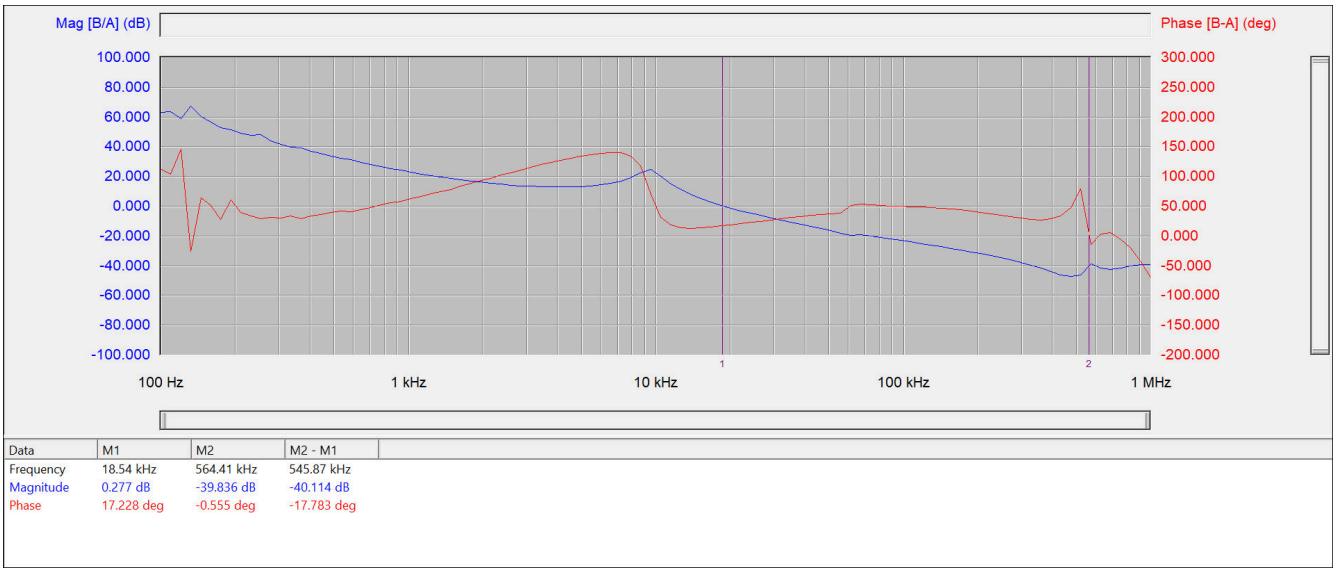


**Figure 6-1. Experimental Result without Cff**

Figure 6-2 shows the validation result with chosen $C_{ff}$=120 pF using the proposed method. It can be seen that bandwidth is increased from 18.54 kHz to 47.22 kHz, while the phase margin is increased from 17.228 degree to 75.353 degree. Both dynamic performance and stability can be enhanced with the 120 pF $C_{ff}$. That proves the effectiveness of the proposed method.

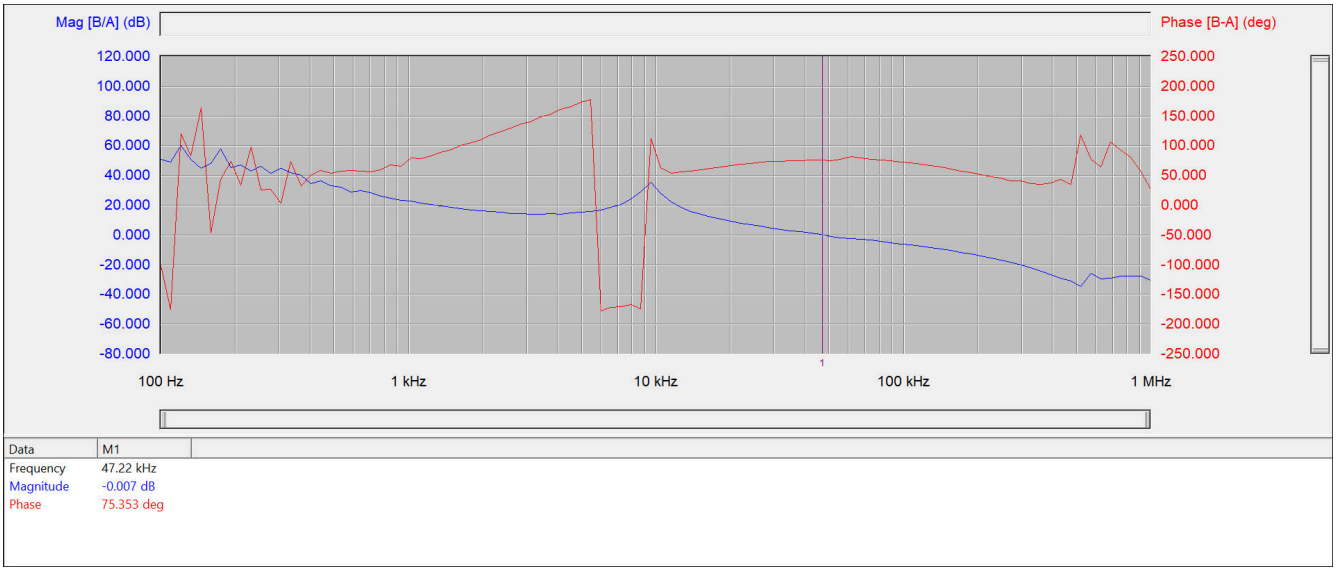


**Figure 6-2. Experimental Verification of Proposed Method**

## 7 Conclusion

A selection method of feedforward capacitor is proposed in this application report for D-CAP2/D-CAP3 converters based on loop stability analysis. First, the necessity of adding $C_{ff}$ in some application with high output voltage is analyzed. Then the impacts of the $C_{ff}$ on the converter loop is introduced and a method to choose $C_{ff}$ for stability is proposed by ensuring -20dB/decade gain slope at gain crossover frequency. Compared with previous methods, the bode plot test results without $C_{ff}$ aren't needed to get recommended $C_{ff}$ value, which makes the method more applicable in application design process. Finally, a detailed flow chart is given to help designing application of D-CAP2/D-CAP3 converter. The proposed method is verified by experiments.

## 8 References


1. *Frequency Domain Analysis of Fixed On-Time with Bottom Detection Control for Buck Converter*, M. Lin, T. Zaitsu, T. Sato, and T. Nabeshima, IEEE IECON2010, pp.475-479
2. Texas Instruments, *D-CAP2TM Frequency Response Model based on frequency domain analysis of Fixed On-Time with Bottom Detection having Ripple Injection*, application report.
3. Texas Instruments, *Loop Stability Analysis of Voltage Mode Buck Regulator with Different Output Capacitor Types – Continuous and Discontinuous Modes*, application report.
4. *Understanding and Applying Current-Mode Control Theory*, application report.
5. Texas Instruments, *Stability Analysis and Design of D-CAP2 and D-CAP3 Converter - Part 1: How to Select Output Capacitor*, application report.
6. Texas Instruments, *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor*, application report.
7. *Feedback Control of Dynamic Systems*, Gene F. Franklin, J. David Powell, Abbas Emami-Naeini.
8. Texas Instruments, *Designing a Feedforward Capacitor for LMR140x0*, application report.


## 9 Appendix A

For TPS568230 $I_{outmax}$=8 A, $V_{ref}$=0.6 V. $C_o$ in the table are effective value considering degrading. The large $C_{ff}$ as 1000 pF can be allowed from loop stability view, but it could inject more high frequency noise into feedback and also might affect converter operation. The $C_{ff}$ theoretical calculation methods must be used combined with real situation and bench test results.

**Table 9-1. Validation Results for the Proposed Method**

| $V_{in}$ (V) | $V_o$ (V) | $f_{sw}$ (kHz) | $R_{top}/R_{bottom}$ | $L_{limits}$ (uH) | $L_{choose}$(uH) | $C_o$ (uF) | $C_{ff}$ limit | $C_{ff}$ choose (pF) | $PM_{test}$ (deg) |
|---|---|---|---|---|---|---|---|---|---|
| 6 | 2.5 | 600 | 95 kΩ/30 kΩ | 0.76-1.52 | 1 | 200 | $C_{ff}$>56pF | 70 | 81.4 |
| | | | | | | | | 1000 | 50.8 |
| 6 | 3.3 | 600 | 90 kΩ/20 kΩ | 0.77-1.55 | 1 | 200 | $C_{ff}$>68 pF | 80 | 80.2 |
| | | | | | | | | 1000 | 47 |
| 18 | 2.5 | 600 | 95 kΩ/30 kΩ | 1.12-2.24 | 1.5 | 200 | $C_{ff}$>69 pF | 82 | 80 |
| | | | | | | | | 1000 | 63 |
| 18 | 3.3 | 600 | 90 kΩ/20 kΩ | 1.4-2.81 | 2.2 | 200 | 100-236 pF | 110 | 83 |
| | | | | | | | | 220 | 75 |
| 18 | 5 | 600 | 220 kΩ/30 kΩ | 1.88-3.76 | 2.2 | 200 | 51-147 pF | 62 | 72 |
| | | | | | | | | 140 | 77 |

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