Application Report

How to Best Use TPS62903 for a Given Application Requirement

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ABSTRACT

The TPS62903 device is a highly-efficient, small, and flexible synchronous step-down DC/DC converter that is easy to use. It provides power designers a lot of flexibility and freedom to adjust certain parameters and features to meet the need of the specific application. This application note is divided into two segments. The first segment walks through how best to configure the TPS62903 for applications with limited space. This section explores how to select the right operating mode and the needed features to achieve the smallest possible solution size by minimizing the need for external components. The second segment of this report provides a detailed analysis on how to configure TPS62903 for best efficiency. This section explores some major power loss factors and discusses how to reduce their losses by making some design tradeoffs and choices.

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Trademarks

1 Applications With Limited Area

Real estate is a luxury in some applications where every inch is needed and utilized. At the same time, power demand increases as more functionalities are added in new designs with higher power requirements. For example, a decade ago smartphones were twice the size as the ones of today and had very limited functionality. More functionalities are added and the performance is dramatically increased with better cameras, more memory, better speed, faster touch screen, better audio, more battery life, faster charging, and so on. Power system designers are left with no other option but to make the best of limited board space with the highest efficiency possible. The TPS62903 gives the designer lots of flexibility to configure it for the smallest application size possible. The following section discusses the possible adjustments needed to achieve that.

1.1 Best TPS62903 Configuration to Reduce Size

The TPS62903 is a very flexible synchronous step-down DC/DC converter. If its flexibility is used in the right way, power designers can get the smallest application size possible. This section discusses how to best configure TPS62903 for smaller possible area . When talking about the solution size of a buck converter, there are three elements to consider:

1. **The DC/DC buck converter package and pinout**: The TPS62903 device is available in a small nine-pin VQFN package measuring 1.50 mm × 2.00 mm. The device footprint covers only 3 mm^2 which helps on reducing the total solution size. The TPS62903 has an optimized pinout for easy layout and placement of external components. Having the sensing pins on the bottom side of the package allows placing the sensing components away from power traces and the switch node. Having VIN on the left side and SW and VOUT on the right side of the package makes it easy to place the input capacitor, the inductor, and output capacitor near the package efficiently.
2. **The inductor:** The inductor is one of the biggest external components on the buck power supply design. Choosing the right inductor for the application is a big contributor to reduce the solution size. A selectable switching frequency of 2.5 MHz or 1.0 MHz allows the use of small inductors. The device is designed for a nominal 1 µH inductor. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency, transient response, cost, and inductor size. Smaller values than 1 µH will cause a larger inductor current ripple which causes larger negative inductor current in forced PWM mode at low or no output current. Therefore, they are not recommended at large voltages across the inductor as it is the case for high input voltages and low output voltages. Low output current in forced PWM mode causes a larger negative inductor current peak which can exceed the negative current limit. There are many 1 µH small inductors that come as small as 2.0 mm × 1.6 mm size.
3. **Other components**:
   - **Input capacitor:** Only one 10 µF input capacitor is needed. Since the TPS62903 supports input voltages between 3–17 V, a 25 V rating is enough to support the full input voltage range. If the input voltage can be limited, then a lower voltage rating capacitor can be used. Typically, the designer should choose a voltage rating of about 50% above the maximum voltage the capacitor will see at any given time. An 0805-size, low-ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and should be placed between VIN and GND as close as possible to those pins.
   - **Output capacitor:** Only one 22 µF output capacitor is recommended. The DCS-Control architecture of the device allows for a tiny ceramic output capacitor to be used. The DC rating of the capacitor can be as low as 10 V since the V_{OUT} is limited to 5.5 V.
   - **Soft start capacitor:** The device provides the user the option to program the start-up time of output voltage. However, to save space, the user can use the pre-programmed soft start time and leave the pin open.
   - **Feedback loop:** This is one of the advantages of the TPS62903. There is no need for external feedback loop as long as the needed output voltage is one of the 16 provided options in the *VSET Selection Table* of the *TPS62903, 3-V to 17-V, High Efficiency and Low IQ Buck Converter in 1.5-mm × 2-mm Data Sheet*. By selecting the VSET option using the MODE/S-CONF pin, and picking one of the 16 options using the resistor from VSET to GND, it allows the user to save space and improve solution accuracy. The VSET option has better accuracy as it does not include the accuracy of the external feedback resistors. For typical E96 resistors, the accuracy is about ±1%, plus an additional ±0.9% of the reference, so the total accuracy of the external feedback option is ±1.9%. On the other side, if VSET is used, then only ±1.25% of the internal loop accuracy needs to be taken into consideration.

- **Precision enable (EN):** The TPS62903 does not require any pullup resistor. The user can connect the EN pin directly to VIN, this reduces the need for another external component. The precise enable input allows the user to program the undervoltage lockout by adding a resistor divider to the input of the enable pin.
- **Power Good (PG):** This is an optional feature too. If the PG pin is not used, then it can be open to save space. This feature is used to indicate whether the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level.

1.2 Design Example

This section describes how to best design a buck converter to support 6 V input supply, and step it down to 1.2 V output and support up to 3 A. The same steps can be taken to design it for other design requirements.

Selection of components:

- **Inductor:** The 6 V_{IN} to 1.2 V output voltage allows the use of 0.68 µH inductor with reasonable inductor current ripple if **2.5 MHz** is chosen. A small size 2.0 mm × 1.6 mm 0.68 µH inductor can be used for this such as the "*DFE201612E-R68M#*" from Murata.
- **Input capacitor:** Input voltage requirement for this design is only 6 V. Therefore, 10 µF with only 10 V rating can be used.
- **Output capacitor:** The recommended output capacitor in the data sheet is 22 µF. In this example, the output is set to 1.2 V, therefore only 6 V voltage rating can be used.
- **Feedback:** 1.2 V V_{OUT} is one of the 16 options VSET can support, to save area and achieve better accuracy, the internal voltage divider can be used in this example. Internal feedback should give a total system accuracy of ±1.25% versus 1.9% if external feedback is used.
- **Mode and Smart Configuration:** A low V_{OUT} can tolerate low switching frequency with good inductor current ripple. Both 1 MHz or 2.5 MHz can be chosen. However, the goal is to have the smallest solution size possible, and 2.5 MHz allows the use of a 0.68 µH inductor with acceptable ripple. Power save mode is preferred to provide high efficiency at light loads. Thus, 26.1 kΩ is connected on the Mode/S-CONF pin to GND.
- **EN, Soft start, and PG:** If there is no need for soft start capacitor and Power Good features, these pins can be left floating. The EN pin can be connected directly to VIN. These add some additional BOM savings.

Here is a suggested schematic for this example:

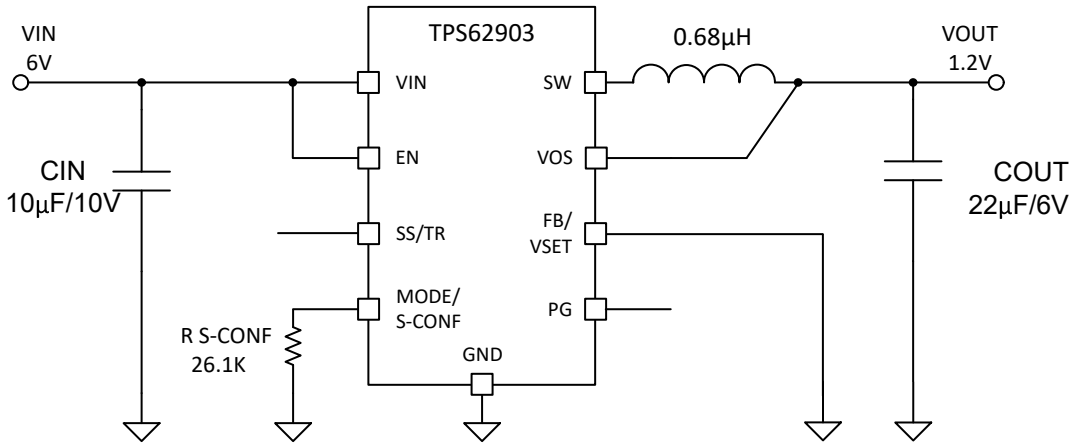

Figure 1-1. Design Example Schematic

Table 1-1. Components PCB Area

Component	Size and Rating	Area
CIN	10 µF, 10 V, 0805, X7R	2.5 mm^2
COUT	22 µF, 6 V, 0805, X7R	2.5 mm^2
Inductor	0.68 µH, 2.0 mm × 1.6 mm × 1.2 mm, 33 mΩ	3.2 mm^2
Mode/S-CONF resistor	26.1 kΩ, ±1%, 0402	0.5 mm^2
TPS62903	Buck Converter, 1.5 mm × 2.0 mm	3.0 mm^2
Routing	Estimated Routing Area	13.3 mm^2
Total Area	Routing plus components	25 mm^2

Figure 1-2 provides a layout example. CIN, COUT, and the inductor L are placed as close as possible to the pin of the device. The SW node trace is kept small for better noise performance. Vias are added on GND, VIN, and VOUT traces to help improve thermal dissipation of the board.

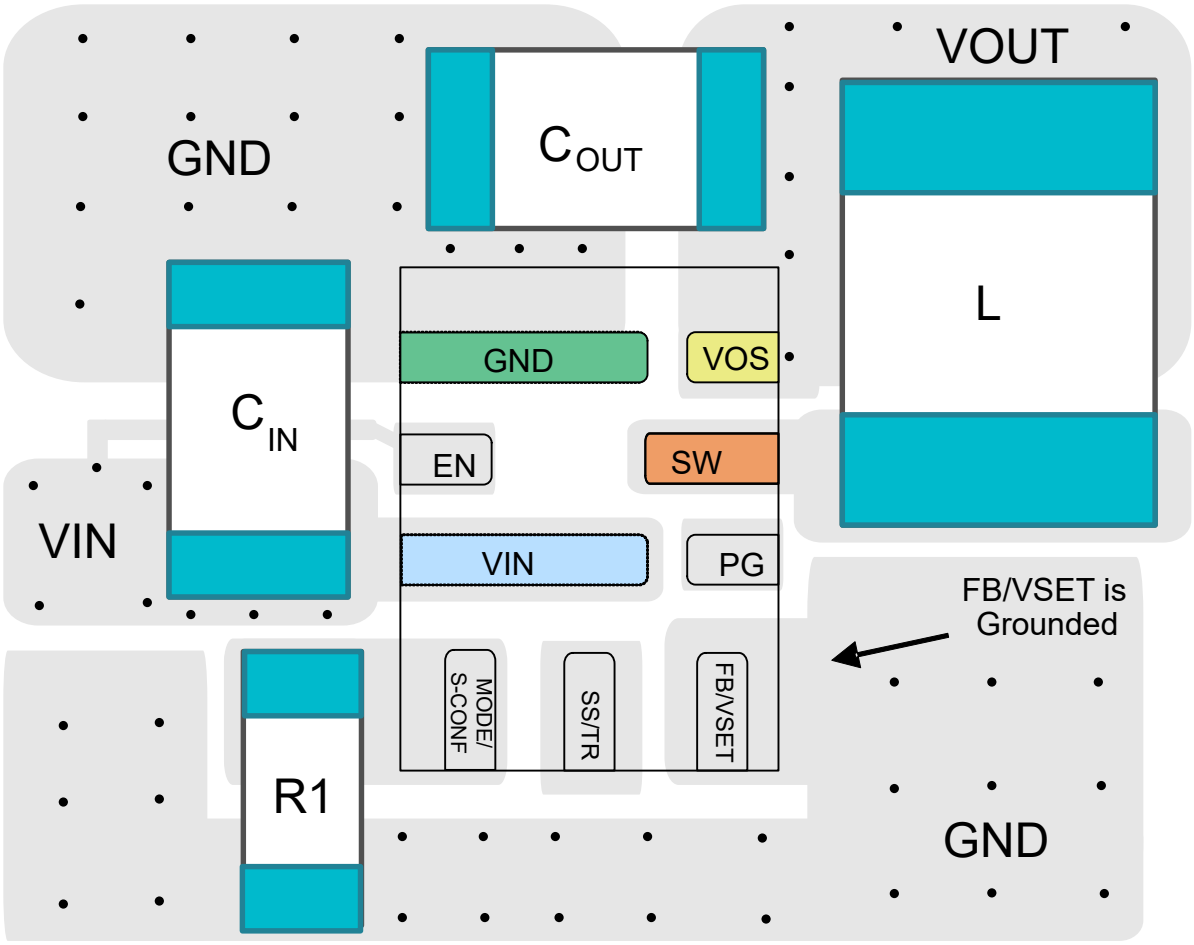

Figure 1-2. Layout Example

2 Applications With High Efficiency and Thermal Requirement

Switching regulators are best known for their good efficiency. However, there are many power loss factors that contribute into the total losses; therefore, they impact the efficiency. To select the highest efficiency design, it is helpful to understand the basic mechanisms of power loss. This section explores some major power loss factors and discusses how to reduce their losses by making some design tradeoffs and choices.

2.1 Conduction Losses in the MOSFET

The conduction loss in the MOSFET inside the buck converter is the power loss due to the on-resistance ($R_{DS(ON)}$) of the high-side FET and low-side FET as they conduct current. As the high-side FET is on and the low-side FET is off, the conduction loss of the high-side FET can be estimated from the output current, on-resistance, and on-duty cycle (D). As the high-side FET is off and the low-side FET is on, the conduction loss of the low-side FET can be estimated from the output current, on-resistance, and off-duty cycle (1-D). Use Equation 1 and Equation 2 to estimate the power loss on both the high-side and low-side FETs. Equation 1 and Equation 2 provide a good estimate of the FET conduction power losses and how the $R_{DS(ON)}$ contributes to efficiency:

$$Conduction\_Loss\_H\_FET = IOUT\_rms^2 \times RDSON\_H \times D \quad (1)$$

$$Conduction\_Loss\_L\_FET = IOUT\_rms^2 \times RDSON\_L \times \left(1 - D\right) \quad (2)$$

D is duty cycle and can be calculated as VOUT/VIN. Choosing a converter that has low $R_{DS(ON)}$ is key to improve efficiency of the system. The TPS62903 has very low $R_{DS(ON)}$, the high-side FET on resistance is 62 mΩ and the low-side FET on resistance is only 22 mΩ. This helps on the reducing the conduction loss.

2.2 Conduction Losses in the Inductor

The same as Section 2.1, the conduction losses in the inductor are caused by the resistive element of the inductor as the current flows through the inductor. The resistive element of the inductor is known as DCR of the inductor, typically provided in the data sheet, and it is generated by the windings that form the inductor. The conduction loss in the inductor can be estimated in the same way as for the FET, see Equation 3:

$$Conduction\_Loss\_Inductor = IOUT\_rms^2 \times DCR \quad (3)$$

In this report, DCR loss estimation is good enough to understand the conduction losses. In addition to the losses caused by the resistive element of the inductor, there are core losses determined by the magnetic properties of the inductor as well as AC resistance of the inductor (ACR). The calculation of the core and ACR losses are too complex for the purpose of this application, so they are not described here.

2.3 Switching Losses in the MOSFET

The switching losses mostly occurring when the FETs are turning ON and OFF. A loss is generated during the transition (the rising and falling transitions). The switching-loss on the high-side FET is calculated with Equation 4:

$$SW\_H\_Loss = 0.5 \times VIN \times IOUT \times (t\_rise + t\_fall) \times Fsw \quad (4)$$

where

- t_rise is the rise time of the switch node voltage
- t_fall is the fall time of the switch node voltage
- Fsw is the switching frequency on the converter.

As Equation 4 shows, the switching frequency, rise and fall time have a direct impact on the switching losses. When selecting the switching frequency of the TPS62903, it is always good to consider using the lowest setting, in this case, 1 MHz with *Power Save Operation Mode* (Auto PFM/PWM). In this mode, the switching frequency decreases linearly with the load current maintaining high efficiency. The losses in the low-side FET can be estimated in the same manner.

2.4 Losses in the Input and Output Capacitors

Several losses can be generated in the capacitor including series resistance, leakage, and dielectric loss. In this report, these losses are simplified into a general loss model as equivalent series resistance (ESR). The power loss in the capacitor is calculated by multiplying the ESR by the square of the RMS value of the AC current flowing through the capacitor. Use Equation 5 to estimate the power losses in the input and the output capacitor:

$$P\_Loss\_Capacitor = Icap\_rms^2 \times ESR \quad (5)$$

The RMS current into the input capacitor is typically proportional to the output current and the input and output voltages, it can be estimated using Equation 6:

$$ICIN\_rms = IOUT \times \frac{\sqrt{(VIN - VOUT) \times VOUT}}{VIN} \quad (6)$$

The output capacitor output current can be calculated using RMS value of the inductor current ripple. It can be estimated using Equation 7:

$$ICOUT\_rms = \frac{\Delta IL}{2\sqrt{3}} \quad (7)$$

Selecting a low-ESR multilayer ceramic capacitor (MLCC) is recommended to reduce these losses.

2.5 Analysis and Recommendations

Throughout this report, there are other losses that were not taken in consideration such as reverse recovery loss of body diode, output capacitance loss of MOSFET, dead time loss, gate charge loss, and IC operation loss. All of these contribute to a certain extent to the total losses. However, our focus in this report is on mid-voltage (3 V to 17 V input), 0.5 MHz to 3 MHz switching frequencies, up to 3 A, 0.4 V to 5.5 V output voltage. For that, the majority of the losses are coming from conduction loss in the high-side MOSFET, conduction loss in the low-side MOSFET, switching-loss in the high-side MOSFET, conduction loss in the inductor, and conduction loss in the input and output capacitor. Looking at the equations provided in the previous sections, the takeaway from this is as follows:

- The $R_{DS(ON)}$ of the high and low side FETs of the converter needs to be as small as possible. There is a trade off for that, as the $R_{DS(ON)}$ becomes smaller, silicon area tends to be bigger and more expensive. There is a balance between cost and $R_{DS(ON)}$. TPS62903 provides a balance between cost and $R_{DS(ON)}$ value. It is 62 mΩ for high-side FET and 22 mΩ for low-side FET and provides a very good efficiency at both high and low load.
- The switching frequency is another important factor and needs to be taken into consideration. Higher switching frequencies lead to higher switching losses. However, if the switching frequency is reduced too much, the inductor current ripple increases with it and thus will require a bigger inductance. A bigger inductor comes with cost, size, and higher DC resistance. Higher DC resistance affects the inductor power loss as described in the previous sections. A good balance between the switching frequency, inductor current ripple, inductance, size, and cost all has to be weighted equally to find the most favorable conditions. In our analysis, a good range of the inductance for the TPS62903 is found at anything between 0.68 µH to 2.2 µH depending on Fsw, V_{IN}, and V_{OUT}.
  1. The 0.68 µH is recommended for:
     - Low V_{OUT} < 1 V applications for 1 MHz
     - Low V_{IN} < 10 V applications for 2.5 MHz
  2. The 1 µH is recommended for:
     - Low V_{OUT} < 1.5 V applications for 1 MHz
     - All voltages at 2.5 MHz
  3. The 2.2 µH recommended for both 2.5 MHz and 1 MHz. Lower frequency provides better efficiency in most cases.
- Using the TPS62903 MODE/S-CONF pin, the user has the option to select Forced Pulse Width Modulation (FPWM) Operation or Auto Pulse Frequency Modulation/ Pulse Width Modulation (Auto PFM/PWM) Operation. In the FPWM mode, the switching frequency variation is well controlled and limited. This is good

for filtering the switching noise as the switching frequency variation is limited. However, the efficiency at light load will be inferior than in Auto mode. This is because, in Auto PFM/PWM, the switching frequency decreases linearly with the load current maintaining high efficiency at light load. See Figure 2-1 to compare the efficiency between the two modes.

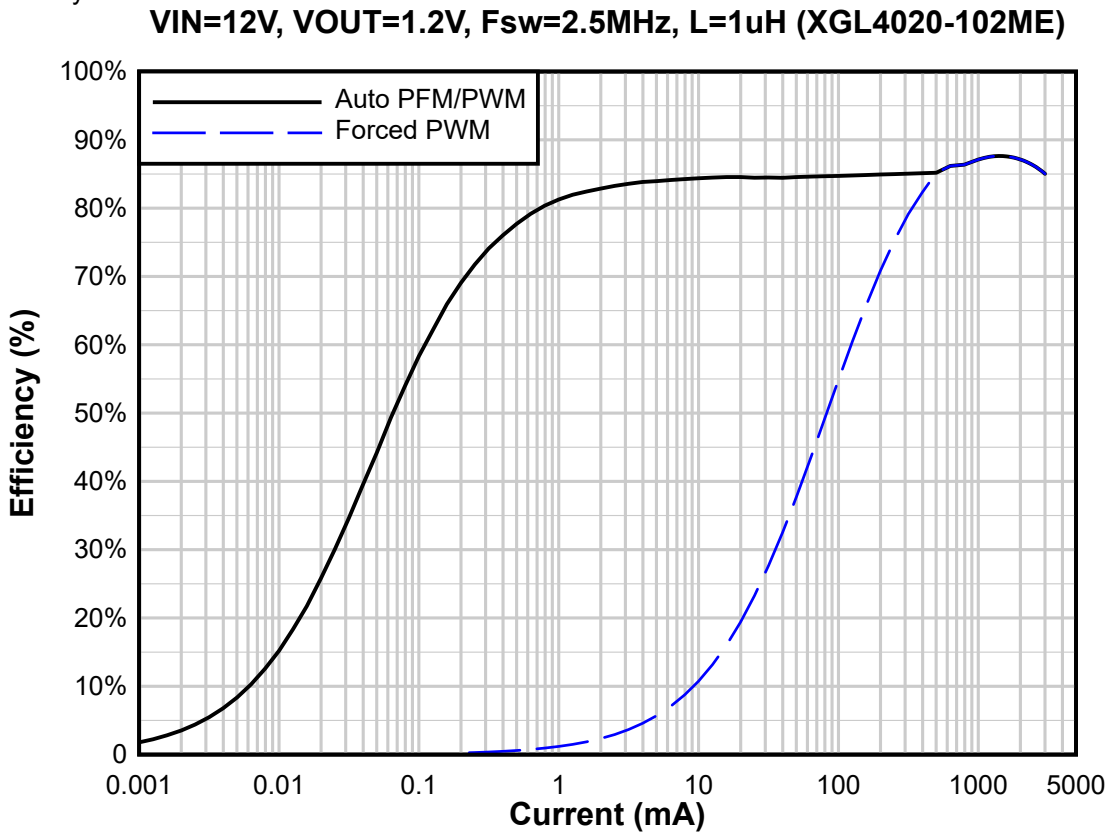

Figure 2-1. Efficiency Comparison at Auto PFM/PWM vs FPWM

- Lower the DCR of the inductor. For 0.68 µH to 2.2 µH inductance range, there is a wide variety of inductors to choose from, and the trade off is the cost and the size. Lowering the DCR typically comes in bigger packages and costs more. It is recommended to use 10 mΩ to 30 mΩ DCR inductors for best efficiency and they come with reasonable package size and cost.
- Lower the output and input capacitor ESR. It is recommended to choose a low-ESR multilayer ceramic capacitor (MLCC) and should be placed as close as possible to the device pins.
- Lower quiescent current of the device helps on the light load efficiency. This is not very helpful in heavy load as other losses are more dominant. In power save mode, the TPS92903 has only 4 µA quiescent current.

3 Conclusion

The TPS62903 can be configured to support the smallest solution in the industry. This is possible due to the flexibility and the low external components requirement of the device. Only one 22 µF output capacitor and one 10 µF input capacitor are required. The enable function does not require a pullup resistor. The internal feedback allows to save the external feedback resistors while improving the system accuracy. The flexibility to adjust the switching frequency allows the use of a small inductor size. In addition, the device comes in a small package size. Finally, the TPS62903 can be configured for best efficiency by selecting the right switching frequency and the best fitted inductor for a given application requirement.

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