Application Note

TPS61381-Q1 Schematic and Layout Guideline

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ABSTRACT

TPS61381-Q1 is a bidirectional boost converter/buck charger designed for back up battery applications such as TBOX or e-call. Schematic design, proper external components selection and board layout is critical for a successful design. This application note details how to route the TPS61381-Q1 to achieve correct function, stable operation, and good thermal and low EMI performance.

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Trademarks

1 Introduction

The TPS61381-Q1 bi-directional boost converter and buck charger is designed for back up battery applications, such as TBOX, E-call. A well-designed schematic and PCB layout is fundamental to a successful system design of any DC/DC or AC/DC power converter. An optimized layout leads to better EMI performance, better thermal performance, and good stability performance within a relatively smaller design size. So an optimized layout means higher reliability, lower cost, and faster release time to market. This application note gives out the TPS61381-Q1 bi-directional boost converter/buck charger schematic and layout guideline. Under the guidance of this application note, the customers can achieve the above goals simply with a 4-layer PCB. The main content includes identification of the schematic notice, layout critical switching loops, power-stage component placement, power circuit, and signal circuit routing, AGND and PGND connection, power and GND copper plane design.

2 TPS61381-Q1 Schematic Guideline

2.1 GND Connection

TPS61381 features in high current limit, fast start-up strategy to make sure the system voltage can be taken over instantly when a power failure is detected. The current can reach up to 25A (Set by I2C) during boost start-up. Vout changes by I2C or short circuit protection-reboot conditions. So GND connection is very important to avoid switching noise form affecting the IC. There is a risk that the IC internal circuit can lose control or even sustain damage if AGND is not connected correctly. The typical schematic is shown in Figure 2-1.

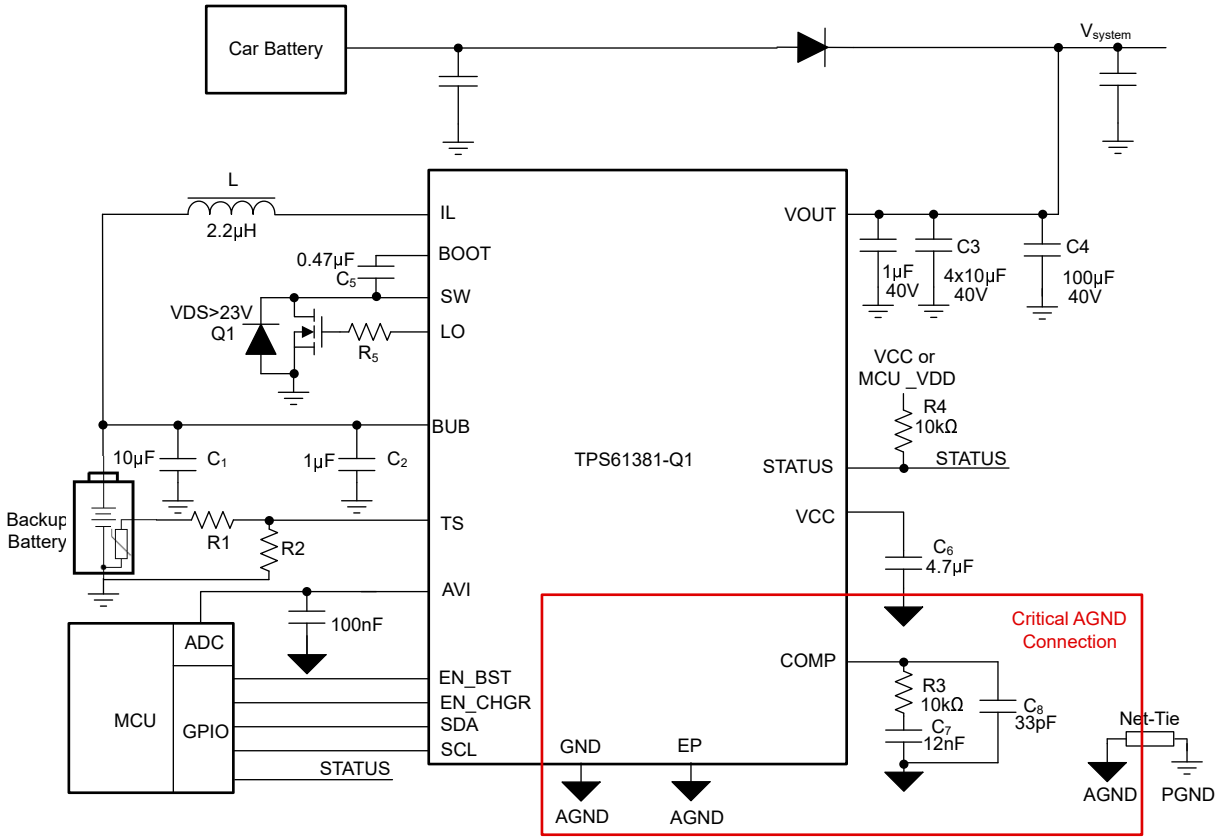

Figure 2-1. TPS61381-Q1 GND Connection

Make sure that there is a separate AGND from PGND and connect VCC, COMP, AGND pin, and the thermal pad to AGND.

AGND must be connected to PGND by a single point (net-tie, 0Ω resistor or wire with 10mil width). Do not connect AGND with PGND by a wide polygon.

2.2 Driver Design

TPS61381-Q1 adjusts the driver speed by gate resistor (R_5). While 1Ω is enough for most MOSFETs, apply a larger resistance (1-2Ω) if the Qgd is below 3nC.

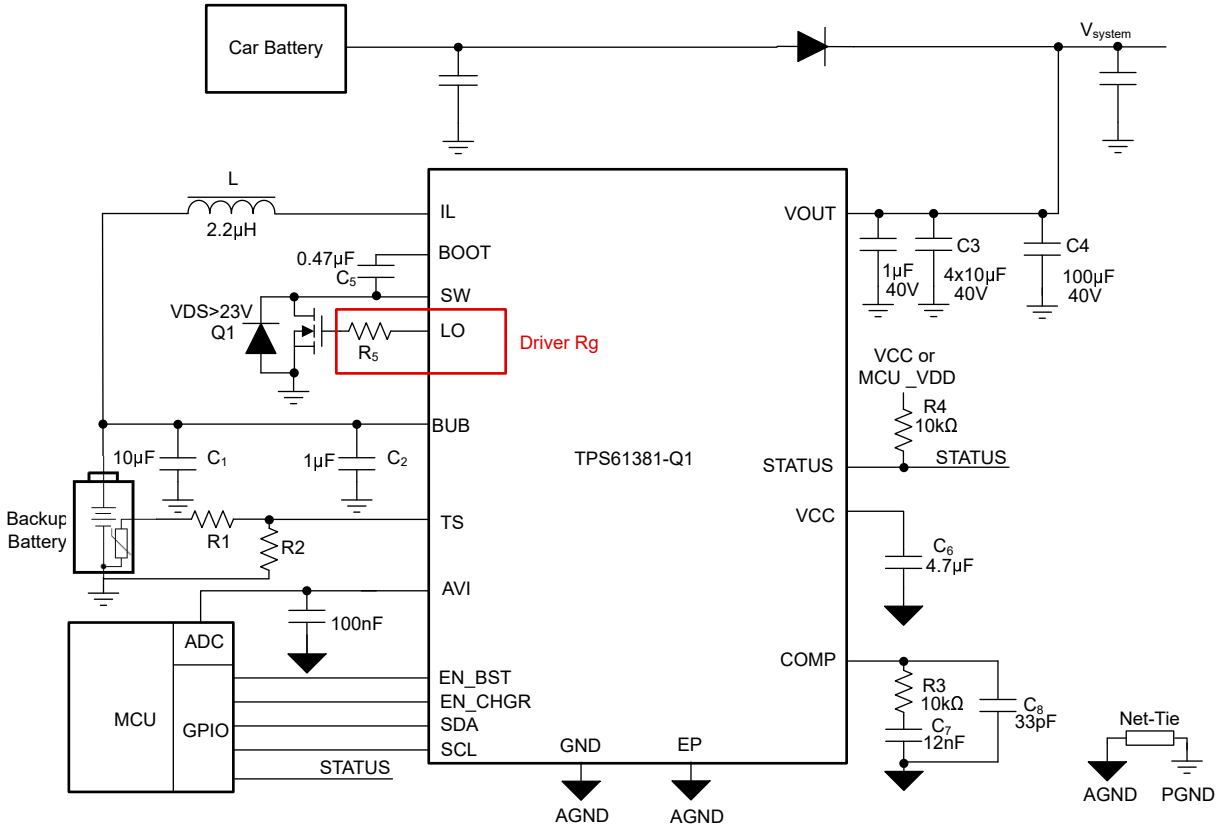

Figure 2-2. TPS61381-Q1 Driver Design

Do not apply less than 1Ω of resistance if the MOSFET has Qgd over 10nC. Slow driver speed can lead to lower efficiency and even power-FETs shooting-through.

R_5 must withstand thermal heat generated by driver loss, so do not select a small package for R_5. Driver loss can be calculated by:

$$P_{gloss} = Q_g V_{CC} f_{sw} \quad (1)$$

where V_{CC} can be calculated as 5V.

2.3 IO Configuration

The digital inputs needs to be pulled up by the MCU power rail. Do not connect to the TPS61381 VCC or Vout.

AVI pin requires a decouple capacitor. The cap can be placed either near the IC or near the MCU ADC (100nF is sufficient).

The STATUS pin is an open drain output that can be pulled up by TPS61381 VCC or MCU_GPIO_VDD.

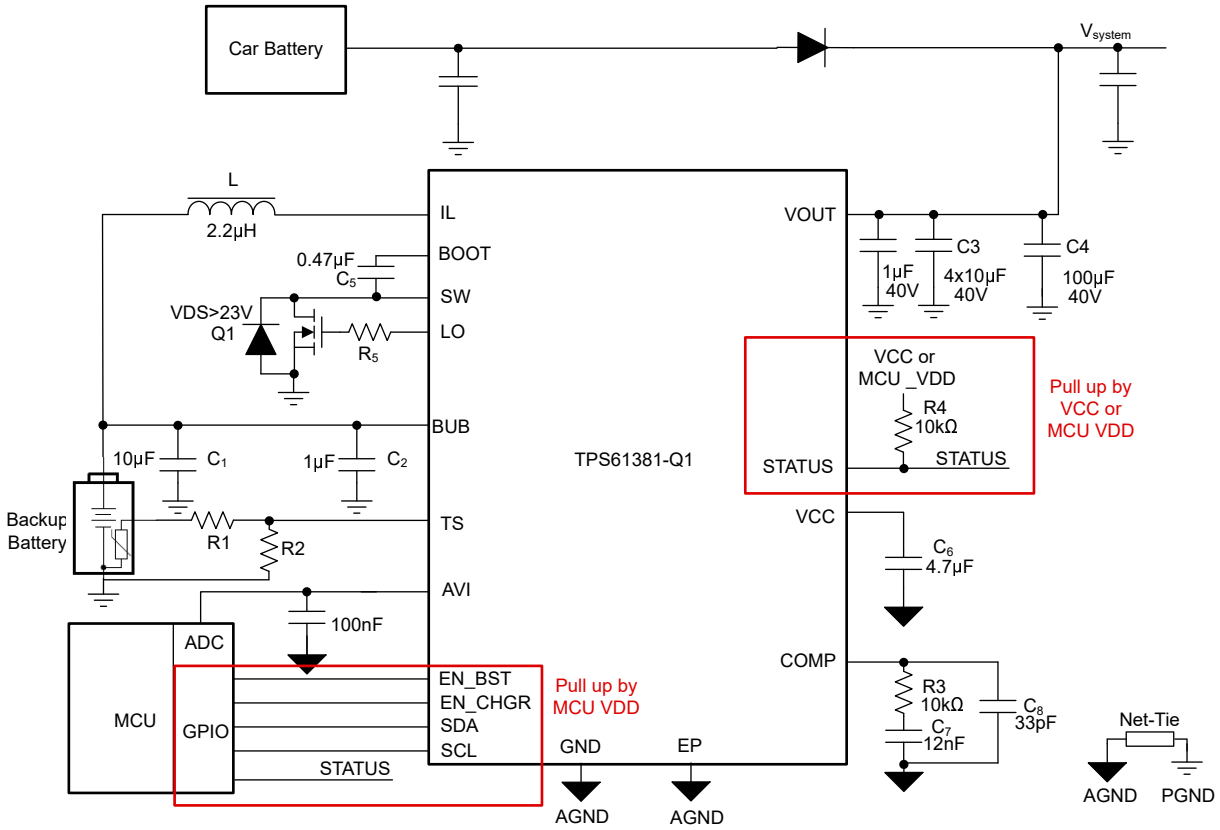

Figure 2-3. TPS61381-Q1 IO Configuration

2.4 Output Capacitor

TPS61381 needs at least 100uF local total output capacitance. TI recommends both MLCC and electrolytic capacitor placed in parallel

Electrolytic capacitors has large ESR and is ineffective for filtering high frequency ripple and switching noise. Make sure the MLCC effective capacitance at Boost Vout target is over 40uF. The MLCC capacitance needs further increase if the electrolytic capacitors has large ESR over 500mΩ. Note that ESR of electrolytic capacitor can increase by over 10 times under low temperature condition and can seriously affect loop stability. Make sure low temperature ESR is considered when calculating loop stability (View Section 2.5 for loop stability calculation).

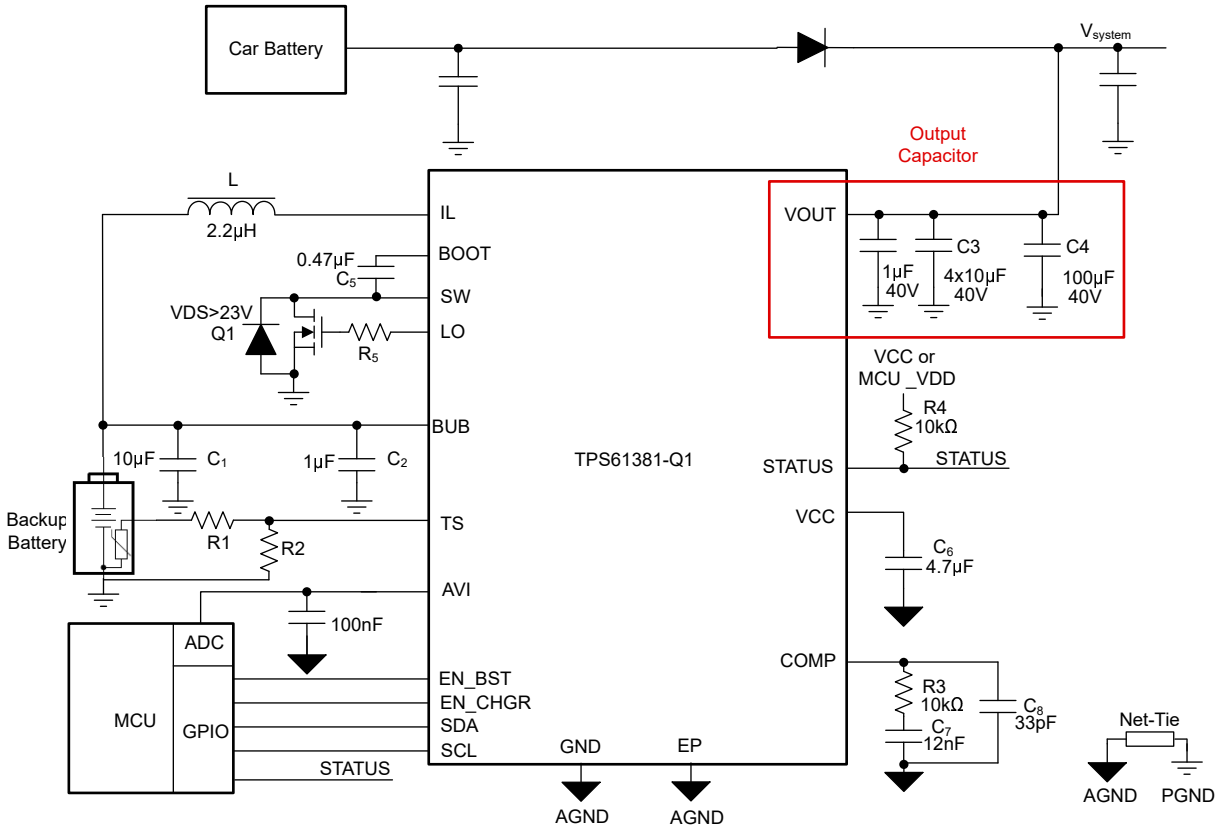

Figure 2-4. TPS61381-Q1 Output Capacitor

MLCCs has DC-bias derating that significantly reduce the effective capacitance when a DC-voltage is applied. Check the DC-bias curve at boost Vout target voltage when calculating the capacitance.

2.5 Compensation Design

The TPS61381-Q1 requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network, comprised of resistor R3, and ceramic capacitors C7 and C8, is connected to the COMP pin. Compensation parameter must be calculated case by case. The following section gives an example about how to calculate the compensation network parameters with the selected inductor and output capacitor.

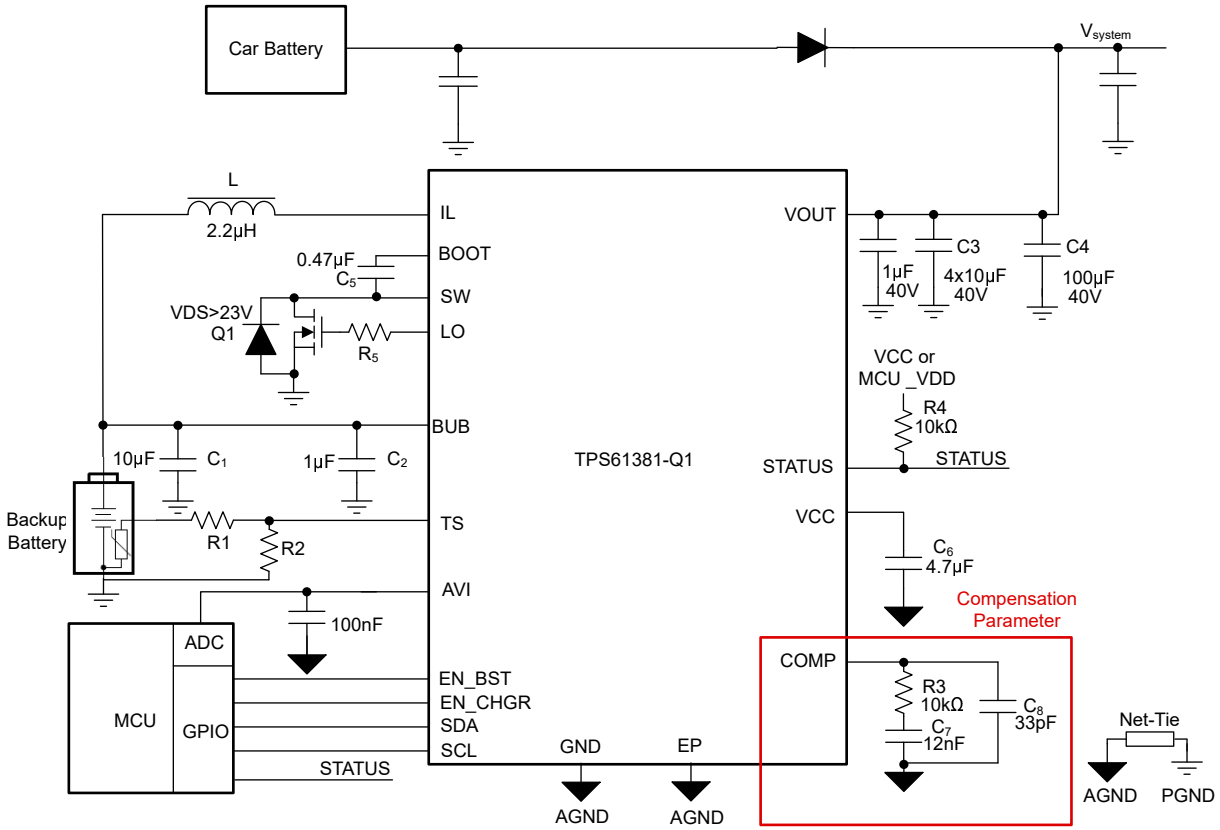

Figure 2-5. TPS61381-Q1 Compensation Design

2.5.1 Small Signal Analysis

The TPS61381-Q1 uses the fixed frequency peak current mode control with an internal adaptive slope compensation to avoid subharmonic oscillation. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by L and C_{OUT}, to a single-pole system, created by R_{OUT} and C_{OUT}. The single-pole system is easily used with the loop compensation. Figure 2-6 shows the equivalent small signal elements of a boost converter.

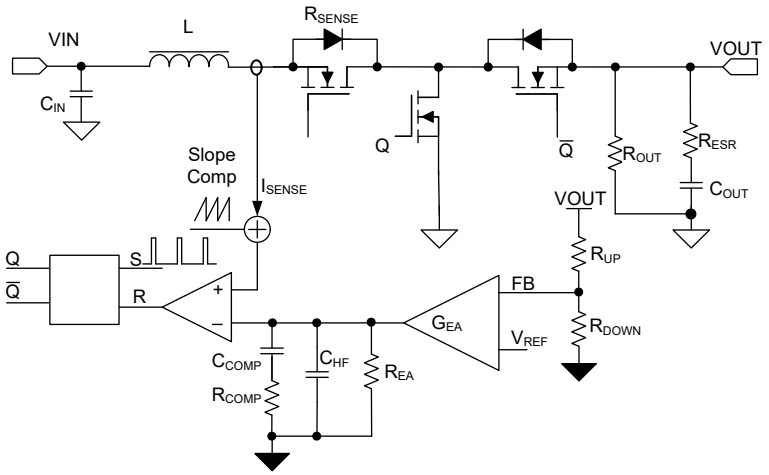

Figure 2-6. TPS61381-Q1 Control Equivalent Circuitry Model

The small signal of power stage can be shown by:

$$K_{PS}(s) = \frac{R_{out}(1-D)}{2R_{sense}} \times \frac{\left(1+\frac{s}{2\pi \times f_{zESR}}\right)\left(1-\frac{s}{2\pi \times f_{zRHP}}\right)}{\left(1+\frac{s}{2\pi \times f_{pPS}}\right)} \quad (2)$$

Where:

- D is the duty cycle
- R_{out} is the output load resistance
- R_{sense} is the equivalent internal current sense resistor, which is typically 6mΩ

The single pole of the power stage can be given by:

$$f_{pPS} = \frac{2}{2\pi \times C_{out} \times R_{out}} \quad (3)$$

Where:

- C_{out} is the output capacitance. For a boost converter having multiple identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance

The zero created by the ESR of the output capacitor can be given by:

$$f_{zESR} = \frac{1}{2\pi \times C_{out} \times R_{ESR}} \quad (4)$$

Where:

- R_{ESR} is the equivalent resistance in series of the output capacitor

The right-hand plane zero can be given by:

$$f_{zRHP} = \frac{R_{out}(1-D)^2}{2\pi \times L} \quad (5)$$

Where:

- D is the duty cycle
- R_{out} is the output load resistor
- L is the inductance

Equation 6 shows the equation for feedback resistor network and the compensation network.

$$H_{COMP}(s) = G_{comp} \times R_{EA} \times \frac{R_{up} + R_{down}}{R_{down}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{zCOMP}}\right)}{\left(s1 + \frac{s}{2\pi \times f_{pCOMP1}}\right)\left(1 + \frac{s}{2\pi \times f_{pCOMP2}}\right)} \quad (6)$$

Where:

- G_{COMP} is the gain of the error amplifier, typically G_{EA} = 24uS
- R_{EA} is the output impedance of the error amplifier, typically R_{EA} = 5MΩ
- f_{pCOMP1}, f_{pCOMP2} is the pole's frequency of the compensation
- f_{zCOMP} is the zero's frequency of the compensation network

f_{pCOMP1} can be given by:

$$f_{pCOMP1} = \frac{1}{2\pi \times R_{EA} \times C_{COMP}} \quad (7)$$

Where:

- C_{COMP} is the compensation capacitor

f_{pCOMP2} can be given by:

$$f_{pCOMP2} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}} \quad (8)$$

Where:

- C_{HF} is the high frequency bypass capacitor on COMP pin
- R_{COMP} is the resistor of the compensation network

f_{zCOMP} can be given by:

$$f_{zCOMP} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad (9)$$

Where:

- C_{COMP} is the zero capacitor compensation
- R_{COMP} is the resistor of the compensation network

2.5.2 Step by Step Loop Compensation Design

With the previous analysis on small signal models, we can calculate the compensation network parameters with the given inductor and output capacitor parameters. TI provides EXCEL calculation tools on designing compensation parameters. This section gives an example on calculating loop compensation with the design calculation tool.

1. **Set the Crossover Frequency, f_C .**

   The first step is to set the loop crossover frequency, f_C. The higher the crossover frequency, the faster the loop response is. This is generally accepted that the loop gain crosses over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{zRHP}.
2. **Set the Compensation Resistance, R_{COMP} .**

   For a well compensated boost system, the f_C is determined by R_{COMP}.Set your desired f_C and the calculation tool can output recommended R_{COMP}.

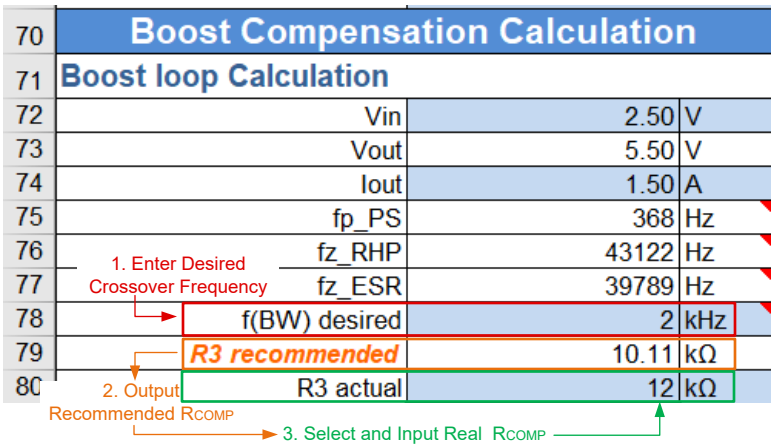

Figure 2-7. Set the Compensation Resistance

The calculation tool recommends the Rout under these assumptions: For a properly designed boost system, f_{zCOMP} must be placed below f_C to make sure of phase margin. For common R_{COMP} range, R_{COMP} must be far smaller than the amplifier output resistance R_{EA}, which makes R_{COMP} | | R_{EA} ~ = R_{COMP}. Therefore, looking at Equation 6, the initial gain $R_{COMP} \times G_{COMP} \times K_{FB}$ is determined by R_{COMP}. Therefore the f_c can be calculated by the equation that the close loop total gain $T_{(s)} = K_{PS}(s) + H_{COMP}(s)$ is zero at f_C.

$$H_{COMP} = 20lg\left(G_{COMP} \times R_{COMP} \times \frac{R_{down}}{R_{up} + R_{down}}\right) = -K_{PS}(f_c) \quad (10)$$

where

- K_{PS} is the gain of the power stage
- G_{EA} is the transconductance of the amplifier, the typical value of G_{EA} = 24μS

3. **Set the Compensation Zero capacitor, C_{COMP} .**

   The compensation zero needs to be placed at the power stage pole f_{pPS} to compensate the phase drop near f_{pPS}. Set $f_Z = f_P$, the C_{COMP} can be calculated . The calculation tool outputs the recommended C_{COMP} when the actual R_{COMP} is entered in line 80.

$$C_{COMP} = \frac{R_{out} \times C_{out}}{2R_{COMP}} \quad (11)$$

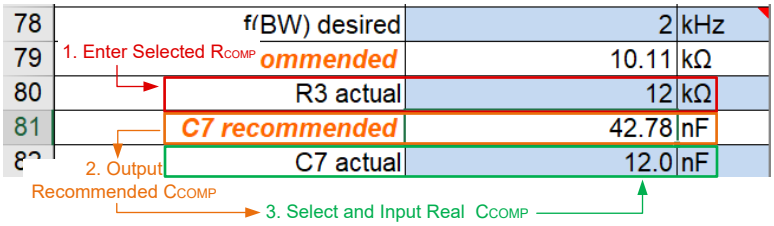

Figure 2-8. Set the Compensation Capacitance

4. **Set the Compensation Pole Capacitor, C_{HF} .**

The compensation pole needs to be placed to eliminate the ESR zero produced by R_{ESR} and C_{out}. Set $f_{pCOMP2} = f_{zESR}$, and get:

$$C_{HF} = \frac{R_{ESR} \times C_{out}}{R_{COMP}} \tag{12}$$

The recommended C_{HF} is located at the calculation tool line 84 after the ESR and Cout is correctly entered in line 15-16.

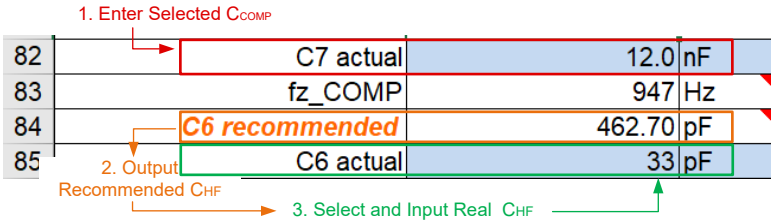

Figure 2-9. Set the Compensation Capacitance

5. **Check Phase Margin and Gain Margin**

The calculated compensation parameters do not always make sure of stability, especially when the Cout has large ESR which bring f_{zESR} into bandwidth. The calculation tool generates bode plot after all compensation parameters are entered. Check the bode plot for stability after steps 1-4. TI recommends phase margin > 60deg and gain margin > 10db. Reduce desired f_c and re-calculate compensation in steps 1-4 if the margin does not meet requirements.

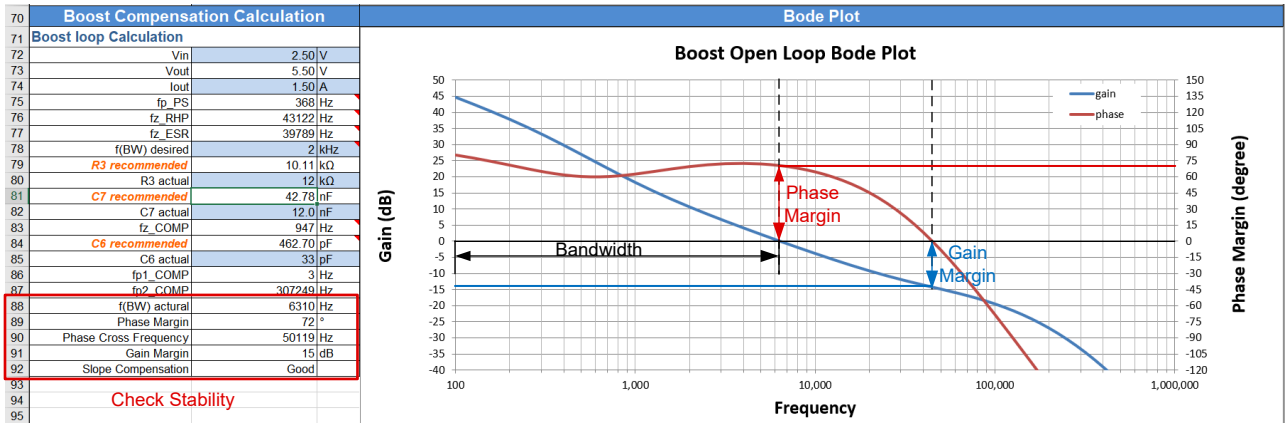

Figure 2-10. Evaluate Loop Stability

3 TPS61381-Q1 Layout Guide Line

3.1 Identification of the Critical Switching Loops

3.1.1 Low Side Driver Loop

Driver loop is one of the most critical loops for all switching regulators. When the IC turns on the MOSFET, current flows from the VCC capacitor through internal driver and gate resistor to charge the gate capacitance of low side MOSFET. The return current flow from the source of low side MOSFET(PGND), through net-tie to and return to VCC capacitor(AGND). When the IC turns off the MOSFET, gate capacitance of low side MOSFET is discharged. Current flows from the MOSFET gate through gate resistor into the LO pin, and eventually to the AGND pin. The return current flow from the IC AGND pin, through net-tie to and return to MOSFET gate capacitance (PGND). These charge and discharge current is generated within several ns and the peak current can reach up to 2A. So parasitic inductance in this current loop can create ringing on MOSFET gate and thus affect the effectiveness of the driver. Switching ringing can even cause boost leg shooting through and damage the device if the layout is not carefully designed. Low side driver current path is depicted in Figure 3-1.

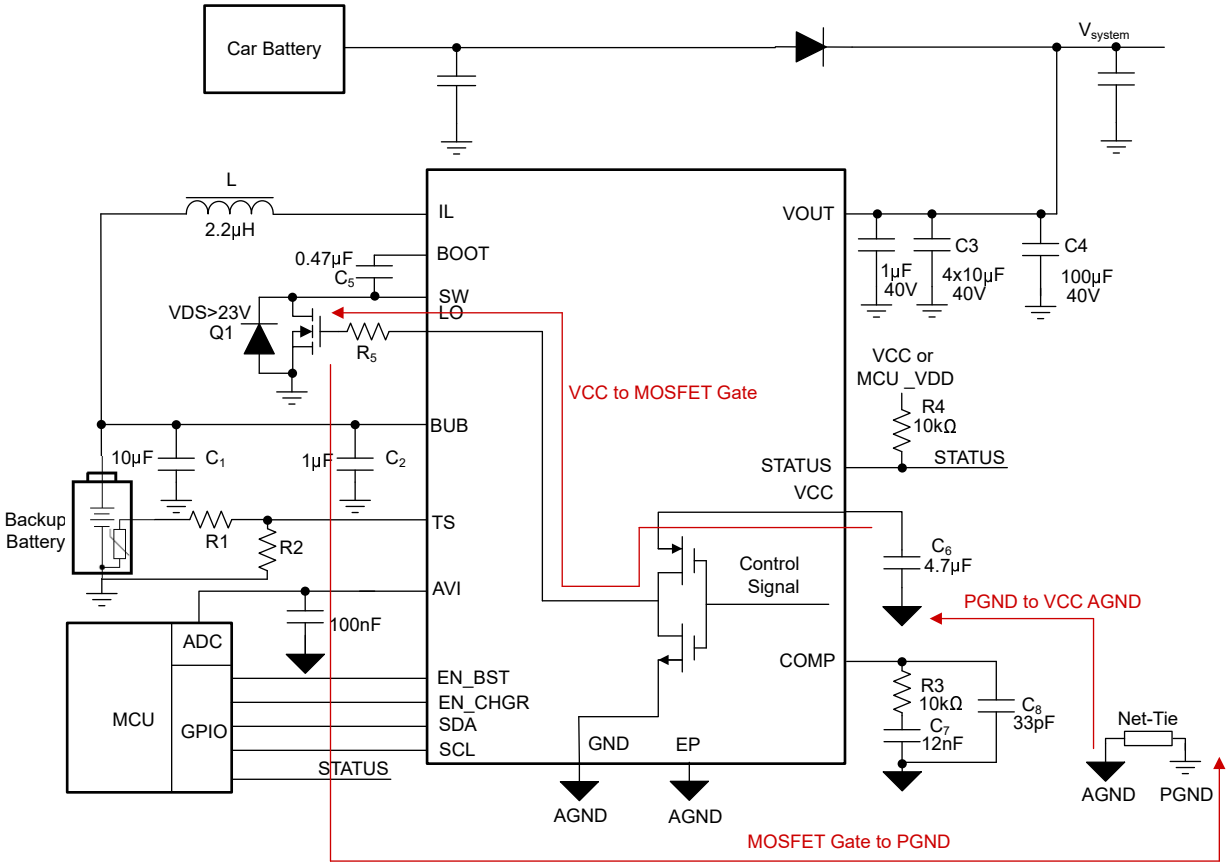

Figure 3-1. TPS61381-Q1 Low Side Driver Current Path

3.1.2 Boost Leg Switching Loop

Boost leg switching loop is the most critical loop for boost devices. Long and thin traces in these two loops can cause excessive noise, overshoot, and ring on the switch node, and the ground bounce because of the parasitic inductance. During a MOSFET switching event, the slew rate of the commutating current can exceed 3–5A/ns, so a 2nH parasitic inductance can result in a voltage spike of 6V. The pulsed current flowing in these critical loops during switching are rich in harmonic content and can cause a large radiated energy emission and electromagnetic interference issue if the loop area is not carefully minimized. This is crucial to minimize the trace length and the enclosed area of loop.

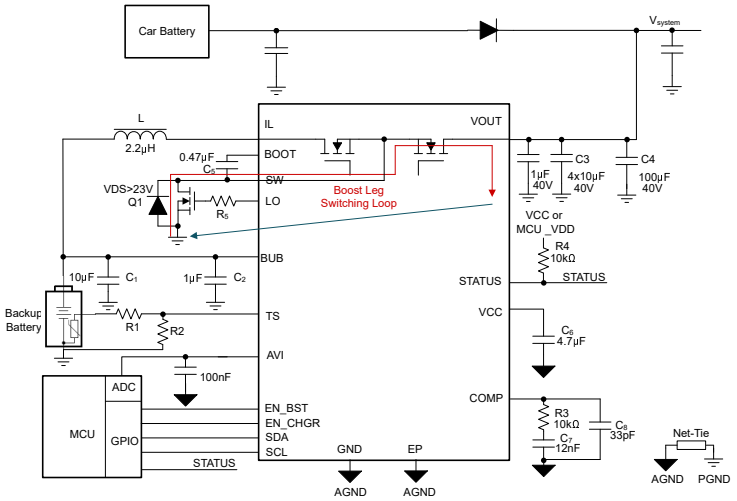

Figure 3-2. TPS61381-Q1 Boost Leg Switching Loop

3.1.3 High Side Driver Loop

High-side gate driver circuits are supplied by the bootstrap capacitor. Since TPS61381-Q1 is a bidirectional boost and buck converter in which both high side and low side MOSFETs can become the main switch. This is similar to low side driver circuit. Parasite inductance in high side driver loop creates extra switching noise in buck charger mode and affects the IC life span.

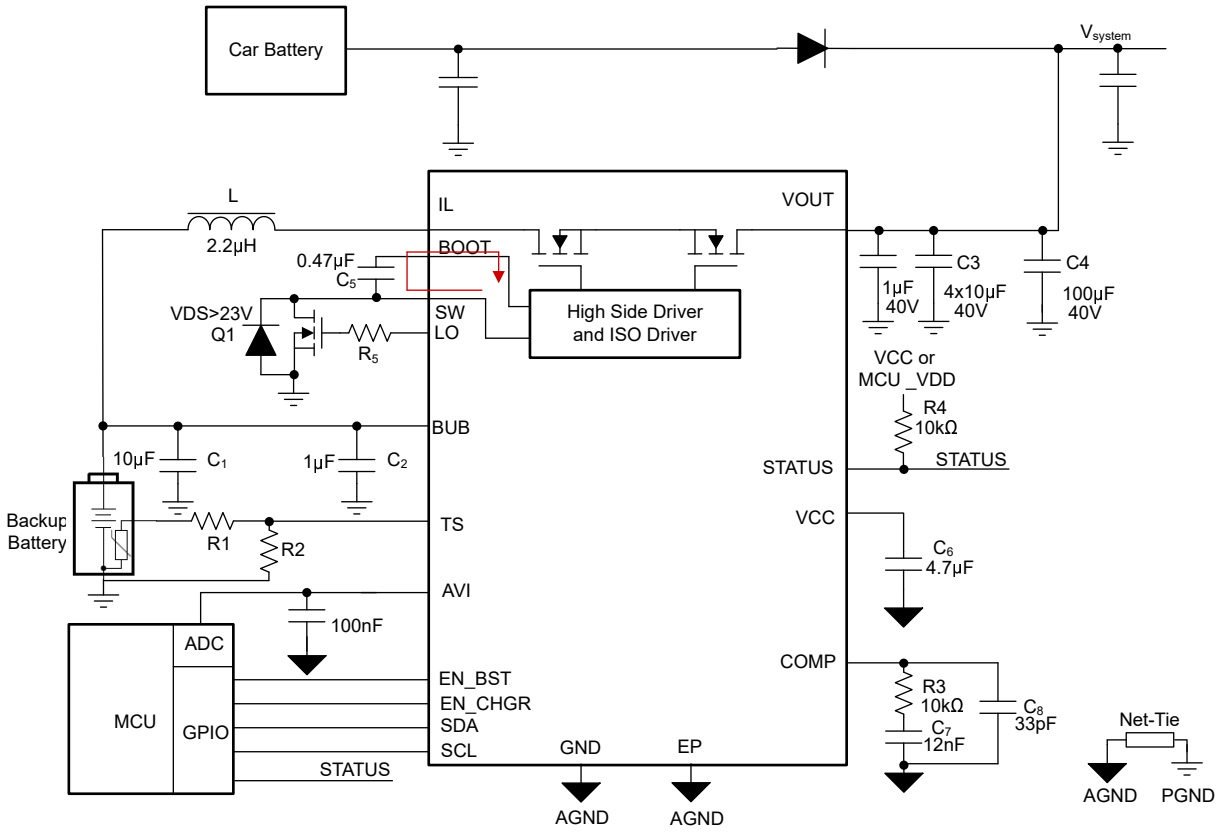

Figure 3-3. TPS61381-Q1 High Side Driver Loop

3.2 Power Component Placement

Figure 3-4 shows the placement of the power MOSFETs, input and output ceramic capacitors, main inductor, and the TPS61381-Q1 silicon on the top layer.

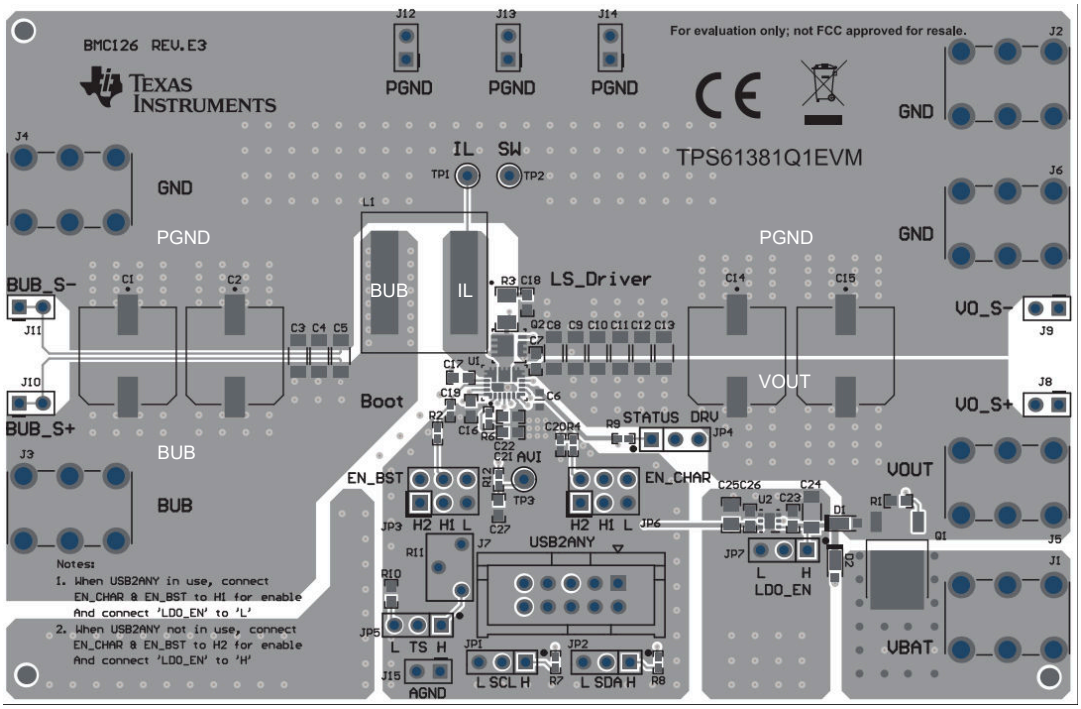

Figure 3-4. TPS61381-Q1 Power Component Placement Example

Output capacitors are placed adjacent to the VOUT pin of the TPS61381 external MOSFET source. The main inductor L1 is placed near the IL pin. The IL and SW nodes are poured with small copper plane to reduce the capacitive coupling relating to the SW node high dv/dt transitions. A large SW node copper plane helps the thermal, but can cause severe radiated emissions.

3.3 Layout Example

3.3.1 Optimizing Low Side Driver Loop Example

According to the analysis in Figure 3-1, driver current must go through the net-tie before returning to VCC to reduce the length and enclosed areas of the low side driver current path. The net-tie between AGND and PGND must be connected between source of the low side MOSFET. Driver current return path is cut out from PGND copper and routed closely in parallel with the gate trace as differential pairs so that the mutual inductance can eliminate parasitic inductance. The VCC capacitor must be placed as close to the IC as possible.

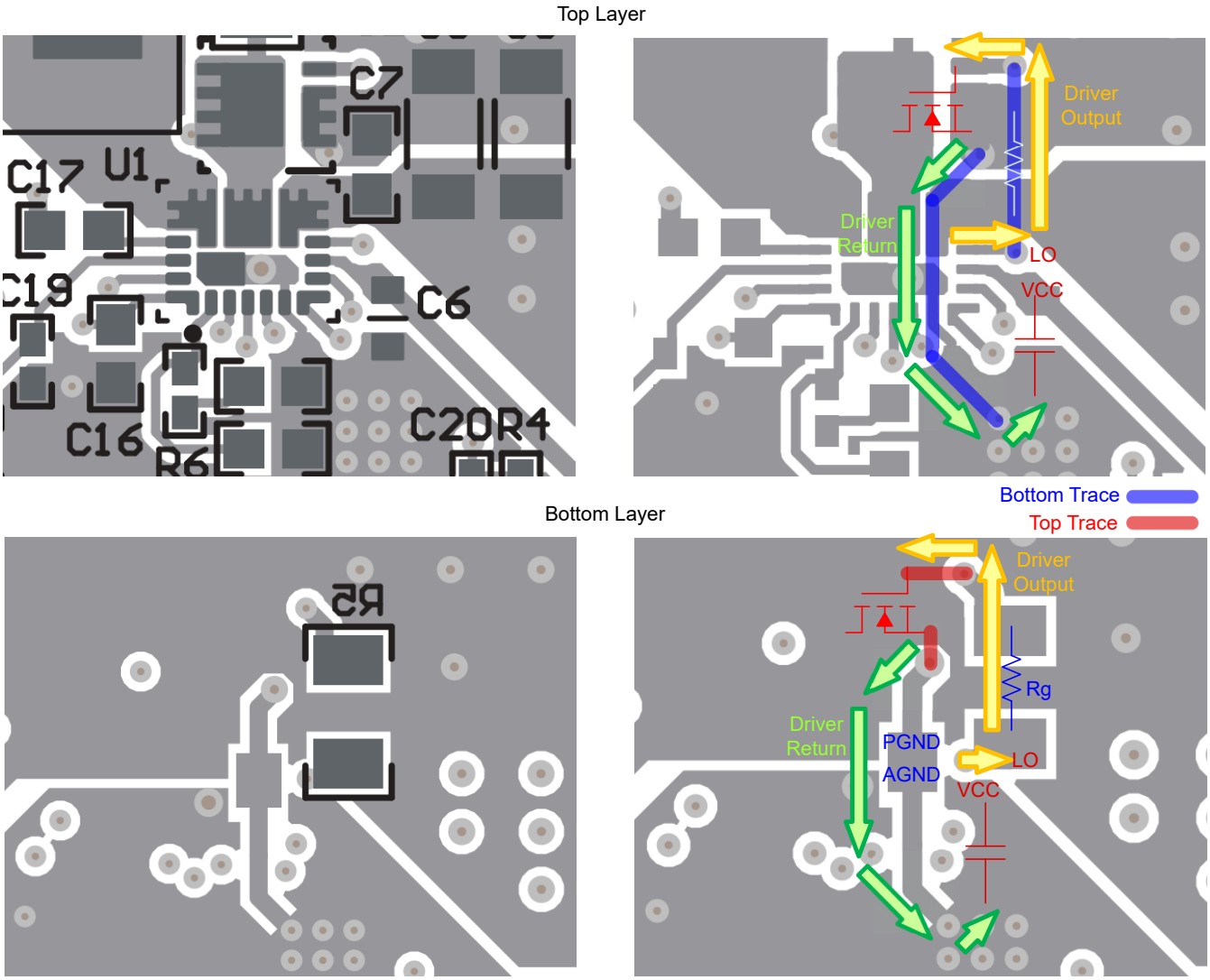

Figure 3-5. TPS61381-Q1 Low Side Driver Layout Example

3.3.2 Optimizing Boost Leg Switching Loop Example

Figure 3-6 shows an example of a boost leg switching loop. To reduce the length of this current path, MLCC must be placed as close to Vout pin as possible (within 1mm) and the low side MOSFET Q1 must be placed as close to SW pin as possible. TI also recommends a smaller Cout (100nF-1uF, 0603 package) closest to the Vout pin to bypass the high frequency noise.

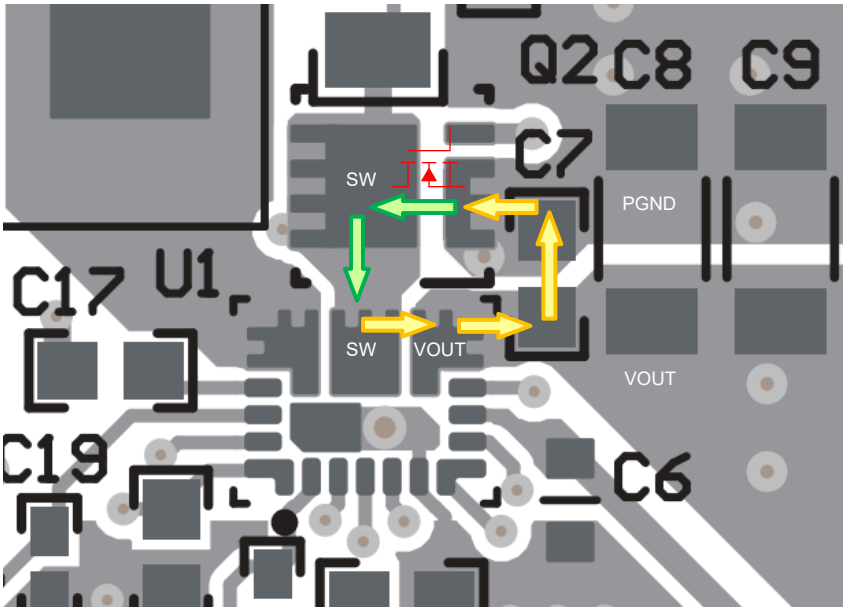

Figure 3-6. TPS61381-Q1 Boost Leg Switching Loop Layout Example

3.3.3 Optimizing High Side Driver Loop Example

Figure 3-7 shows an example of high side driver loop routing. Placing the bootstrap capacitor very close to the SW and the boot pins can reduce the gate loop enclosed areas. Route the gate drive traces from the silicon to the MOSFET as short as possible, routing the gate drive and the return traces side by side can minimize the gate-loop inductance and the gate-loop area.

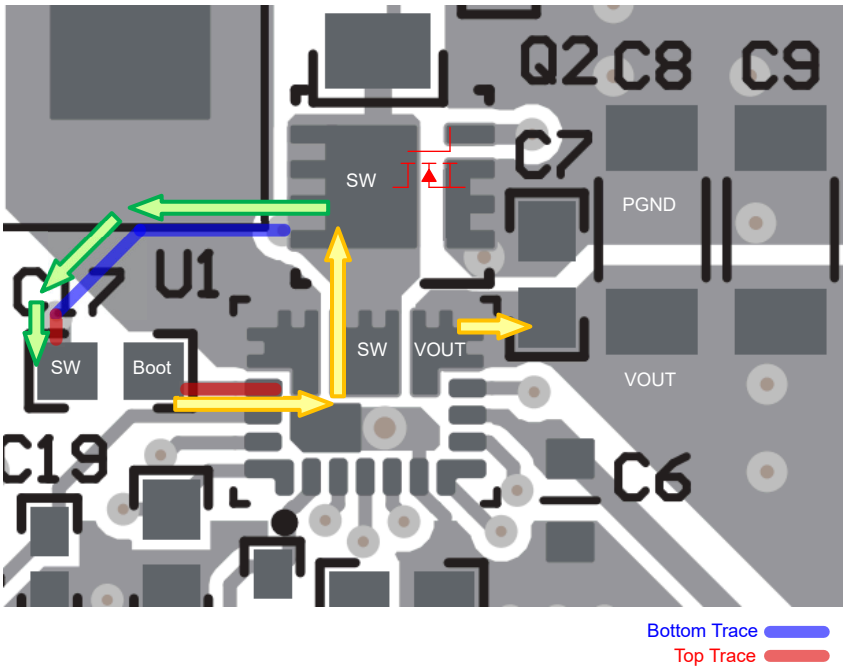

Figure 3-7. TPS61381-Q1 High Side Driver Layout Example

3.3.4 Signal Circuit Routing Example

The area of the switching node SW and IL must be as small as possible. If the SW and IL are poured with big area copper planes, the high dv/dt noisy signal can couple into other traces nearby though capacitive coupling and causes electromagnetic interference issues. Signal traces must avoid the area near or under SW and IL nets.

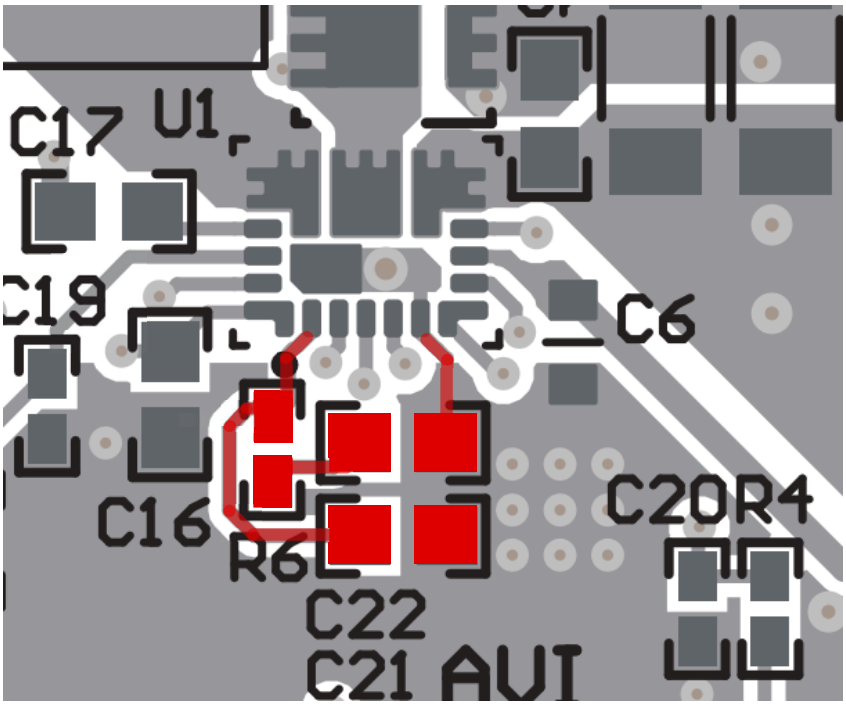

Figure 3-8. TPS61381-Q1 Signal Circuit Routing Example

COMP pin is vulnerable to CM noise and the compensation parts must be placed near the IC to make sure the high frequency cap C_8 can bypass the noise.

4 Summary

This application note describes how to route the TPS61381-Q1 bidirectional boost and buck converter with a 4-layer printed circuit board. This begins with the identification of the critical switching loops. By proper power component placement, keeping critical loops small, placing a whole layer GND copper plane under the switching loops, and carefully routing the sensitive traces, a successful converter design can be achieved.

5 References

- Texas Instruments, TPS61381-Q1 Automotive 400kHz, 40V, 15A Boost Converter with LDO Charger and Battery State of Health Detection, datasheet.

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