Application Note

Multiple TAC5x1x Devices with a Shared TDM and I²C Bus

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ABSTRACT

The TAC5x1x devices (TAC5111, TAC5112, TAC5211, TAC5212, TAC5311-Q1, TAC5312-Q1, TAC5412-Q1) are mono- (TAC5x11) or dual- (TAC5x12) channel, high-performance codecs for audio applications. This document describes how to configure multiple TAC5x1x devices to share a single TDM and I²C Bus.

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1 Introduction

Each ADC channel of the TAC5x1x supports one analog differential or single-ended input or two digital pulse density modulation (PDM) microphone inputs, while each DAC channel supports one differential or up to two single-ended outputs.

Up to four TAC5x1x devices can share a single audio data bus using a time-division multiplexed (TDM) interface to minimize board routing area for systems with up to 8 analog or 16 PDM inputs, and up to 16 analog outputs.

TAC5x1x supports a shared control bus using the I^{2}C interface. This application note focuses on how to configure the TAC5x1x to share a single control and audio data bus between the devices, as shown in Figure 1-1.

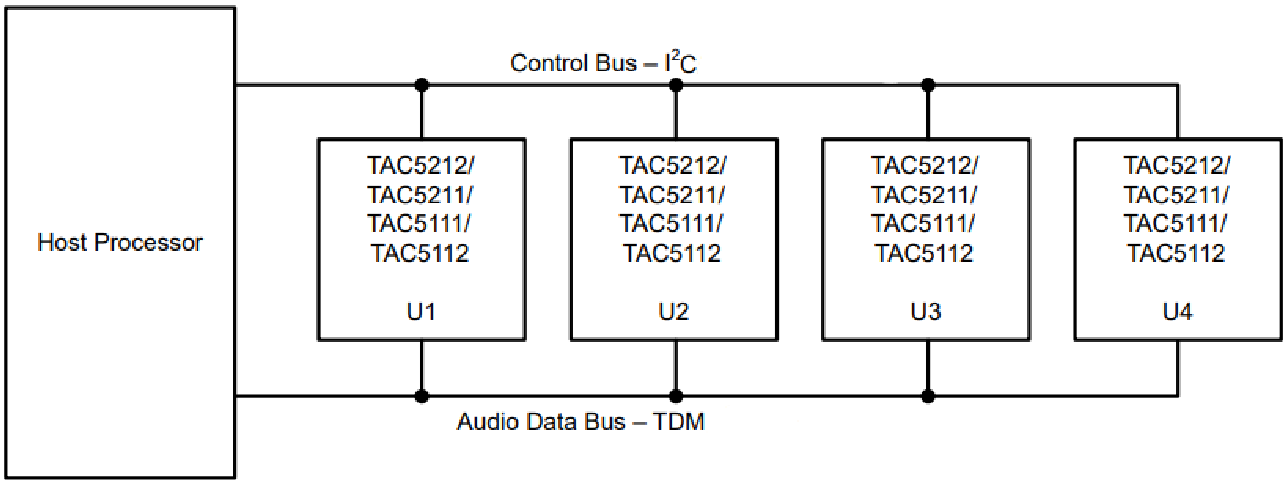

Figure 1-1. Four TAC5x1x Devices with a Shared Control and Audio Data Bus

2 Sharing the Control Bus

The TAC5x1x devices are controlled through an I^{2}C bus operating in standard-mode, fast-mode, or fast-mode plus. This I^{2}C control bus requires a 7-bit target address whose two least significant bits are programmable by pulling the ADDR pin to GND or AVDD with a resistor of a specified value. Table 2-1 lists the four possible TAC5x1x device addresses resulting from the configuration options for this pin.

Table 2-1. TAC5x1x I^{2}C Target Address Settings

ADDR Setting	Device Address (7-bit)	Device Address (8-bit)
Short to GND	0x50	0xA0
Pull down 4.7kΩ to GND	0x51	0xA2
Pull up 22kΩ to AVDD	0x52	0xA4
Pull up 4.7kΩ to AVDD	0x53	0xA6

With each TAC5x1x device having a unique ADDR setting, the SCL and SDA lines can be shorted between devices and connected to a single I^{2}C bus from the main controller.

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3 Sharing the Audio Bus

TAC5x1x devices send the digitized audio data through a TDM audio bus in which channel transfers start on the rising edge of FSYNC with the first slot of data (slot 0), followed by the remaining data slots in increasing order (slot 1, slot 2, etc.). Each slot transmits a bit on the rising edge of BCLK, starting with the most significant bit first. Figure 3-1 shows an example of TDM bus operation for 8 slots when TX_OFFSET is set to 0, meaning that the MSB is transmitted on the same BCLK edge as FSYNC. In this figure, FSYNC is the frame sync signal from the host processor, BCLK is the bit clock signal from the host processor, and DIN/DOUT is the data bus to or from the TAC5x1x devices. TAC5x1x supports up to 32 slot assignments for each channel on the DIN and DOUT data bus.

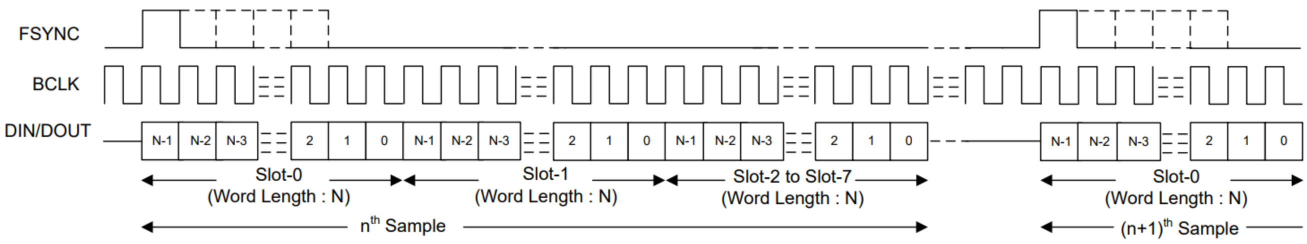

Figure 3-1. TDM Mode Standard Protocol Timing (TX_OFFSET = 0)

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the programmed word length of the output channel data, as shown in Equation 1. For the example shown in Figure 1-1 with four devices, each with four channels, at a 48 kHz sampling rate and 32-bit word length, BCLK ≥ 4 × 4 × 48 000 × 32 = 24.576 MHz. Since the maximum supported BCLK is 25 MHz, the maximum number of devices available on the shared audio bus is dependent on the number of channels used per device, the sampling rate, and the word length.

$$25\text{ MHz} \geq \text{BCLK} \geq (\text{\# channels/device}) \times (\text{\# devices}) \times (\text{sampling rate}) \times (\text{word length}) \quad (1)$$

Note

For BCLK periods greater than 18.5 MHz, the microprocessor must latch the DOUT data on same BCLK edge polarity as the device.

Failure to observe this condition might result in the microprocessor capturing corrupted data from DOUT.

The TAC5x1x supports wiring several devices together in a Shared TDM configuration of the ADC and DAC paths. Additionally, there is a Daisy Chain TDM configuration, but it is only supported for the ADC path. The following two sections detail the registers that need to be programmed to configure the TAC5x1x devices to share the TDM bus in these methods.

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3.1 ASI Configuration for Shared TDM

In Shared TDM bus configuration, the ASI buses of multiple TAC5x1x devices are connected together into a single shared bus, as shown in Figure 3-2.

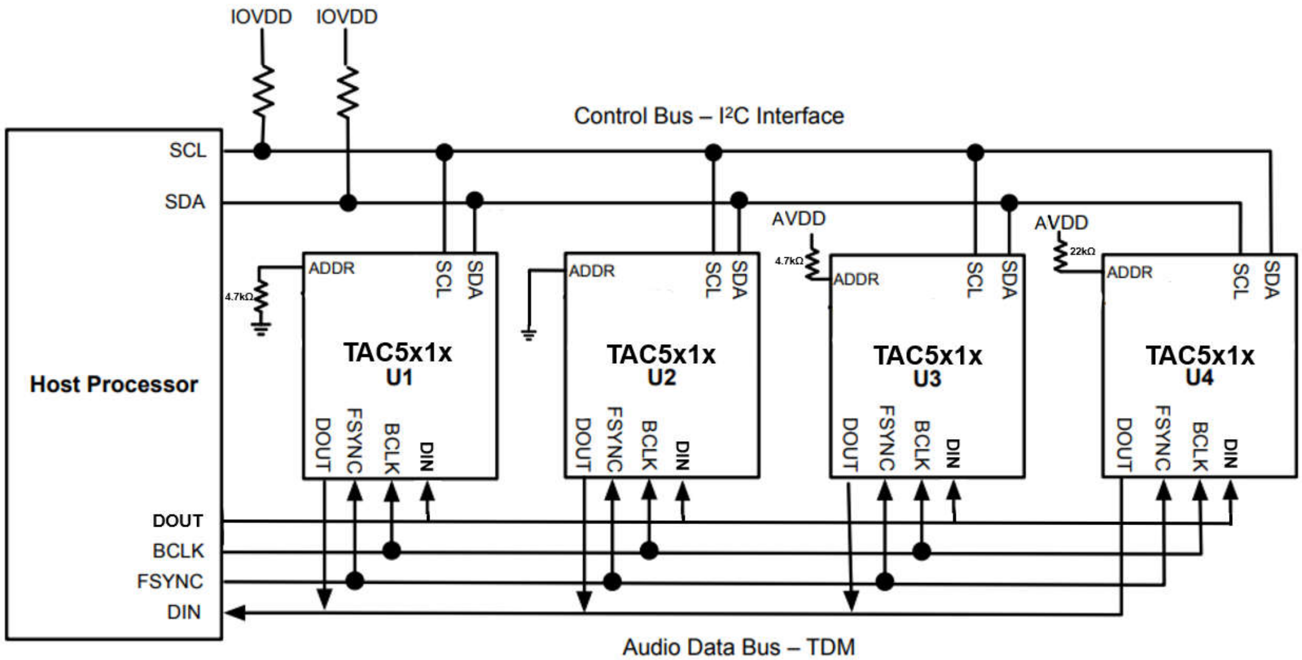

Figure 3-2. TAC5x1x Shared TDM Connection Diagram

To avoid multiple devices transmitting output data in the same slot, the TAC5x1x supports mapping the input channels of a device to a programmable slot using the following registers:

- PASI_TX_CH1_CFG (Page 0x00, Register 0x1E)
- PASI_TX_CH2_CFG (Page 0x00, Register 0x1F)
- PASI_TX_CH3_CFG (Page 0x00, Register 0x20)
- PASI_TX_CH4_CFG (Page 0x00, Register 0x21)

Similarly, the output channels of a device can be mapped to a programmable slot using the following registers:

- PASI_RX_CH1_CFG (Page 0x00, Register 0x28)
- PASI_RX_CH2_CFG (Page 0x00, Register 0x29)
- PASI_RX_CH3_CFG (Page 0x00, Register 0x2A)
- PASI_RX_CH4_CFG (Page 0x00, Register 0x2B)

This allows any channel on either data bus to be mapped to any of the 32 available TDM slots in any order.

For the example of Figure 3-2, the following I^{2}C script configures the input channels of U1–U4 into TX slots 0–15 for TAC5x1x, respectively. This script enables a shared ADC data output bus, but this configuration also works for the DAC input bus, as shown in Figure 3-2. This script can be applied to the DAC input data on the RX bus by changing the register addresses to the corresponding RX values mentioned above. Note that slots are not assigned to the input channels of each device in sequence to show the flexibility of channel assignments to TDM slots:

```
w A0 1E 24  # Set U1 Ch1 mapped to slot 4 of DOUT
w A0 1F 26  # Set U1 Ch2 mapped to slot 6 of DOUT
w A0 20 21  # Set U1 Ch3 mapped to slot 1 of DOUT
w A0 21 20  # Set U1 Ch4 mapped to slot 0 of DOUT
w A2 1E 23  # Set U2 Ch1 mapped to slot 3 of DOUT
w A2 1F 25  # Set U2 Ch2 mapped to slot 5 of DOUT
w A2 20 22  # Set U2 Ch3 mapped to slot 2 of DOUT
w A2 21 27  # Set U2 Ch4 mapped to slot 7 of DOUT
w A4 1E 28  # Set U3 Ch1 mapped to slot 8 of DOUT
```


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```
w A4 1F 29  # Set U3 Ch2 mapped to slot 9 of DOUT
w A4 20 2A  # Set U3 Ch3 mapped to slot 10 of DOUT
w A4 21 2C  # Set U3 Ch4 mapped to slot 12 of DOUT
w A6 1E 2F  # Set U4 Ch1 mapped to slot 15 of DOUT
w A6 1F 2D  # Set U4 Ch2 mapped to slot 13 of DOUT
w A6 20 2E  # Set U4 Ch3 mapped to slot 14 of DOUT
w A6 21 2B  # Set U4 Ch4 mapped to slot 11 of DOUT
```

This configuration requires that all the devices place their outputs in high-impedance mode, so another device can drive the bus. TAC5x1x supports driving the output line low or placing it in high-impedance during unused bit clock cycles through the PASI_TX_CFG0 register 0x1B bit field PASI_TX_FILL, shown in Table 3-1. Setting the PASI_TX_FILL places the output line DOUT in high-impedance during unused bit clock cycles. Note the reset value configures DOUT to drive low during unused cycles.

Table 3-1. PASI_TX_CFG0 Register 0x1B

Bit	Field	Type	Reset	Description
7	PASI_TX_EDGE	R/W	0b	Primary ASI data output (on the primary and secondary data pin) transmit edge 0d = Default edge as per the protocol configuration setting in PASI_BCLK_POL 1d = Inverted following edge (half cycle delay) with respect to the default edge setting
6	PASI_TX_FILL	R/W	0b	Primary ASI data output (on the primary and secondary data pin) for any unused cycles 0d = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles
5	PASI_TX_LSB	R/W	0b	Primary ASI data output (on the primary and secondary data pin) for LSB transmissions 0d = Transmit the LSB for a full cycle 1d =Transmit the LSB for the first half cycle and Hi-Z for the second half cycle 2d = 24 bits 3d = 32 bits
4-3	PASI_TX_KEEPER[1:0]	R/W	00b	Primary ASI data output (on the primary and secondary data pin) bus keeper 0d = Bus keeper is always disabled 1d = Bus keeper is always enabled 2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = 32 Bus keeper is enabled during LSB transmissions only for one and half cycles
2	PASI_TX_USE_INT_FSYNC	R/W	0b	Primary ASI uses internal FSYNC for output data generation in Controller mode configuration as applicable 0d = Use external FSYNC for ASI protocol data generation 1d = Use internal FSYNC for ASI protocol data generation
1	PASI_TX_USE_INT_BCLK	R/W	0b	Primary ASI uses internal BCLK for output data generation in Controller mode configuration. 0d = Use external BCLK for ASI protocol data generation 1d = Use internal BCLK for ASI protocol data generation
0	PASI_TDM_PULSE_WIDTH	R/W	0b	Primary ASI FSYNC pulse width in TDM format. (Valid for Controller mode) 0d = FSYNC pulse is 1 BCLK period wide 1d = FSYNC pulse is 2 BCLK period wide

TAC5x1x also supports tri-stating unused channels slots through the PASI_TX_CHx_CFG registers, as shown in Table 3-2, or disabling unused input slots through the PASI_RX_CHx_CFG registers, as shown in Table 3-2.

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Table 3-2. PASI_TX_CHx_CFG Register 0x1E - 0x25

Bit	Field	Type	Description
7-6	RESERVED	R	Reserved bits; Write only reset values
5	PASI_TX_CHx_CFG	R/W	Primary ASI output channel X configuration 0d = Primary ASI channel X output is in a tri-state condition 1d = Primary ASI channel X output corresponds to ADC/PDM Channel X data
4-0	PASI_TX_CHx_SLOT_NUM[4:0]	R/W	Primary ASI output channel X slot assignment. 0d = TDM is slot 0 1d = TDM is slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 16d = TDM is slot 16 17d = TDM is slot 17 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31

Table 3-3. PASI_RX_CHx_CFG Register 0x28 - 0x2F

Bit	Field	Type	Description
7-6	RESERVED	R	Reserved bits; Write only reset values
5	PASI_RX_CHx_CFG	R/W	Primary ASI input channel X configuration 0d = Primary ASI channel X input is disabled 1d = Primary ASI channel X output corresponds to DAC Channel X data
4-0	PASI_TX_CHx_SLOT_NUM[4:0]	R/W	Primary ASI input channel X slot assignment. 0d = TDM is slot 0 1d = TDM is slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 16d = TDM is slot 16 17d = TDM is slot 17 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31

Furthermore, the TAC5x1x supports configuring a GPIO pin as a secondary DOUT output (DOUT2) or secondary DIN input (DIN2) through the GPIO1_CFG0, GPIO2_CFG0, or GPO1_CFG0 register. This allows one or more devices transmitting data through two pins. The PASI_TX_CFG2 register 0x1D bit field PASI_TX_CHx_SEL maps a slot to the primary (DOUT) or secondary output (DOUT2). The PASI_RX_CFG1 register 0x27 bit field PASI_RX_CHx_SEL maps a slot to the primary (DIN) or secondary input (DIN2).

These secondary data lines can be used to support a greater number of slots than Equation 1 allows. This connection method not only decreases the bit clock (BCLK) speed, but also reduces the load capacitance on the data lines of the host processor. For example, a system with 12 channels, 32-bit data words, and running with a 96-KHz sample rate requires a bit clock of 36.864 MHz (three devices * four channels/device * 32 bit words * 96 kHz), violating the maximum BCLK speed of 25 MHz. Dividing the 12 channels by assigning six channels to a primary bus and six channels to a secondary bus keeps the BCLK under 25 MHz. Since each device has four channels, one device has two channels assigned to the primary bus and two channels assigned to the secondary bus.

For the example described above, the following I^2C script configures U1, U2, and U3 for Shared TDM of the ADC output with primary and secondary DOUT bus.

```
w A0 1E 20  # Set U1 Ch1 mapped to slot 0 of DOUT
w A0 1F 21  # Set U1 Ch2 mapped to slot 1 of DOUT
w A0 20 22  # Set U1 Ch3 mapped to slot 2 of DOUT
w A0 21 23  # Set U1 Ch4 mapped to slot 3 of DOUT
w A2 1E 24  # Set U2 Ch1 mapped to slot 4 of DOUT
w A2 1F 25  # Set U2 Ch2 mapped to slot 5 of DOUT
w A2 0A 62  # Set U2 GPIO1 as DOUT2
w A2 1D 0C  # Set U2 Ch3 and Ch4 to DOUT2
w A2 20 20  # Set U2 Ch3 mapped to slot 0 of DOUT2
```


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```
w A2 21 21  # Set U2 Ch4 mapped to slot 1 of DOUT2
w A4 0A 62  # Set U3 GPIO1 as DOUT2
w A4 1D 0F  # Set U2 Ch1-4 to DOUT2
w A4 1E 42  # Set U3 Ch1 mapped to slot 2 of DOUT2
w A4 1F 43  # Set U3 Ch2 mapped to slot 3 of DOUT2
w A4 20 44  # Set U3 Ch3 mapped to slot 4 of DOUT2
w A4 21 45  # Set U3 Ch4 mapped to slot 5 of DOUT2
```

As mentioned previously, the shared TDM configuration can be enabled on the DAC input data bus as well as the ADC output bus. For the example described above, the following I^{2}C script configures U1, U2, and U3 for Shared TDM of the DAC input with primary and secondary DIN.

```
w A0 28 20  # Set U1 Ch1 mapped to slot 0 of DIN
w A0 29 21  # Set U1 Ch2 mapped to slot 1 of DIN
w A0 2A 22  # Set U1 Ch3 mapped to slot 2 of DIN
w A0 2B 23  # Set U1 Ch4 mapped to slot 3 of DIN
w A2 28 24  # Set U2 Ch1 mapped to slot 4 of DIN
w A2 29 25  # Set U2 Ch2 mapped to slot 5 of DIN
w A2 0A 12  # Set U2 GPIO1 as input
w A2 0F 04  # Select GPIO1 as DIN2
w A2 27 0C  # Set U2 Ch3 and Ch4 to DIN2
w A2 2A 20  # Set U2 Ch3 mapped to slot 0 of DIN2
w A2 2B 21  # Set U2 Ch4 mapped to slot 1 of DIN2
w A4 0A 12  # Set U3 GPIO1 as input
w A4 0F 04  # Select GPIO1 as DIN2
w A4 27 0F  # Set U2 Ch1-4 to DIN2
w A4 28 22  # Set U3 Ch1 mapped to slot 2 of DIN2
w A4 29 23  # Set U3 Ch2 mapped to slot 3 of DIN2
w A4 2A 24  # Set U3 Ch3 mapped to slot 4 of DIN2
w A4 2B 25  # Set U3 Ch4 mapped to slot 5 of DIN2
```

3.2 ASI Configuration for Daisy Chain TDM

To simplify board routing and TDM bus timing requirements, or to avoid high DOUT line load capacitance, TAC5x1x devices offer a daisy-chain mode that routes data output (DOUT) of one device as input to the GPIO1, GPIO2, or GPI1 pin of another device. Each device internally combines the data into the appropriate slot in the TDM bus and passes it to the next device. Unlike the Shared TDM, this configuration is only available for the ADC path, as the analog DAC output cannot be daisy-chained.

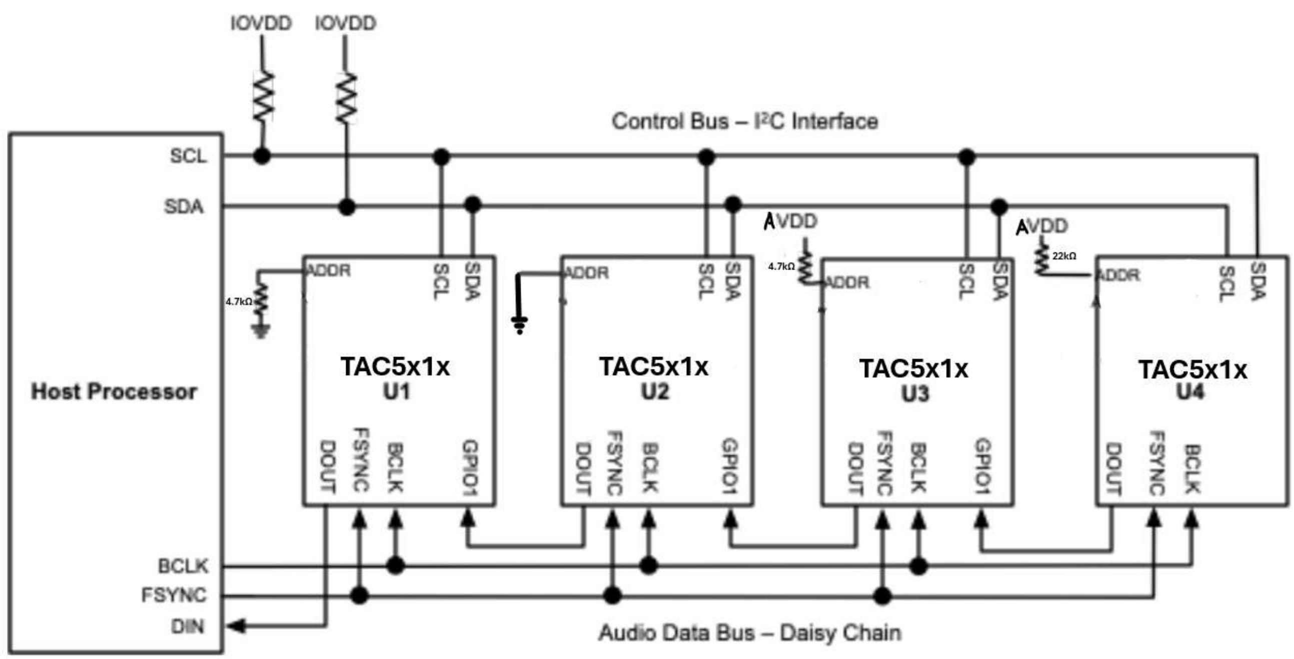

Figure 3-3. TAC5x1x Daisy Chain TDM Connection Diagram

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Setting the DAISY_EN bit field of the ASI_CFG0 Register shown in Table 3-4 configures the devices for daisy chain configuration. The DAISY_IN_SEL bit field selects the GPIO pin to be used as the daisy chain input. The selected GPIO must also be configured as an input. Only one ASI is available when configuring in daisy chain mode.

Table 3-4. ASI_CFG0 Register 0x18

Bit	Field	Type	Reset	Description
7	PASI_DIS	R/W	0b	Disable or enable primary ASI (PASI). 0d = Primary ASI enabled 1d = Primary ASI disabled
6	SASI_DIS	R/w	1b	Disable or enable secondary ASI (SASI). 0d = Secondary ASI enabled 1d = Secondary ASI disabled
5	SASI_CFG_GANG	R/W	0b	All configurations of secondary ASI ganged with primary ASI. 0d = Secondary ASI has independent configurations 1d = Secondary ASI configurations same as primary ASI
4	DAISY_EN[1:0]	R/W	00b	Daisy chain feature enable (Only 1 ASI with 1 DOUT AND DIN available) 0d = Daisy chain disabled 1d = PASI daisy chain enabled (Secondary ASI not available) 2d = SASI daisy chain enabled (Primary ASI not available) 3d = Reserved; Don't use
3-0	DAISY_IN_SEL[2:0]	R/W	000b	Daisy input select configuration. 0d = Daisy input disabled 1d = GPIO1 2d = GPIO2 3d = GPI1 4d = Reserved 5d = DIN 6d to 7d = Reserved

For the example of Figure 3-3, the following I^{2}C script configures U1, U2, and U3 for daisy chain, taking input from the next device in the DOUT through GPIO1 of the chain. Note that channels of each device are mapped to slots 0-3. However, the DOUT of U1 has slots 0-3 with the U1 channels, slots 4-7 with the U2 channels, slots 8-11 with the U3 channels, and slots 12-15 with the U4 channels. Note that the first device in the daisy chain (U4) does not need to be configured for daisy chain mode since it is not taking input on GPIO1 from another device.

```
w A0 1E 20  # Set U1 Ch1 mapped to slot 0 of DOUT
w A0 1F 21  # Set U1 Ch2 mapped to slot 1 of DOUT
w A0 20 22  # Set U1 Ch3 mapped to slot 2 of DOUT
w A0 21 23  # Set U1 Ch4 mapped to slot 3 of DOUT
w A2 1E 20  # Set U2 Ch1 mapped to slot 0 of DOUT
w A2 1F 21  # Set U2 Ch2 mapped to slot 1 of DOUT
w A2 20 22  # Set U2 Ch3 mapped to slot 2 of DOUT
w A2 21 23  # Set U2 Ch4 mapped to slot 3 of DOUT
w A4 1E 20  # Set U3 Ch1 mapped to slot 0 of DOUT
w A4 1F 21  # Set U3 Ch2 mapped to slot 1 of DOUT
w A4 20 22  # Set U3 Ch3 mapped to slot 2 of DOUT
w A4 21 23  # Set U3 Ch4 mapped to slot 3 of DOUT
w A6 1E 20  # Set U4 Ch1 mapped to slot 0 of DOUT
w A6 1F 21  # Set U4 Ch1 mapped to slot 1 of DOUT
w A6 20 22  # Set U4 Ch1 mapped to slot 2 of DOUT
w A6 21 23  # Set U4 Ch1 mapped to slot 3 of DOUT
w A0 18 49  # Set U1's ASI to daisy chain via GPIO1
w A0 21 10  # Set U1's GPIO1 input as ASI input for daisy chain
w A2 18 49  # Set U2's ASI to daisy chain via GPIO1
w A2 21 10  # Set U2's GPIO1 input as ASI input for daisy chain
w A4 18 49  # Set U3's ASI to daisy chain via GPIO1
w A4 21 10  # Set U3's GPIO1 input as ASI input for daisy chain
```


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4 Configuring PurePath Console 3 for Multiple TAC5x1x EVMs

The PurePath™ Console 3 supports multiple TAC5x1x devices connected to a single AC-MB. However, the AC-MB connector can only be connected to one TAC5x1x. To connect additional devices to a single AC-MB, externally wire power, ground, I²C, and TDM signals of the board connected to a single AC-MB to the respective signals of the other TAC5x1x EVMs. Connect only one EVM to the AC-MB while connecting the other signals through their respective headers or jumpers as follows:

- Connect together IOVDD from all the TAC5x1x EVMs through the IOVDD test point.
- Connect together AVDD from all the TAC5x1x EVMs through the AVDD test point.
- Connect together the SCL pins from all TAC5x1x devices through the SCL test point.
- Connect together the SDA pins from all TAC5x1x devices through the SDA test point.
- Connect together the BCLK pins from all TAC5x1x devices through the BCLK test point.
- Connect together the FSYNC pins from all TAC5x1x devices through the FSYNC test point.
- Connect together a common GND from all TAC5x1x devices through any GND test point.
- DOUT connections depend on Shared TDM or Daisy-Chain TDM mode:
  - For Shared TDM mode, connect together the DOUT pins from all TAC5x1x devices through the DOUT test point.
  - For Daisy-Chain TDM mode, connect the TAC5x1x EVMs in a daisy chain fashion:
    - Connect the GPIO1 signal at the GPIO1 test point from the board connected to the AC-MB to the DOUT pin of the second board through the DOUT test point.
    - Connect the signal of the second board at the GPIO1 test point to the DOUT pin of the third board through the DOUT test pin, if using three devices or more.
    - Connect the signal of the third board at the GPIO1 test point to the DOUT pin of the fourth board through the DOUT test pin, if using four devices.

These signals can be tapped at the respective digital test points of the TAC5x1x EVMs, as shown in Figure 4-1.

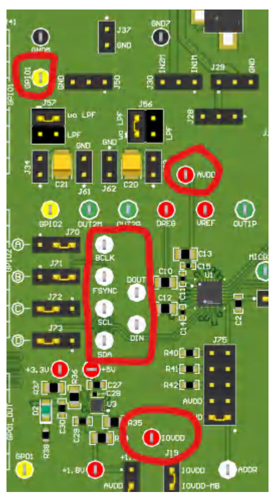

Figure 4-1. Location of TAC5x1x EVM I²C and TDM signals

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4.1 Changing the Default I²C Address of the TAC5x1x

When multiple TAC5x1x EVMs are connected to a single I2C bus, each EVM must have a unique I²C address. On TAC5x1x EVMs, the I²C address is set by pullups and pulldowns at header J75, as shown in Figure 4-2. Placement of the jumper in this section, as shown in Table 4-1, controls the I2C address of each TAC5x1x device.

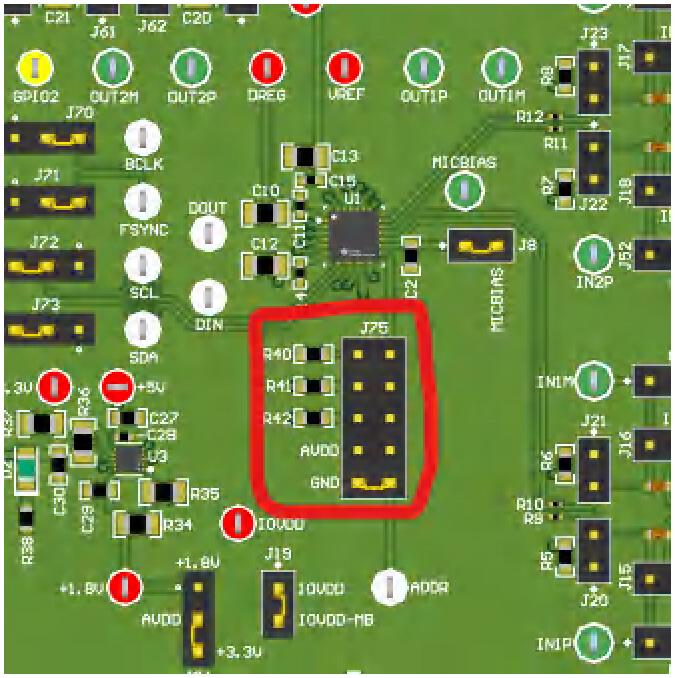

Figure 4-2. I²C Address Configuration for the TAC5x1x EVM

Table 4-1. TAC5x1x EVM I²C Target Address

J75 Position	ADDR Setting	I²C TARGET ADDRESS (BINARY)
1 (shown in Figure 4-2)	Short to GND	1010 000
2	Short to AVDD	N/A (SPI)
3	Pull up 22kΩ to AVDD	1010 010
4	Pull up 4.7kΩ to AVDD	1010 011
5	Pull down 4.7kΩ to GND	1010 001

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4.2 Launching PurePath Console with Multiple Devices

When PurePath Console is launched, it queries the user on how many devices are connected to an AC-MB, as shown in Figure 4-3. In this dialog window, after selecting two TAC5212 devices and clicking on New, the main window shown in Figure 4-4 launches.

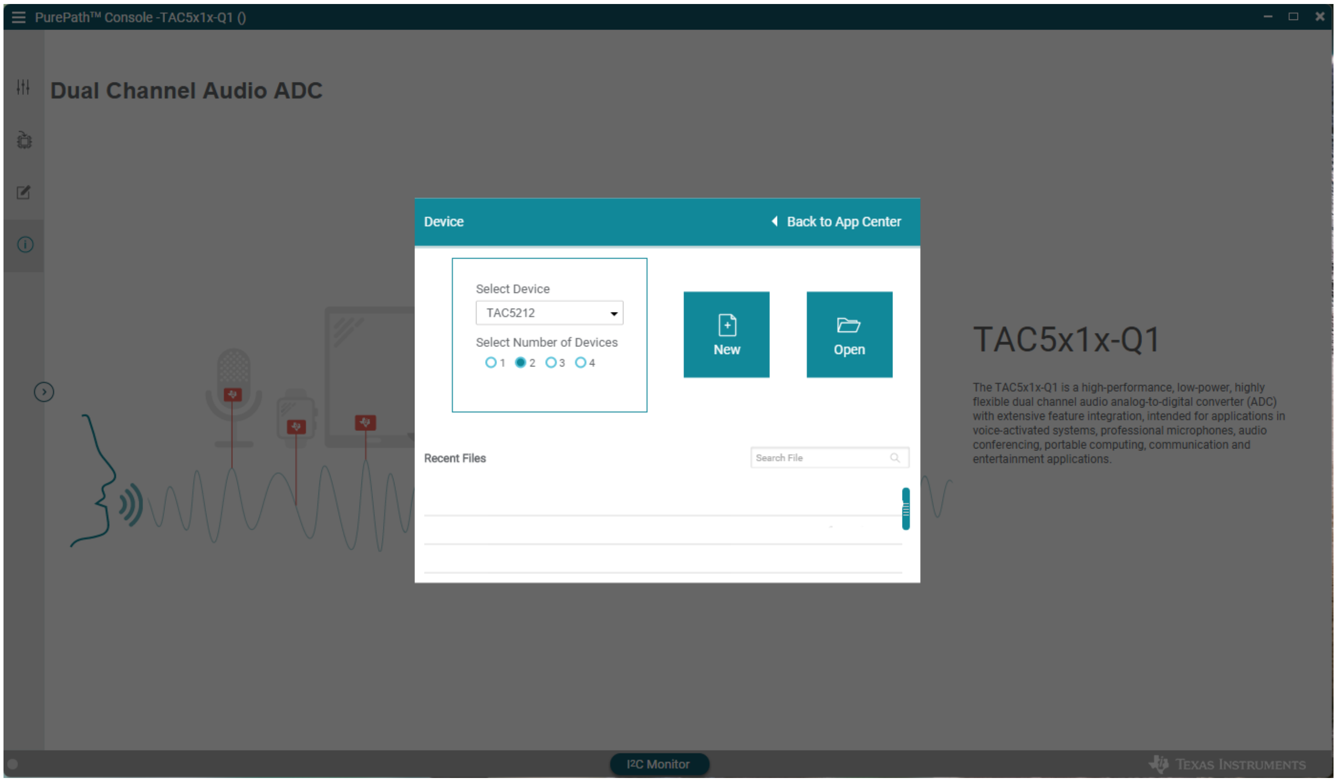

Figure 4-3. PurePath Console Input Number of Devices Dialog

PurePath Console configures only one device at a time. The devices are labeled by a device icon with a letter at the top of the screen, as shown in Figure 4-4. Clicking on device icon A programs the lower number I^2C address, B programs the next I^2C address, and so forth.

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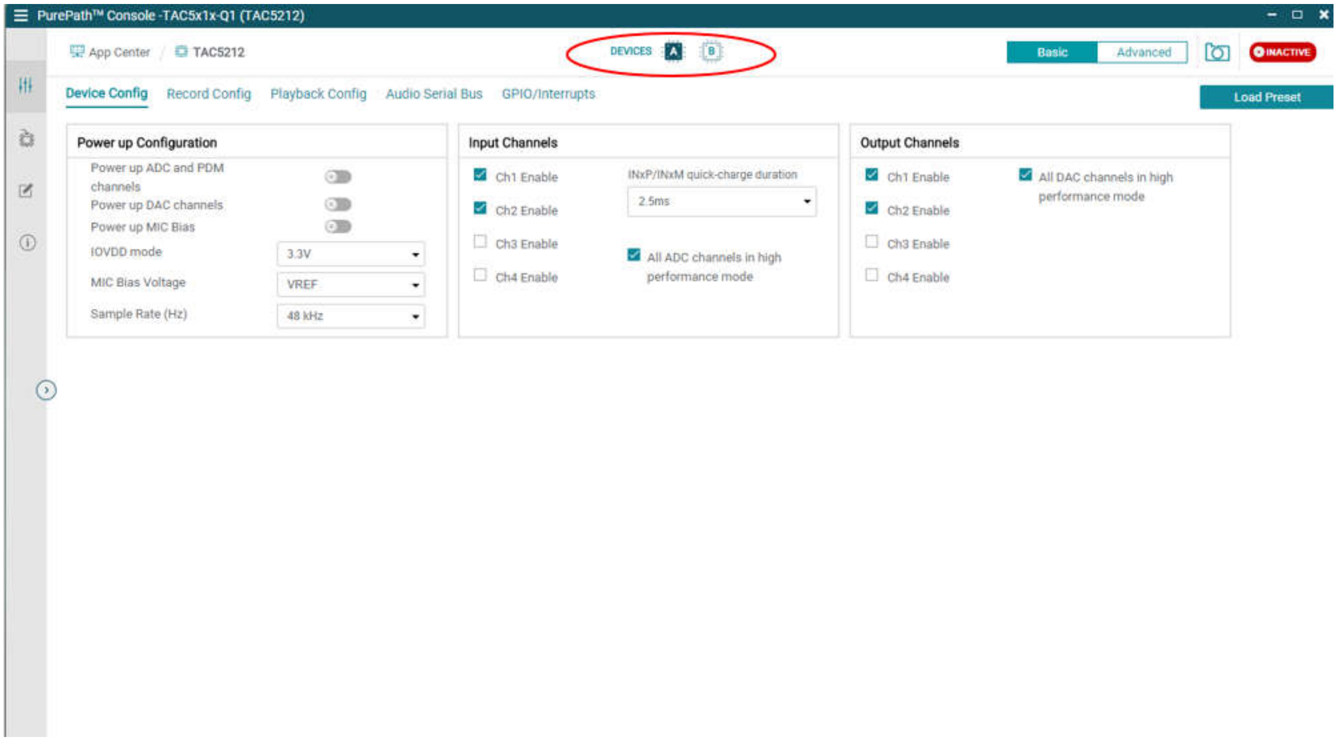

Figure 4-4. PurePath Console Main Window

The Audio Serial Bus tab assigns each channel of a device to a slot. In Figure 4-5, the device A input channels 1-4 are assigned to slots 0-3, respectively. In Figure 4-6, the device B input channels 1-4 are assigned to slots 4-7. Note that the previous slots in the TDM bus are not shown, but an ellipsis at the beginning of the audio interface signal line plot in BCLK, FSYNC, and SDOUT signifies that other slots precede these slots.

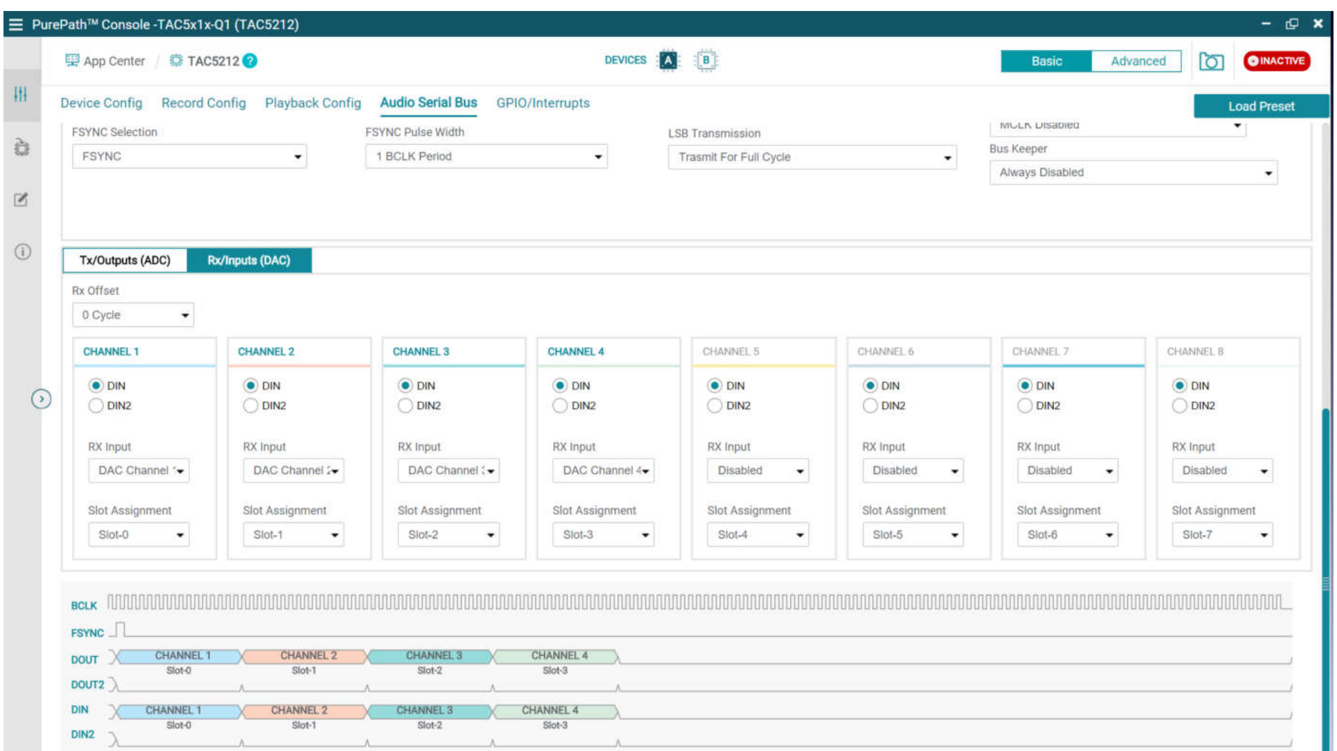

Figure 4-5. PurePath Console Device A Channel to Slot Mapping

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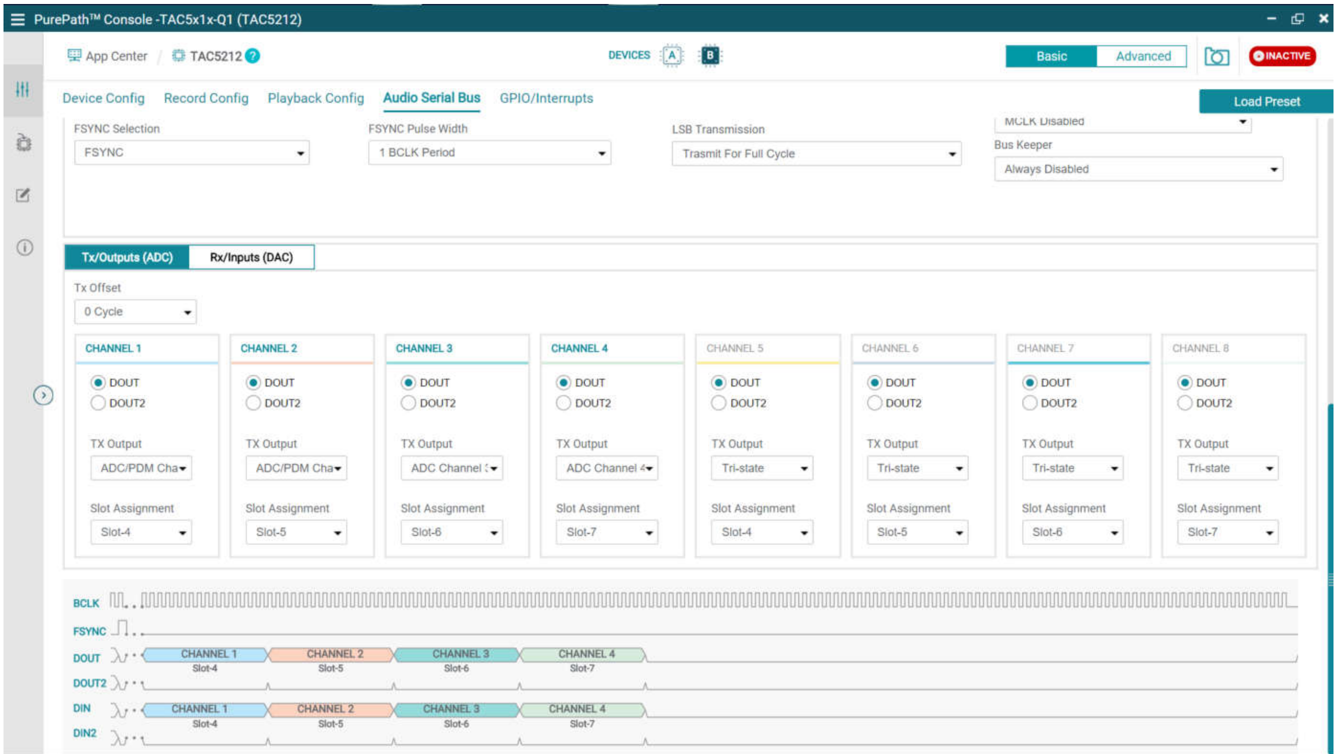

Figure 4-6. PurePath Console Device B Channel to Slot Mapping

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5 PurePath Console I2C Scripts

5.1 TAC5x1x I2C Scripts for Shared TDM

The following I2C scripts sets four devices for shared TDM mode, after devices are reset:

```
# Key: w NN YY ZZ ==> write to I2C address 0xNN, to register 0xYY, data 0xZZ
#                # ==> comment delimiter
#
# I2C programming script for four devices sharing a TDM bus
#  U4(SDOUT) -> U3 (SDOUT) -> U2 (SDOUT) -> U1 (SDOUT) -> Host Processor
#
#########################################################################
# Power-up Sequence:
# Power up IOVDD and AVDD power supplies
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Wait for 2ms.
#########################################################################
# Wake-up devices
w A0 02 09  # Wake-up Device U1
w A2 02 09  # Wake-up Device U2
w A4 02 09  # Wake-up Device U3
w A6 02 09  # Wake-up Device U4
d 10        # 10 ms delay
# Program Device A (U1), interfaces to host processor
w A0 00 00  # Set Device page register to Page 0
w A0 1A 30  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity
w A0 1B 60  # ASI transmit Hi-Z for unused cycles
w A0 1E 20  # ASI primary output (DOUT) with CH1 assigned to slot 0
w A0 1F 21  # ASI primary output (DOUT) with CH2 assigned to slot 1
w A0 20 22  # ASI primary output (DOUT) with CH3 assigned to slot 2
w A0 21 23  # ASI primary output (DOUT) with CH4 assigned to slot 3
w A0 28 20  # ASI primary input (DIN) with CH1 assigned to slot 0
w A0 29 21  # ASI primary input (DIN) with CH2 assigned to slot 1
w A0 2A 22  # ASI primary input (DIN) with CH3 assigned to slot 2
w A0 2B 23  # ASI primary input (DIN) with CH4 assigned to slot 3
w A0 76 FF  # Enable Ch1-4 of Device A
# Program Device B (U2)
w A2 00 00  # Set Device page register to Page 0
w A2 1A 30  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity
w A2 1B 60  # ASI transmit Hi-Z for unused cycles
w A2 1E 24  # ASI primary output (DOUT) with CH1 assigned to slot 4
w A2 1F 25  # ASI primary output (DOUT) with CH2 assigned to slot 5
w A2 20 26  # ASI primary output (DOUT) with CH3 assigned to slot 6
w A2 21 27  # ASI primary output (DOUT) with CH4 assigned to slot 7
w A2 28 24  # ASI primary input (DIN) with CH1 assigned to slot 4
w A2 29 25  # ASI primary input (DIN) with CH2 assigned to slot 5
w A2 2A 26  # ASI primary input (DIN) with CH3 assigned to slot 6
w A2 2B 27  # ASI primary input (DIN) with CH4 assigned to slot 7
w A2 76 FF  # Enable Ch1-4 of Device B
# Program Device C (U3)
w A4 00 00  # Set Device page register to Page 0
w A4 1A 30  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity
w A4 1B 60  # ASI transmit Hi-Z for unused cycles
w A4 1E 28  # ASI primary output (DOUT) with CH1 assigned to slot 8
w A4 1F 29  # ASI primary output (DOUT) with CH2 assigned to slot 9
w A4 20 2A  # ASI primary output (DOUT) with CH3 assigned to slot 10
w A4 21 2B  # ASI primary output (DOUT) with CH4 assigned to slot 11
w A4 28 28  # ASI primary input (DIN) with CH1 assigned to slot 8
w A4 29 29  # ASI primary input (DIN) with CH2 assigned to slot 9
w A4 2A 2A  # ASI primary input (DIN) with CH3 assigned to slot 10
w A4 2B 2B  # ASI primary input (DIN) with CH4 assigned to slot 11
w A4 76 FF  # Enable Ch1-4 of Device C
# Program Device D (U4)
w A6 00 00  # Set Device page register to Page 0
w A6 1A 30  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity
w A6 1B 60  # ASI transmit Hi-Z for unused cycles
w A6 1E 2C  # ASI primary output (DOUT) with CH1 assigned to slot 12
w A6 1F 2D  # ASI primary output (DOUT) with CH2 assigned to slot 13
w A6 20 2E  # ASI primary output (DOUT) with CH3 assigned to slot 14
w A6 21 2F  # ASI primary output (DOUT) with CH4 assigned to slot 15
w A6 28 2C  # ASI primary input (DIN) with CH1 assigned to slot 12
w A6 29 2D  # ASI primary input (DIN) with CH2 assigned to slot 13
w A6 2A 2E  # ASI primary input (DIN) with CH3 assigned to slot 14
w A6 2B 2F  # ASI primary input (DIN) with CH4 assigned to slot 15
w A6 76 FF  # Enable Ch1-4 of Device D
# Power-up Devices A, B, C, & D
w A0 78 C0  # Power up ADC and DAC of Device A
```


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```
w A2 78 C0  # Power up ADC and DAC of Device B
w A4 78 C0  # Power up ADC and DAC of Device C
w A6 78 C0  # Power up ADC and DAC of Device D
```

5.2 TAC5x1x I2C Scripts for Daisy Chain TDM

The following I2C scripts sets four devices for Daisy-Chain TDM mode, after devices are reset:

```
# Key: w NN YY ZZ ==> write to I2C address 0xNN, to register 0xYY, data 0xZZ
#                # ==> comment delimiter
#
# I2C programming script for four devices in daisy chain TDM mode
#  U4(DOUT) -> (GPIO1) U3 (DOUT) -> (GPIO1) U2 (DOUT) -> (GPIO1) U1 (DOUT) -> Host Processor
#
#########################################################################
# Power-up Sequence:
# Power up IOVDD and AVDD power supplies
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Wait for 2ms.
#########################################################################
# Wake-up devices
w A0 02 09  # Wake-up Device U1
w A2 02 09  # Wake-up Device U2
w A4 02 09  # Wake-up Device U3
w A6 02 09  # Wake-up Device U4
d 10        # 10 ms delay
# Program Device A (U1), interfaces to host processor
w A0 00 00  # Set Device page register to Page 0
w A0 1A 30  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity
w A0 1B 60  # ASI transmit Hi-Z for unused cycles
w A0 18 49 # Set U1's ASI to daisy chain via GPIO1
w A0 21 10 # Set U1's GPIO1 input as ASI input for daisy chain
w A0 1E 20 # Set U1 Ch1 mapped to slot 0 of DOUT
w A0 1F 21 # Set U1 Ch2 mapped to slot 1 of DOUT
w A0 20 22 # Set U1 Ch3 mapped to slot 2 of DOUT
w A0 21 23 # Set U1 Ch4 mapped to slot 3 of DOUT
w A0 76 F0  # Enable Ch1-4 of Device A
# Program Device B (U2)
w A2 00 00  # Set Device page register to Page 0
w A2 1A 30  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity
w A2 1B 60  # ASI transmit Hi-Z for unused cycles
w A2 18 49 # Set U2's ASI to daisy chain via GPIO1
w A2 21 10 # Set U2's GPIO1 input as ASI input for daisy chain
w A2 1E 20 # Set U2 Ch1 mapped to slot 0 of DOUT
w A2 1F 21 # Set U2 Ch2 mapped to slot 1 of DOUT
w A2 20 22 # Set U2 Ch3 mapped to slot 2 of DOUT
w A2 21 23 # Set U2 Ch4 mapped to slot 3 of DOUT
w A2 76 F0  # Enable Ch1-4 of Device B
# Program Device C (U3)
w A4 00 00  # Set Device page register to Page 0
w A4 1A 30  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity
w A4 1B 60  # ASI transmit Hi-Z for unused cycles
w A4 18 49 # Set U3's ASI to daisy chain via GPIO1 w A4 21 10 # Set U3's GPIO1 input as ASI input
for daisy chain
w A4 1E 20 # Set U3 Ch1 mapped to slot 0 of DOUT
w A4 1F 21 # Set U3 Ch2 mapped to slot 1 of DOUT
w A4 20 22 # Set U3 Ch3 mapped to slot 2 of DOUT
w A4 21 23 # Set U3 Ch4 mapped to slot 3 of DOUT
w A4 76 F0  # Enable Ch1-4 of Device C
# Program Device D (U4)
w A6 00 00  # Set Device page register to Page 0
w A6 1A 30  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity
w A6 1B 60  # ASI transmit Hi-Z for unused cycles
w A6 1E 20 # Set U4 Ch1 mapped to slot 0 of DOUT
w A6 1F 21 # Set U4 Ch1 mapped to slot 1 of DOUT
w A6 20 22 # Set U4 Ch1 mapped to slot 2 of DOUT
w A6 21 23 # Set U4 Ch1 mapped to slot 3 of DOUT
w A6 76 F0  # Enable Ch1-4 of Device D
# Power-up Devices A, B, C, & D
w A0 78 C0  # Power up ADC and DAC of Device A
w A2 78 C0  # Power up ADC and DAC of Device B
w A4 78 C0  # Power up ADC and DAC of Device C
w A6 78 C0  # Power up ADC and DAC of Device D
```


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