Application Brief

Achieving Higher Output Current by Stacking TPS546E25 and TPS546C25 DC/DC Converters

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Introduction

The TPS546E25 and TPS546C25 synchronous buck converters provide the ability to link multiple devices to share a common output. When *stacked* in this way, the devices can share current, synchronize switching frequencies and shift out-of-phase to reduce input and output ripple noise while providing higher levels of output current.

Stacking is achieved by connecting the TRIGGER and ISHARE pins of the devices to be stacked together. In addition, the GOSNS and VOSNS pins of all devices need to be connected to the same point at the load.

Programming MSEL1 and MSEL2 Pins

One of the devices needs to have the MSEL1 pin connected to the AGND with a resistor selecting the desired per device current limit, feedback selection (internal versus external), fault response, and soft-start time. This device is the *primary* – each stack must only have 1 primary. Each additional device needs to have the MSEL1 pin floating (>412kΩ to AGND) to select a secondary device.

The primary device uses MSEL2 to select the switching frequency and compensation options for V_{RAMP} and gain. As with single-phase operation, the switching frequency is *per phase* so a 3-phase stack operating at 800kHz can have an input ripple and output ripple frequency of 3 × 800kHz = 2.4MHz.

Secondary devices use the MSEL2 pin to select switching frequency and the phase current limit. Since each device is operating constant on-time generator, all devices in the stack have the same switching frequency selected is important. Selecting different switching frequencies can prevent current sharing from working and result in a large phase current imbalance.

Programming VSEL/FB pin

The primary device uses the VSEL/FB pin to set the regulated output voltage. When using the internal feedback divider, a single resistor from VSEL/FB to AGND sets the internal divider ratio (VOUT_SCALE_LOOP) and reference voltage (VBOOT) to set the power-on output voltage. When using the external feedback divider, a top resistor is placed from VOSNS to VSEL/FB and a bottom resistor is placed from VSEL/FB to AGND. Along with the reference voltage, this sets the output voltage as:

$$V_{OUT} = V_{REF} \times (1 + R_{TOP}/R_{BOT}) \quad (1)$$

Secondary devices use the VSEL/FB programming pin to setup the internal feedback divider on VOSNS for the on-time generator. When using the internal divider, secondary devices need to use the same VSEL resistor as the primary. When using an external divider, secondary devices need to use a VSEL resistor that selects the closest available V_{OUT} to the value which can be selected by the feedback divider.

Programming the PBM_ADDR/VORST# pin

Both primary and secondary devices use the PMB_ADDR/VORST# pin to program the devices stacking configuration and PMBus® addresses. For proper operation of the multi-phase stack, only the recommended pairings of PMB_ADDR/VORST# resistor options are used. All devices are programmed with the same *common*

address, the primary device is programmed to trigger the correct number of secondary devices, and each secondary device has a different unique PMBus address, which also assigns the TRIGGER order.

Stacking With D-CAP4 Control Architecture

The D-CAP4 control loop operates in multi-phase much like this does in single phase. Each stacked converter operates on-time generator, which produces an on-time according to the programmed switching frequency, sensed input voltage, and sensed output voltage. The primary device can operate the loop for all devices in the stack, sending out a trigger pulse to secondary devices to start the devices on-time generator.

For regulation, the primary device operates a single fixed amplitude ripple emulation ramp (V_{RAMP}) for the entire loop. This produces an effective ramp voltage of N × V_{RAMP} at the per-phase switching frequency.

Due to this N_x scaling of the ramp voltage, the transient performance of a multi-phase stack can be similar to a single-phase operating with the same compensation. This simplifies the design equations and allows designers to scale the number of phases more easily to adapt to the load current and thermal environment requirements without having to redesign the compensation options.

Note

In theory, the additional switching frequency afforded by the multiple phases can allow a higher loop bandwidth than can be achieved with single phase operation. In practice, however, this higher bandwidth comes as the cost of reduced dynamic phase current sharing, so while this is possible to reduce the output capacitance of a multi-phase stack and maintain steady-state stability, this is generally not recommended.

Inductor Selection

All phases within a stack must have the same inductor value. The ISHARE loop can compensate for normal part to part variations of inductance, but is not intended to compensate for different nominal inductor values.

Inductor Connections

Since the primary device monitors the output voltage at a single point and uses the output voltage ripple along with the internal ripple for phase triggering, the outputs of the inductor needs to be merged into a single connection before the output capacitors. Layouts where the inductor outputs are kept separate with separate per-phase capacitors before merging to the shared output have shown unbalanced phase timing, which increases the output ripple.

PVIN Connections

The D-CAP4 stack-able architecture is intended to operate with a common PVIN voltage. The recommendation is that all devices operating in a stack share a common input voltage.

Control Line

All devices in the stack needs to share a common CNTRL line. If any device within a stack is not enabled, the stack is not enabled.

VOSNS and GOSNS Pins

As noted, all devices within a stack need to have the VOSNS and GOSNS pins connected to the same point. The VOSNS pin is used to sense the output voltage for the per-phase On-time generator while the GOSNS pin provides a *virtual ground* for ISHARE. Failure to connect VOSNS and GOSNS to the same point can negatively affect current sharing.

Communicating With Devices in the Stack

Each device in the stack has both a Common Address and a Unique Address. Stacked devices can be communicated with normally using the devices unique address, or the devices can be communicated with through the Common Address using the P2_PLUS_READ and P2_PLUS_WRITE commands. When using the P2_PLUS commands, the PAGE value need to be set to FFh (All Pages) or 00h (Page 0) no other pages are supported. The PHASE value can be FFh (All Phases) or 00h, for the primary, or 01h – 03h for the First, Second, or Third secondary device. When reading from PHASE = FFh, the primary device responds for all phases, scaling current responses by the number of phases.

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