*Application Note*

# *Restart Problem and Solution for DC Brushed Motor Driver DRV8231*

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**ABSTRACT**

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BDC motors (brushed DC motors) are widely used in the home appliance field. Due to their simple structure, low cost, and ease of control, they have become the core driving components of traditional home appliances. Common applications include: washing machine pulsator drive, achieving clothes washing through forward and reverse rotation; refrigerator compressor auxiliary fan, maintaining stable internal temperature; vacuum cleaner motor, providing high-speed airflow; high torque power output for juicers and blenders; microwave oven turntable motor, achieving uniform heating; dishwasher pump motor driving water circulation, etc. BDC motors excel in low-speed, high-torque applications, making them ideal for devices that prioritize consistent power delivery over high rotational speeds. Although BDC motors exhibit slightly higher noise levels and shorter lifespans compared to Brushless DC (BLDC) motors, they remain highly competitive in cost-sensitive appliance applications, particularly dominating the mid-to-low-end market segment. As technology advances, certain high-end appliances are gradually transitioning to more efficient brushless motors. However, thanks to their mature technology and excellent cost-effectiveness, BDC motors are expected to remain a viable and active solution in the short term [1] .

This article mainly discusses the restart problem caused by accidentally entering TEST Mode during the use of BDC motor drivers, taking DRV8231 as an example. It first introduces the basic principles of BDC motor drivers, then elaborates in detail on the reasons for entering TEST mode, the behavior, and the methods to exit TEST mode. Furthermore, it proposes some improvement measures for the chip's anti-interference capability to avoid the chip erroneously entering TEST mode, aiming to provide reference for other designers of BDC drivers such as DRV8231.

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# 1 Fundamentals of BDC Driver DRV8231

Figure 1-1 is the typical schematic block diagram of a BDC motor. The working principle of the BDC motor is based on the law of electromagnetic induction and the mechanical commutation mechanism. Fundamentally, its operation is driven by the dynamic interaction between the magnetic fields generated by the stator and the rotor. The motor consists of three parts: the stator, the rotor, and the commutator (brush). The stator generates a fixed magnetic field through permanent magnets or field windings. The rotor is formed by armature windings wound around an iron core and is supported by bearings to rotate. The commutator has a segmented copper ring structure, and the brushes serve as sliding contacts to connect the external power source with the armature windings. As current passes through the brushes into the armature windings, the conductors intersect the stator's magnetic field. In accordance with the left-hand rule, this interaction generates an electromagnetic force that drives the rotor's rotation. To achieve maximum torque, the magnetic field induced by the armature windings is maintained perpendicular to the stator's magnetic field. To maintain continuous rotation, the commutator, which rotates synchronously with the rotor, switches the brush contact position when the winding passes through the neutral plane. This forces the reversal of the armature current direction, ensuring that the armature magnetic field and the stator magnetic field always maintain a 90° phase difference. The rotational speed is directly proportional to the armature voltage, enabling seamless speed control via Pulse Width Modulation (PWM). The torque is determined by the armature current and follows the equation T = Kt × I. When the load increases, the armature current automatically rises to maintain torque balance. The mechanical contact between the brushes and the commutator causes friction loss and sparking phenomena, which limits the motor's lifespan and maximum rotational speed, but also endows it with the advantages of high starting torque and strong overload capability.

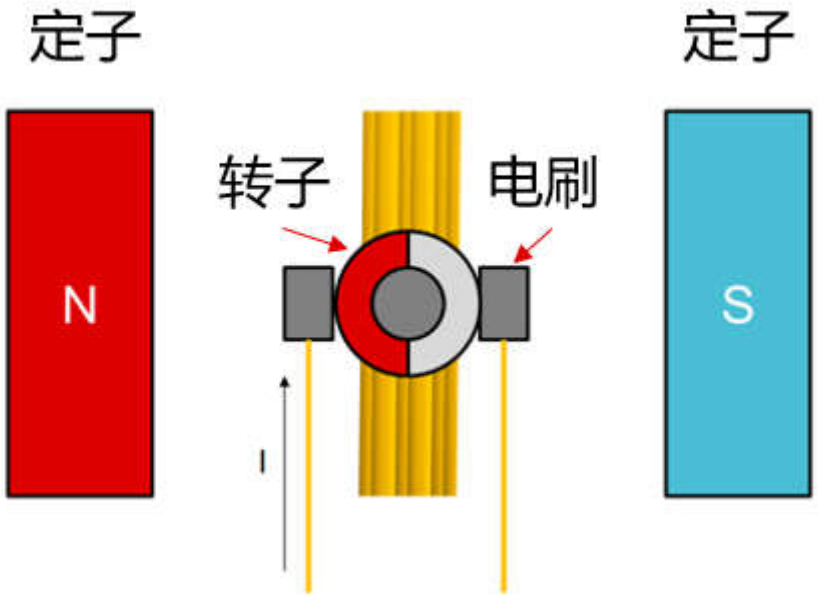


**Figure 1-1. Typical Schematic Block Diagram of a BDC Motor**

Figure 1-2 is the internal functional block diagram of DRV8231, which internally integrates H-bridge motor driver, charge pump, over-current protection, under-voltage protection, over-temperature protection, H-bridge driver and more. The charge pump improves efficiency and provides the capability of 100% duty cycle for driving N-channel MOSFET half-bridge. It compares the current flowing through RSENSE with VREF to control the half-bridge circuit, realizing constant-current driving of the BDC motor.

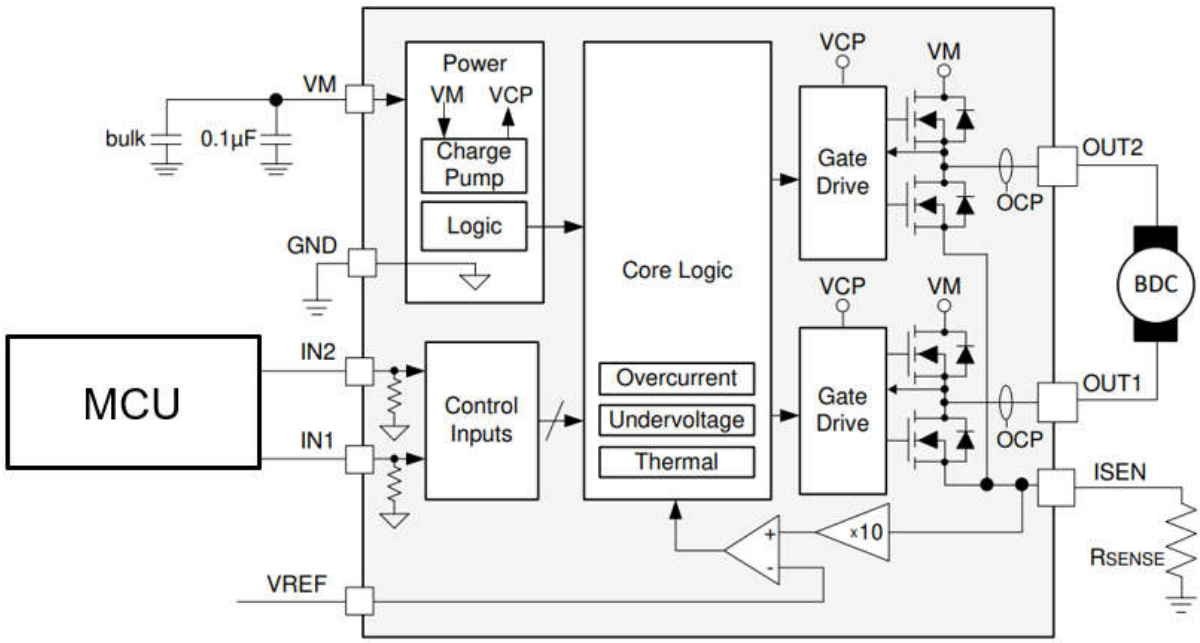


**Figure 1-2. Internal Functional Block Diagram of DRV8231**

The MCU controls the driving of Coil1 and Coil2 via the IN1 and IN2, as defined in the truth table Table 1-1. Referring to Figure 1-3, when driving Coil1, OUT1 is low (VOUT1 = GND), applying the VM voltage across Coil1 to drive its rotation. Simultaneously, OUT2 is high (VOUT2 = VM), ensuring no current flows through Coil2, vice versa.

**Table 1-1. Truth Table for IN1 and IN2 Driving**

| IN1 | IN2 | OUT1 | OUT2 | Description |
|---|---|---|---|---|
| 0 | 0 | High impedance | High impedance | H-bridge not enabled |
| 0 | 1 | Low | High | Driving Coil1 |
| 1 | 0 | High | Low | Driving Coil2 |
| 1 | 1 | Low | Low | Driving both |

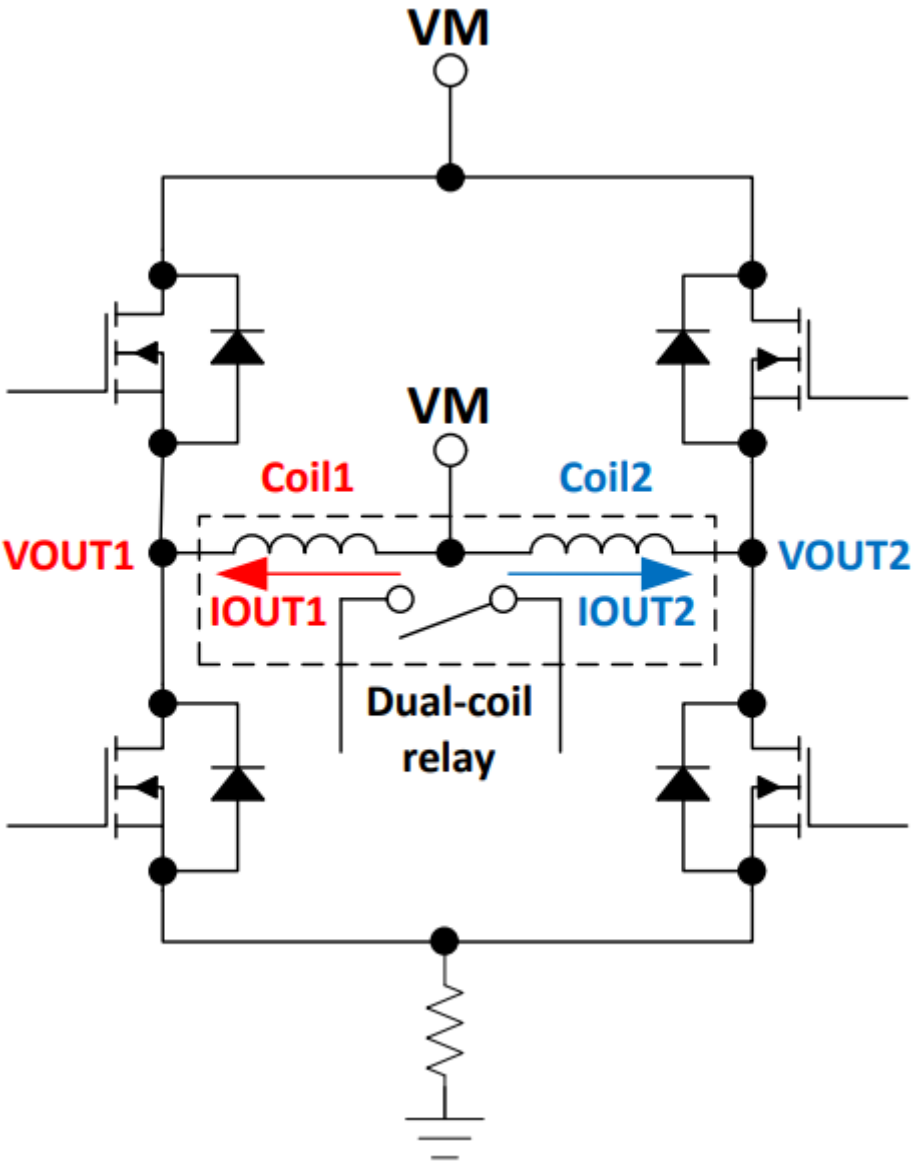


**Figure 1-3. IN1 and IN2 driving logic**

## 2 DRV8231 Restart Behavior and Test Mode Analysis

We received feedback from customers using the DRV8231 that during the operation of the whole device, the motor may occasionally stall and do not move. At this time, if the device is powered off and restarted, the fault can be recovered. However, performing a full power cycle is often impractical across various customer applications. For instance, in kitchen range hoods, the power outlet is typically located at a significant height after installation, making repeated plugging and unplugging highly inconvenient for end users. Consequently, this workaround is unacceptable to both end consumers and OEMs. Therefore, it is imperative that we identify the root cause of the issue and provide a solution for our customers.

Taking the following case as an example, customers found that during the use of DRV8231, after a certain power-on of the same chip, the BDC motor could not be driven and was accompanied by low-frequency noise. After the whole device was powered off and restarted, the problem could be fixed. Due to the low-frequency noise from the motor, we first suspected abnormal output current from the DRV8231. We captured the OUT output current waveform as shown in Figure 2-2. The green waveform is the VM voltage of 15V, the yellow waveform is the BDC motor current waveform, and the blue one is the REF waveform. It can be seen that when the load current reaches 200mA, the DRV8231 output current drops to zero. After 3ms, the DRV8231 restarts.

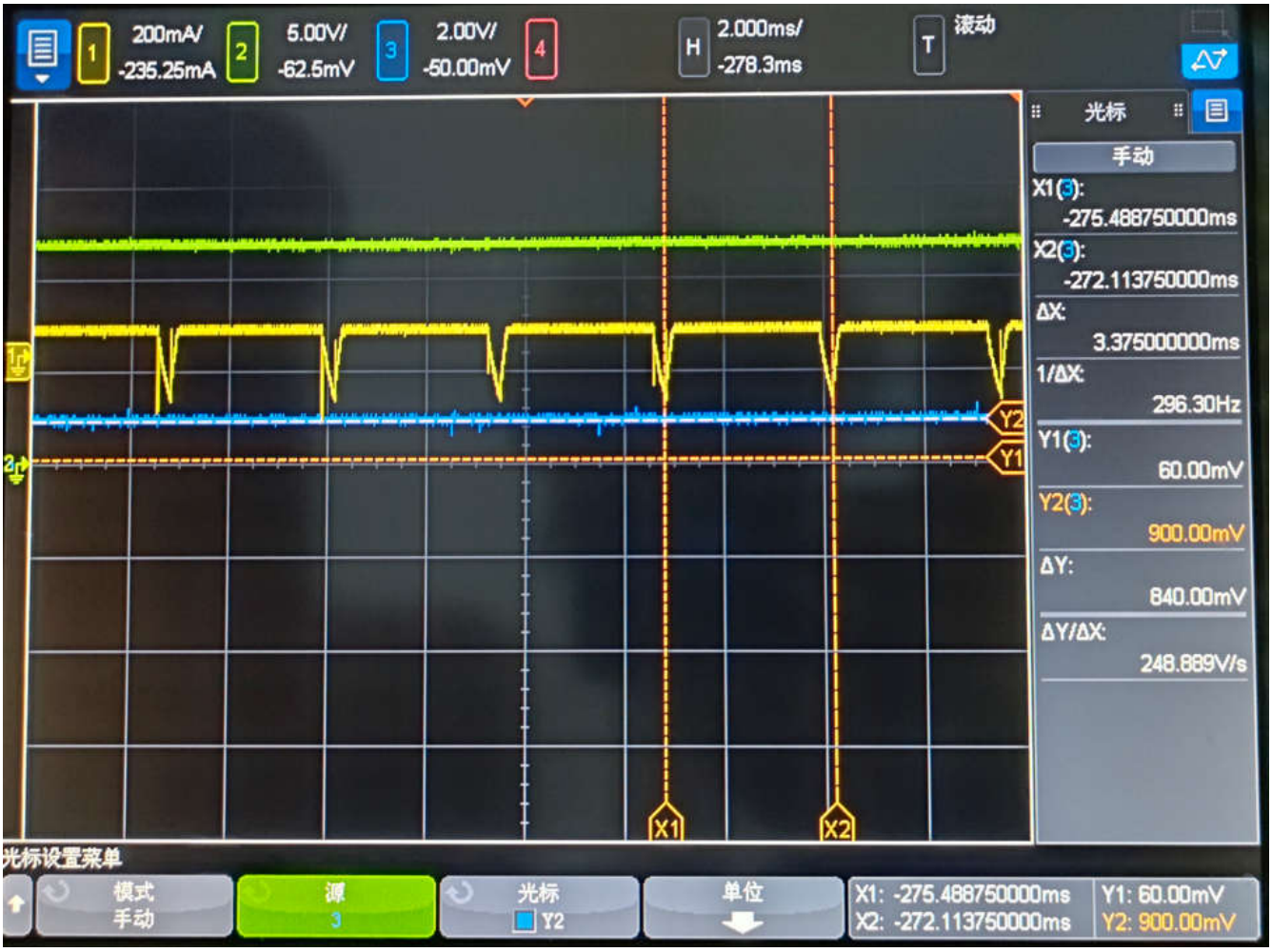


**Figure 2-1. DRV8231 Restart Behavior Waveform**

Based on the behavior of repeated restarting according to the current waveform, we suspect it is related to two current-related features of the DRV8231: one is the Itrip control feature, and the other is the OCP overcurrent protection feature. Let us begin by introducing and analyzing the Itrip control feature:

For the Itrip control feature, the DRV8231 internally samples the Rsense resistor through an op-amp with a fixed gain of 10, and compares it with the voltage at the Vref pin to maintain the ISEN voltage near Vref. Simply put,

the DRV8231 controls the current Itrip flowing through the BDC motor by controlling the voltage across both sides of the Rsense resistor [2] .

$$Itrip = \frac{Vref}{10*Rsense} \quad (1)$$

The BDC current continues to rise during the tblank time. After tblank, until the current reaches Itrip, the two high-side tubes are turned off and the two low-side tubes are turned on, entering the slow decay mode. Itrip is set via the peripheral hardware of Vref and Rsense. By inspecting the PCB board, the schematic, and the final REF waveform, it was found that the REF voltage and the Rsense resistor are set correctly. Vref is set to 1.1V through 5V and voltage division by resistors of 62kohm and 220kohm. Rsense is a 0.12ohm resistor in 2010 package. Itrip is calculated by equation to be 0.92 A. Also, if Itrip is falsely triggered, the restart time should be toff+tblank=25us+2us=27us. Therefore, this restart behavior is not consistent with the description in the datasheet.

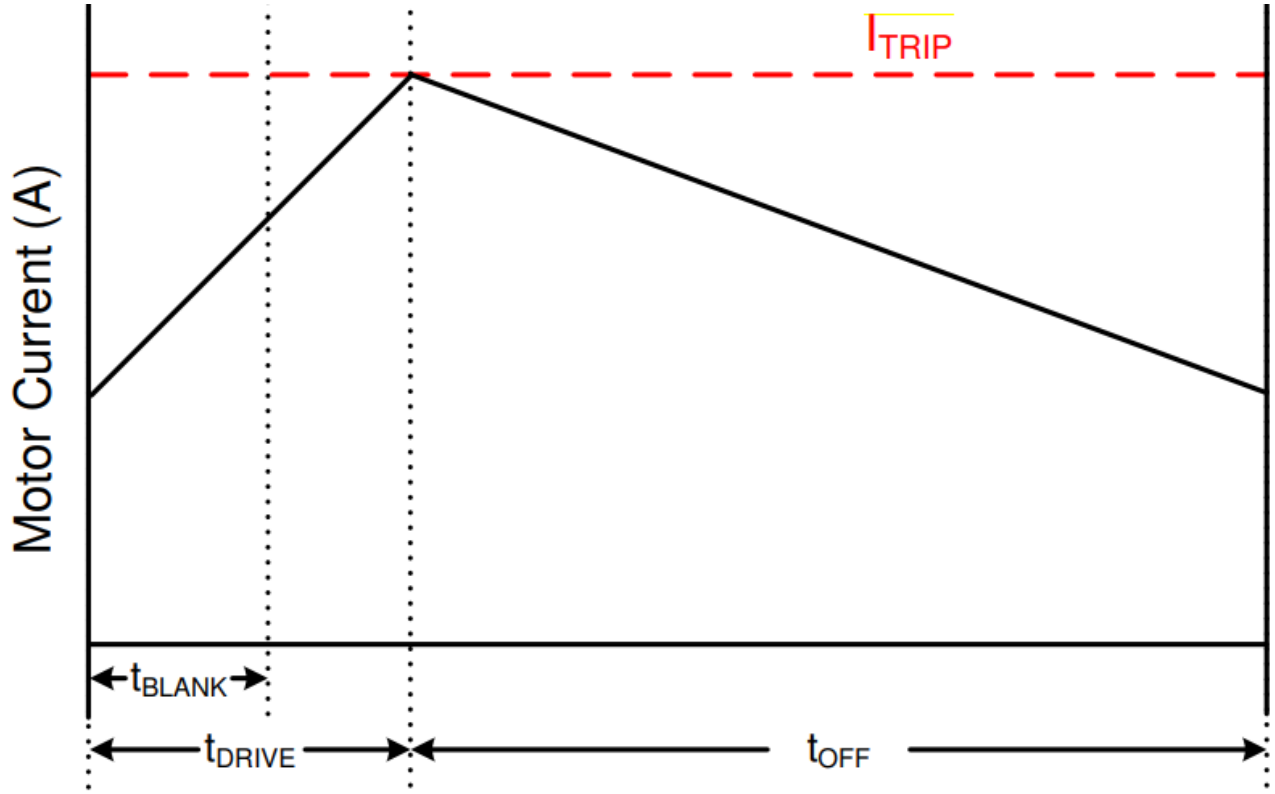


**Figure 2-2. Itrip Modulation Operation Mechanism**

Regarding the OCP over-current protection feature, unlike Itrip, OCP directly samples the half-bridge midpoint current and feeds it to the internal control core. When the BDC current is greater than Iocp=3.7A and the duration exceeds tocp=1.5us, all internal FETs will be turned off. After tretry=3ms, the BDC motor is re-driven. If the over-current fault still exists, it will cycle repeatedly as shown in the Figure 2-3 below, which is similar to the fault waveform.

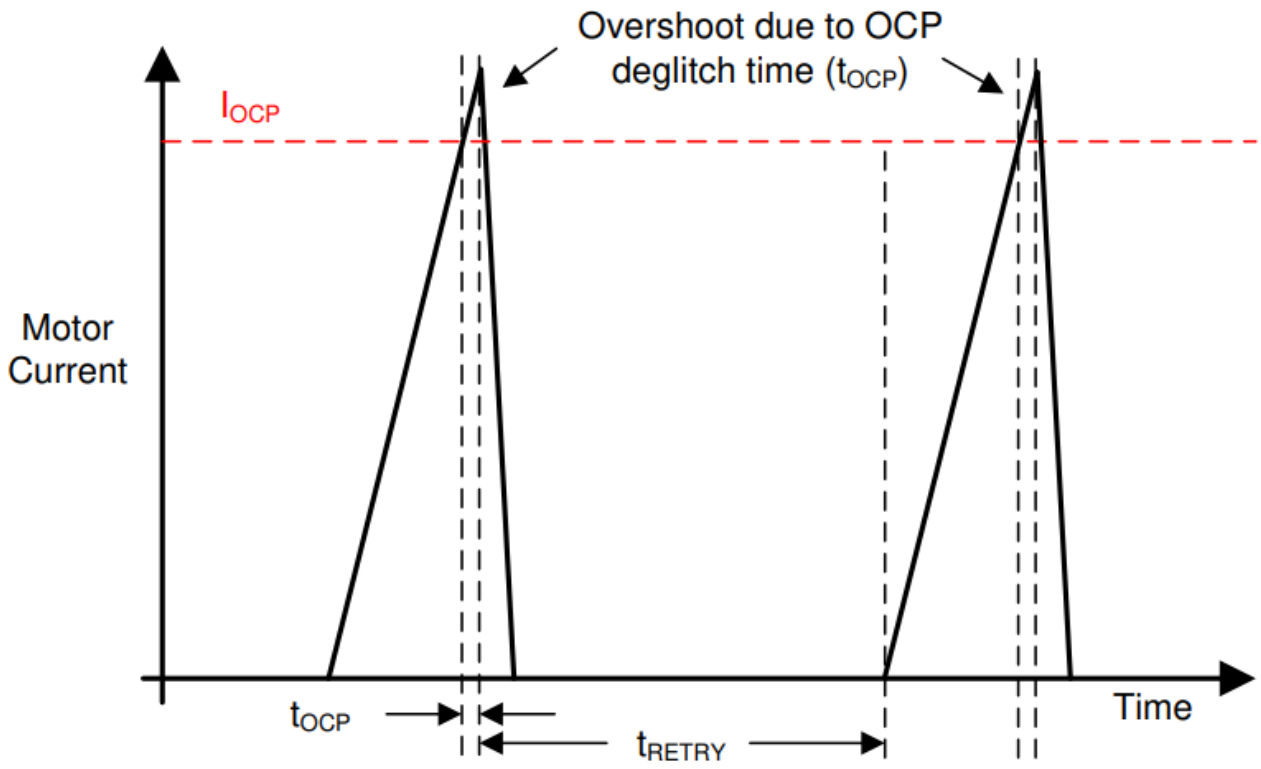


**Figure 2-3. OCP Protection Operation Mechanism**

Based on the above analysis of Itrip and OCP, the restart caused by Itrip is ruled out. However, the fault waveform is similar to the OCP waveform. In terms of time scale, the restart time captured by the oscilloscope and the OCP restart time tretry are both 3ms. However, at the over-current protection current point, Iocp is 3.7A, while the fault waveform captured by the oscilloscope is only 200mA. Following internal verification with the Business Unit (BU), it has been confirmed that the DRV8231 has entered Test Mode. This mode is designed to bypass standard operational sequences, either during pre-shipment validation or fault diagnosis, to safeguard internal circuit logic. Its primary objective is to streamline the detection of potential manufacturing defects or functional anomalies. And the test mode of DRV8231 will reduce the OCP protection point from 3.7A to 200mA, which is consistent with the phenomenon captured by the oscilloscope.

Following discussions with the product line team, it is confirmed that the DRV8231 has two test modes that will affect the output, as shown in Table 2-1 below. Regarding the entry method, a disturbance on IN1 and IN2 at the nanosecond level is sufficient to enter test modes. When IN1 is greater than 7.5V and IN2 is less than 7.5V, the device enters TM_OCPLS mode, where Iocp will drop from 3.7A to around 200mA. When IN1 is less than 7.5V and IN2 is greater than 7.5V, the device enters TM_OTS mode, where the output voltages are all high level. Regarding the exit method, TM_OCPLS mode can be exited by modifying the software to force the DRV8231 into sleep mode, or by power cycling. However, TM_OTS mode can only be exited by power cycling.

In summary, since the OCP current dropped from 3.7A to around 200mA in this case, and the behavior was reproduced in the lab through ESD experiments, it can be confirmed that the DRV8231 was subjected to external interference in the field and entered the first test mode. The customers exited the test mode by power cycling. However, for the second test mode, there is still a risk of entering it due to interference, and it cannot be exited via software.

**Table 2-1. Methods for Entering and Exiting Test Modes**

| IN1>7.5 | IN2>7.5V | Test Mode | Behavior | Exit Method |
|---|---|---|---|---|
| Yes | No | TM_OCPLS | Iocp drops from 3.7A to 200mA, while other logics remain normal. | To exit the test mode , set IN1:IN2=0:0 to enter Sleep Mode, and then apply a normal drive signal. Alternatively, the test mode can be exited by power cycling of the DRV8231. |
| No | Yes | TM_OTS | The OUT output is always high. | The test mode can only be exited by power cycling of the DRV8231. |

# 3 Solutions for Test Mode and Measured Waveforms

From the analysis of test modes above, if the first test mode is entered, it can be avoided by modifying the control logic, that is, inserting a 6ms 0:0 at IN1 and IN2 to exit the test mode to avoid restart; if the second test mode is entered, it can only be exited by power cycling, which is unacceptable in many practical applications. Finally, TI decided on the roadmap planning for DRV8231 and derivatives such as DRV8251/DRV8870, and made the following optimizations for test modes.

1. Regarding the entry method, since previously ns-level glitch greater than 7.5V would cause the DRV8231 to enter test modes, TI added deglitch circuits inside IN1 and IN2 to improve anti-interference capability. Therefore, when glitch time < 1.9us, the DRV8231 will not enter test modes. The comparison test is as follows: As shown in Figure 3-1, after adding the deglitch circuit internally, applying 10V on IN2 for 1.8us did not cause the chip to enter test modes; as shown in Figure 3-2, applying 10V on IN2 for 2us caused the DRV8231 to enter the second test mode, with OUT1 and OUT2 outputting high level simultaneously.

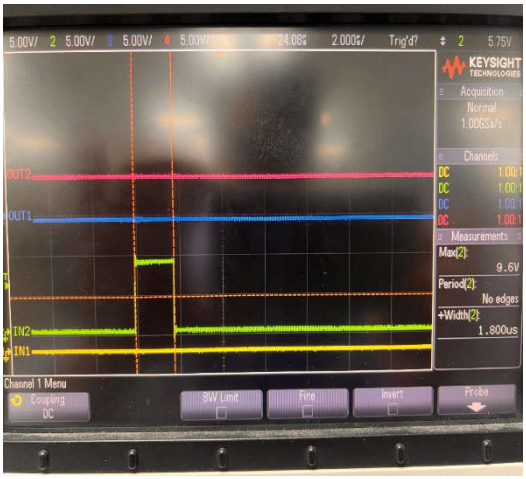


**Figure 3-1. Test Mode Not Entered with 1.8us 10V IN2**

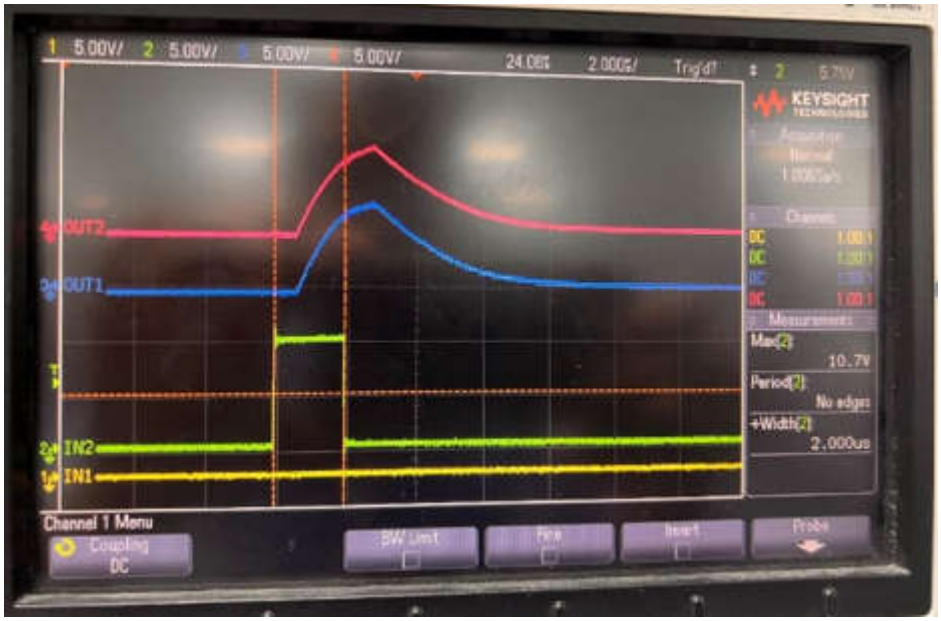


**Figure 3-2. Test Mode Entered with 2us 10V IN2**

2. Regarding the exit method, even if the DRV8231 receives glitch >1.9us and enters the second test mode, as long as IN1 and IN2 are restored to the normal 5V level, the DRV8231 can exit from the test mode. As shown in Figure 3-3, when IN2 increases from 5V to 10V, the DRV8231 enters the second test mode, with

OUT1 and OUT2 reaching high level simultaneously; as shown in Figure 3-4, when IN2 recovers from 10V to 5V, the DRV8231 exits the test mode, with OUT1 high and OUT2 low, and the BDC motor operates normally.

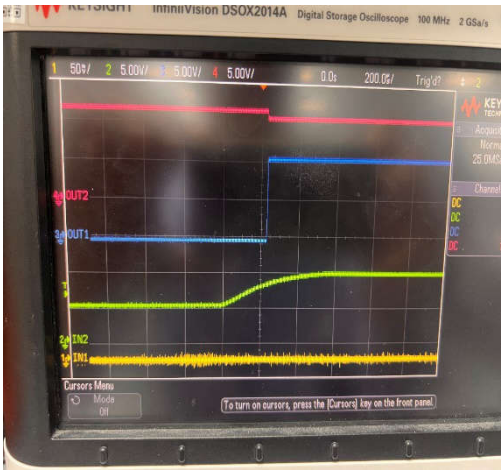


**Figure 3-3. DRV8231 Entering Test Mode with 10V IN2**

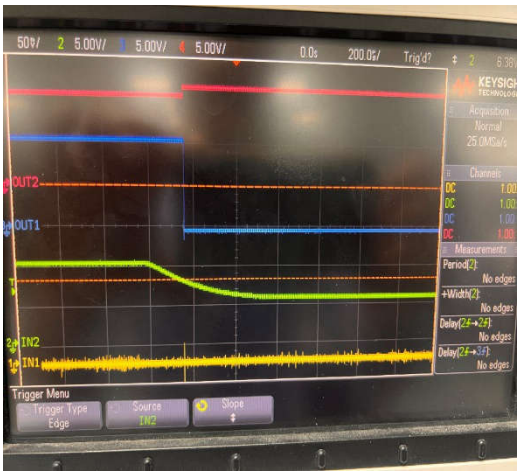


**Figure 3-4. DRV8231 Exiting Test Mode with IN2 Recovering from 10V to 5V**

## 4 Summary

This article analyzes the abnormal restart problem of DRV8231 and reveals the operating logic of the test mode of DRV8231 and the unreasonable entry and exit mechanism. The internal deglitch circuit of the DRV8231 was modified to add 1.9us deglitch logic for greater reliability, and an exit mechanism was added for the second test mode to exit without a power cycle. This lowers the barrier to entry for future designers and provides a clear idea of debugging.

## 5 References

1. Brushless DC Motor Market Size and Future Outlook. Brushless DC Motor Market Size Boosts 10.88% CAGR by 2034
2. DRV8231 Datasheet. SLVSFZ7

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