Application Note

TPS7B7702-Q1 Reverse Current Protection

Given Ding

ABSTRACT

This document was translated from a simplified Chinese source. (ZHCAG84)

The TPS7B7702-Q1 is a widely used antenna LDO that supports a wide input range and integrates various sensing and protection features. Its Vsense pin can be used for current sensing and fault reporting, and it requires an external capacitor for compensation; otherwise, oscillation may occur. This article explains the detection mechanism of reverse overcurrent protection in detail and presents the analysis and avoidance solutions based on the issues that arise in real-world applications.

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1 Profile of TPS7B7702

The TPS7B7702-Q1 is an antenna LDO that supports a wide input voltage range (4.5-40V). It can be connected directly to a 12V battery input (to adapt to voltage fluctuations caused by conditions such as cold boot or load dump). It commonly supplies a stable voltage output via coaxial cables to loads such as low-noise amplifiers in active antennas. It offers excellent diagnostic and protection features, using the sense and Error pins to characterize failures such as output short-circuit, output short-to-battery, overtemperature, and reverse current. Its sense pin can also characterize the current actually flowing by mirroring the current source, which helps customers save on external shunt resistors without affecting the LDO's dropout voltage. The following figure shows a typical application circuit.

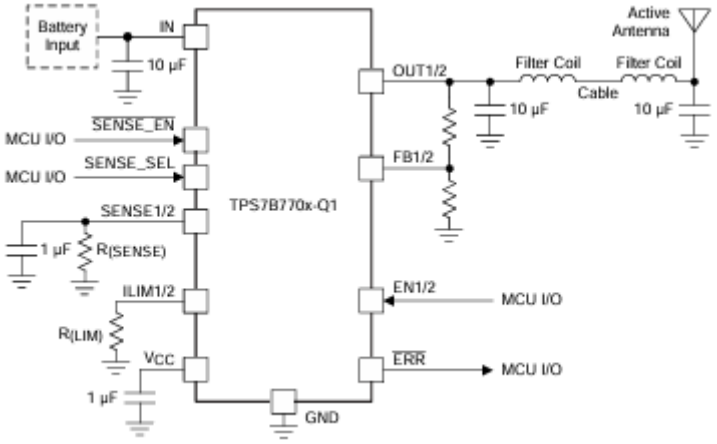

Figure 1-1. TPS7B7702-Q1 Typical Application Block Diagram

There are a few points to note when designing the actual circuit, which are introduced in the corresponding sections of the reference datasheet:

1. For the input capacitor, the datasheet recommends a nominal value of 10uF and does not specify a minimum effective capacitance. The input capacitor is intended to prevent the triggering of undervoltage protection due to output voltage dropping during load transients. In general, when the input supply impedance is greater than 0.5 ohms, an input capacitor is required. For a dual-channel LDO like the 7702, when one channel's output is shorted to ground, the energy stored in the input capacitor is momentarily drawn, causing a transient drop. This may trigger reverse overcurrent protection on the other channel, thereby affecting its normal operation. Considering this condition, a larger input capacitor would be better.
2. The dual-channel LDO can also be connected in parallel to increase current capability. TI offers a reference design, TIDA050096, for reference. This device can also be used in single-channel mode; the corresponding EN pin can be left floating, as there is an internal pull-down on the pin. Unused pins can be left floating or connected to ground. Grounding is recommended to improve the thermal dissipation of the chip.
3. In the EVM for this device, a ferrite bead is placed at the output, similar to the figure above. This bead is not required and is originally intended to simulate an inductive clamping feature. Placing a bead is also fine, which essentially adds an extra stage of LC filtering.

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2 Vsense Waveform

In practical applications, the device's Vsense pin can be used to sense the current flowing through the LDO. This pin may be left floating to simplify the design if the feature is not needed. However, this pin can also characterize the failure type when an issue occurs. Therefore, customers often measure the voltage on this pin to identify the failure type when troubleshooting.

When this pin is left floating, oscillation on the Vsense voltage is observed at power-up. This behavior is normal. The datasheet specifies that a 1uF capacitor connected to ground is required on this pin for frequency compensation. In other words, the current sensing circuit needs an external capacitor to ensure a stable output and proper operation within the specified bandwidth. The oscillation observed is sinusoidal, which is caused by insufficient loop stability. Even if SENSE_EN and SENSE_SEL are both pulled low and the current sense function is disabled, the Vsense pin may still oscillate if no external capacitor is connected. Therefore, it is not available for diagnosing the failure in this state. However, the oscillation does not affect device reliability as long as the pin voltage is within the recommended range.

Figure 2-1. Startup Waveform

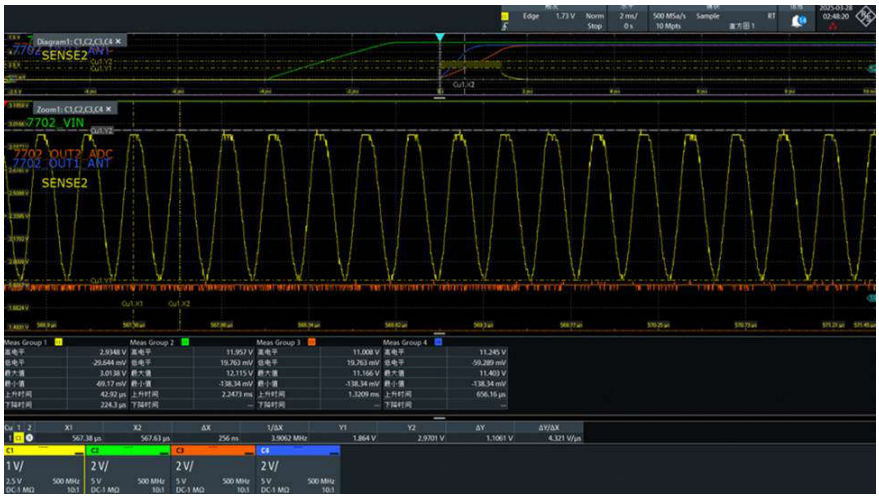

Figure 2-2. Amplified Startup Waveform

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3 Reverse Overcurrent Protection

The device integrates complete oscillation and protection features. The following figure shows a practical application block diagram where the values of the input capacitor and the output capacitors on two channels are close. Vout1 is loaded, and Vout2 is unloaded. The device input is directly connected to the 12V battery. The output voltage is set to 12V.

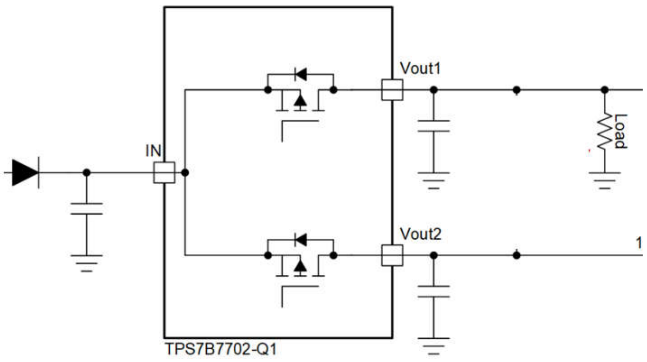

Figure 3-1. Real-World Use Case

In the input voltage drop test, which simulates scenarios such as a car startup, it was found that when the input voltage dropped to 5V and was maintained at this level for approximately 100ms before returning to 9V, the output of Channel 2 was latched off, as shown in the figure. If Channel 2 was somewhat loaded, there would not be such an issue.

Figure 3-2. Output Channel 2 (No Load) Latch-off After the Input Voltage Drops and Recovers

In the event of this issue, the output was found to be latched off, and troubleshooting should be done in conjunction with the failure table in the datasheet. Therefore, first troubleshoot the voltage across the Vsense and ERR pins to check what failure is currently existing. Then it was confirmed that the pin voltage was in line with the description of the latch-off protection in the failure table. Therefore, it must be that one of the two protections is triggered: the short-to-battery protection or the reverse current protection.

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FAILURE MODE	$V_{(SENSE)}$	$\overline{ERR}$	LDO SWITCH OUTPUT	LATCHED
Open load	$\frac{I_O \times R_{(SENSE)}}{198}$	HIGH	Enabled	No
Normal		HIGH	Enabled	No
Overcurrent		HIGH	Enabled	No
Short-circuit or current limit	2.4 to 2.65 V	LOW	Enabled	No
Thermal shutdown	2.7 to 3 V	LOW	Disabled	No
Output short-to-battery	3.05 to 3.3 V	LOW	Disabled	Yes
Reverse current	3.05 to 3.3 V	LOW	Disabled	Yes

Figure 3-3. Failure Table From Datasheet

Section 7.3.3 of the datasheet describes these two failures, but the detection mechanism is not clearly explained. A little bit more explanation is added here:

1. The short-to-battery protection is only detected during startup. Even if this failure occurs again during subsequent steady-state operation, the device does not report or detect the error.
2. The short-to-battery failure may cause reverse current during normal operation, which triggers reverse current protection. The reverse current protection begins detection 16ms after a relevant event occurs. If the reverse current exceeds the threshold for 5µs, the protection is triggered. The figure below illustrates this more clearly.
3. As mentioned in #b, there is a 16ms delay (t(blk_rc)) after a relevant event occurs. Relevant events include power-up, the rising edge of EN, and recovery from overcurrent protection. This is primarily because in these scenarios, the resonance caused by parasitic parameters or the sudden release of overcurrent limiting may cause the output voltage to instantaneously exceed the input voltage. In this case, it is undesirable to trigger reverse overcurrent protection, which would otherwise cause the device to latch off.

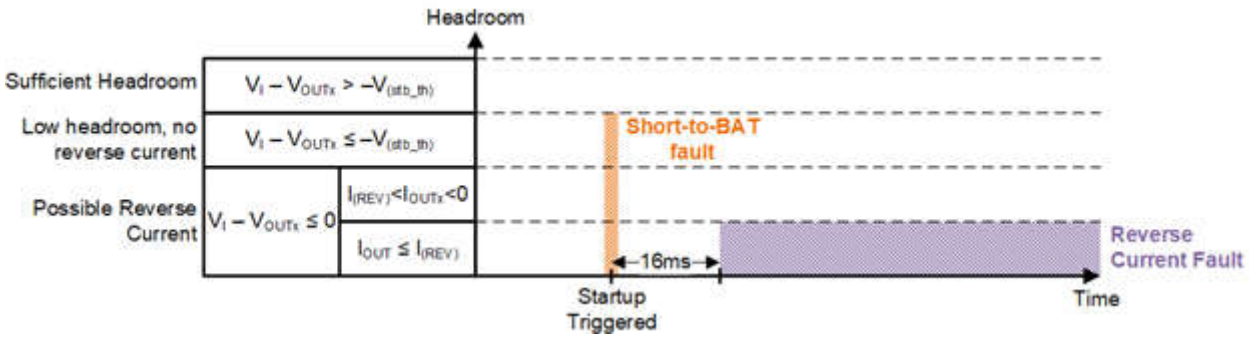

Figure 3-4. Overcurrent Protection Detection and Filtering Time

In customer's application scenarios, when the input voltage is lower than the output voltage, the device operates in an open-loop state, acting as a switch. When the input voltage drops, the loaded channel pulls its input voltage to the same level as the output voltage because of its load consumption. On the no-load channel, however, the voltage across the output capacitor may be higher than the input voltage that has dropped because of the energy stored in the output capacitor. This causes a negative current, triggering latch off. Whether the negative current is generated, as well as its magnitude, depends on the input voltage slew rate and the load condition. When there are loads on both channels, the energy stored in the output capacitor is consumed, avoiding the condition where the output voltage is higher than the input voltage.

For a practical application, there may be one channel with no load and the other channel with a heavy load. In this case, the output capacitor discharges to the input capacitor according to the analysis above. It is then necessary to find a way to discharge the electrical energy stored in the capacitor on the no-load channel, thereby avoiding this issue.

1. Block the output capacitor from discharging to the input capacitor. Connect a diode in series between the output capacitor and the output pin to block the discharge path. For this device, the datasheet recommends an output ESR of less than 5 ohms to meet stability requirements. Adding a diode directly is equivalent

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to adding an impedance at the output in the small-signal model under no-load conditions. However, the small-signal impedance of the diode is too high, making it difficult to achieve stability. It is suggested to add a small capacitor between the output and the diode (so that the reverse current does not exceed the threshold when the capacitor discharges) to achieve stability, but this must be verified through practical testing.

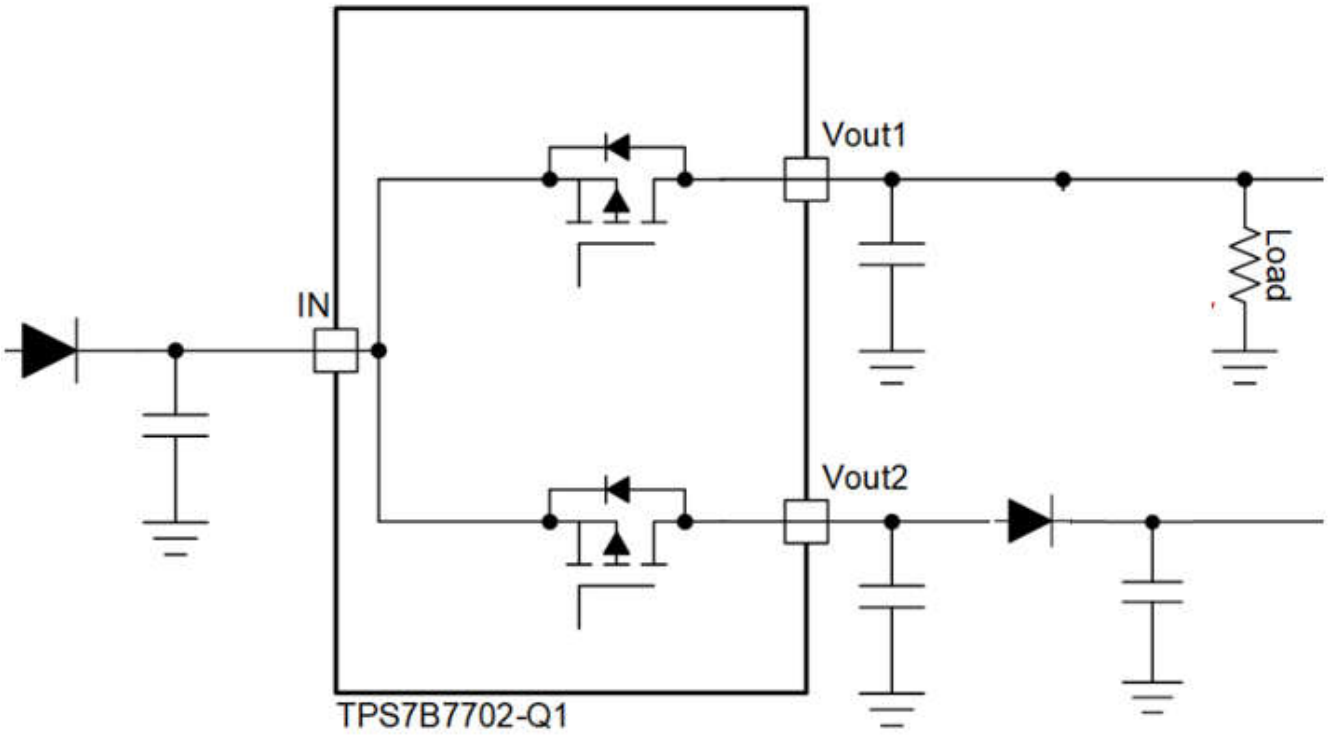

Figure 3-5. Connecting a Diode at the Output to Suppress Reverse Current

2. It is possible to connect a low-dropout diode in parallel between the two outputs because the output voltage is consistent in this application. Its voltage drop must be lower than the sum of the voltage drop along the path to Vin plus the dropout voltage of Vout1. This ensures that Vout2 discharges through the load of Vout1 when Vin drops, which is equivalent to providing a load on Vout2 to facilitate discharge. During normal operation, the diode is off and therefore does not affect the output voltage stability.

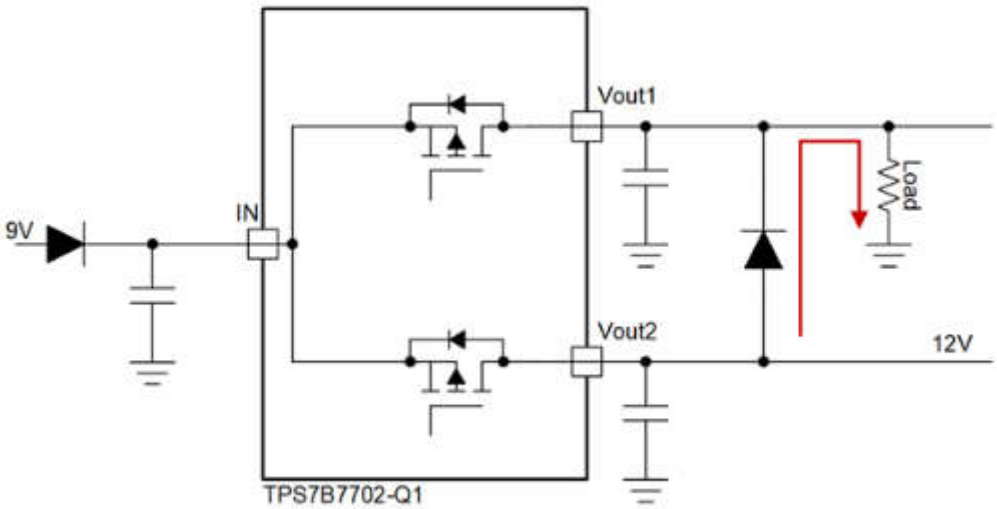

Figure 3-6. Connecting a Diode at the Output to Add a Discharge Path

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4 Conclusion

This article gives some design considerations for the application of the TPS7B7702-Q1 and explains the waveforms of Vsense oscillation encountered during practical testing. It also provides a detailed explanation of the chip's latch-off protection mechanism based on real-world applications and offers analysis and feasible solutions for issues that arise in practice, providing certain guidance for the application of this chip.

5 References

1. Datasheet "TPS7B770x-Q1, Automotive, Single- and Dual-Channel Antenna LDO With Current Sense datasheet (Rev. C)"

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