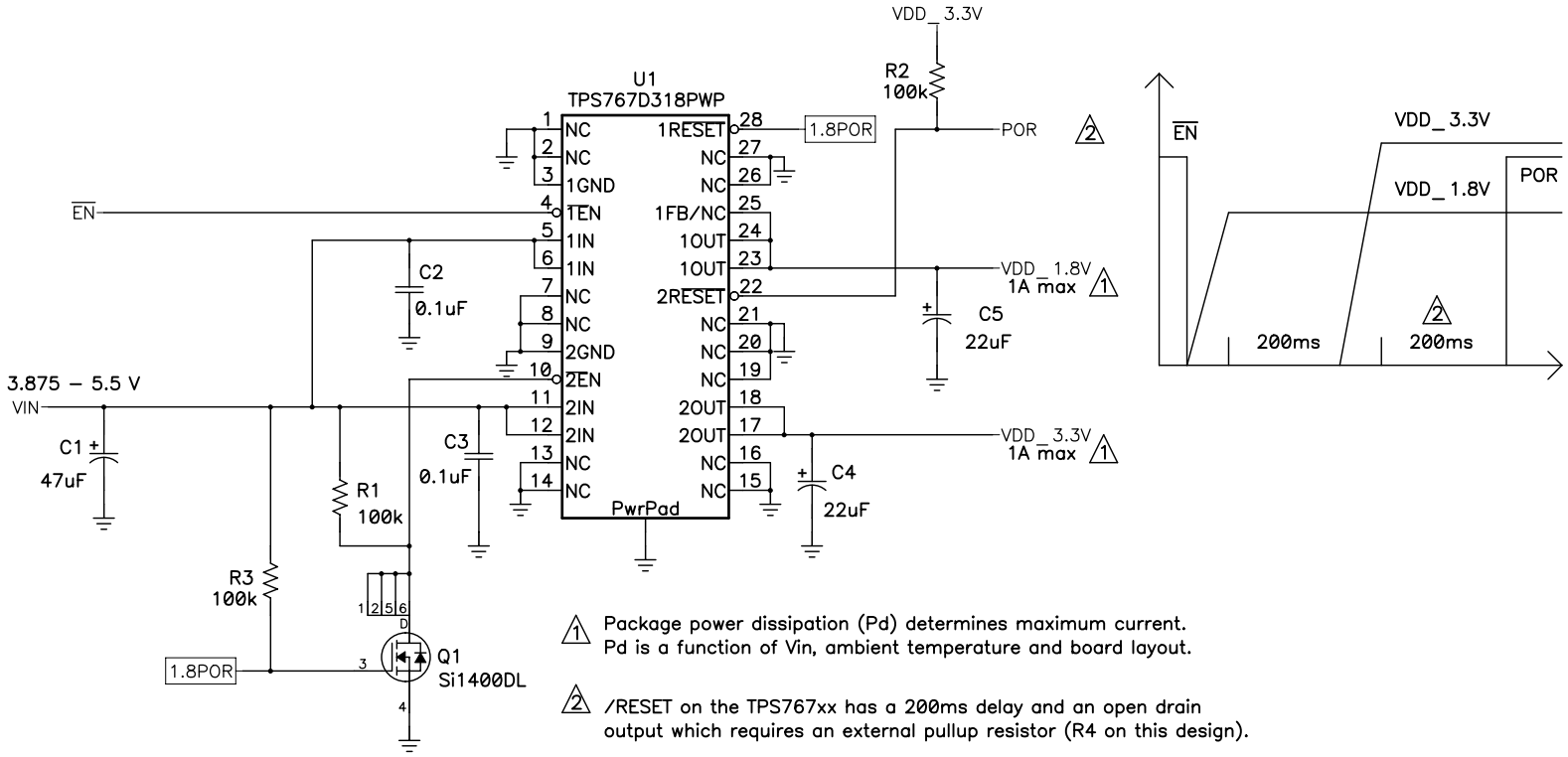

1. Package power dissipation (Pd) determines maximum current. Pd is a function of Vin, ambient temperature and board layout.

2. /RESET on the TPS767xx has a 200ms delay and an open drain output which requires an external pullup resistor (R4 on this design).

3. Additional input may be required depending on the regulator's proximity to the system power supply. Additional output capacitance will be required to meet load transient requirements.

Title	28xx DSP Power Single Chip, High Power Solution	
Size B	Number PR675	Rev E–1
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PR675E-1 BOM

COUNT	RefDes	Value	Description	Size	Part Number	MFR	AREA
1	C1	47uF	Capacitor, Tantalum, 6.3V, 1.4milliohm, 20%	B Case	293D476X6R3B2	Vishay	
2	C2, C3	0.1uF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	STD	STD	
2	C4, C5	22uF	Capacitor, Tantalum, 6.3V, 570milliohm, 20%	B Case	595D226X96R3B2	Vishay	
1	Q1	Si1400DL	MOSFET, N-ch, 20V, 1.3A, 235milliOhms	SC-70	Si1400DL	Vishay	
3	R1, R2, R3	100k	Resistor, Chip, 1/16W, 5%	0402	Std	Std	
1	U1	TPS767D318PWP	IC, Dual 1A Low-Dropout Regulator	PWP28	TPS767D318PWP	TI	

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants.
   Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted.
   All other components can be substituted with equivalent MFG's components.

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