TPS54325 4.5-V to 18-V, 3-A Output Synchronous Step Down Switcher with Integrated FET

1 Features

- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide V_{CC} Input Voltage Range: 4.5 V to 18 V
- Wide V_{IN} Input Voltage Range: 2.0 V to 18 V
- Output Voltage Range: 0.76 V to 5.5 V
- Highly Efficient Integrated FET's Optimized for Lower Duty Cycle Applications – 120 mΩ (High Side) and 70 mΩ (Low Side)
- High Efficiency, less than 10 μA at shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 700-kHz Switching Frequency (f_{SW})
- Cycle By Cycle Over Current Limit
- Power Good Output

2 Applications

- Wide Range of Applications for Low Voltage System
  - Digital TV Power Supply
  - High Definition Blu-ray Disc™ Players
  - Networking Home Terminal
  - Digital Set Top Box (STB)

3 Description

The TPS54325 device is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54325 device enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low component count, low standby current solution.

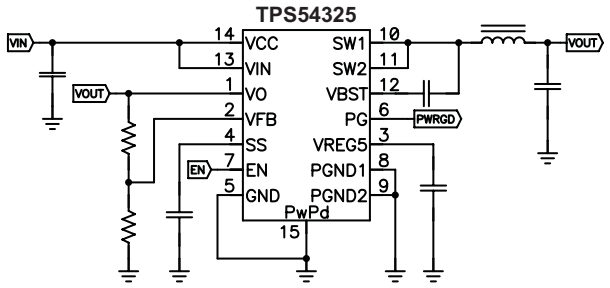
The main control loop for the TPS54325 uses the D-CAP2™ mode control which provides a very fast transient response with no external components. The TPS54325 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VCC input , and from 2.0-V to 18-V VIN input power supply voltage. The output voltage can be programmed between 0.76 V and 5.5 V. The device also features an adjustable slow start time and a power good function. The TPS54325 is available in the 14 pin HTSSOP package, and designed to operate from –40°C to 85°C.

Device Information(1)

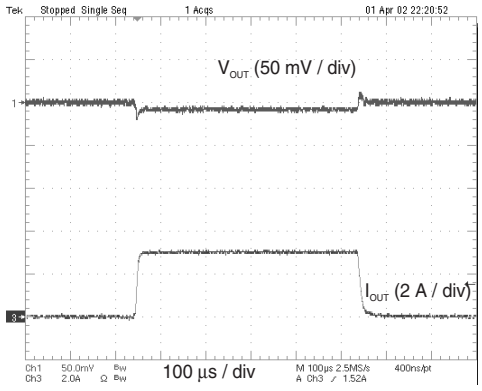
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54325	HTSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Load Transient Response



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2014) to Revision F — **Page**

- Added, updated, or renamed the following sections: Device Information Table, *Application and Implementation*; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* ... 1

Changes from Revision D (January 2012) to Revision E — **Page**

- Changed text in the *Bootstrap Capacitor Selection* from "between the VREG5 to GND pin for proper operation" to "between the VBST to SW pin for proper operation ... 13

Changes from Revision C (July 2011) to Revision D — **Page**

- Removed (SWIFT™) from the data sheet title ... 1
- Added conditions to *Typical Characteristics* ... 7

Changes from Revision B (March 2011) to Revision C — **Page**

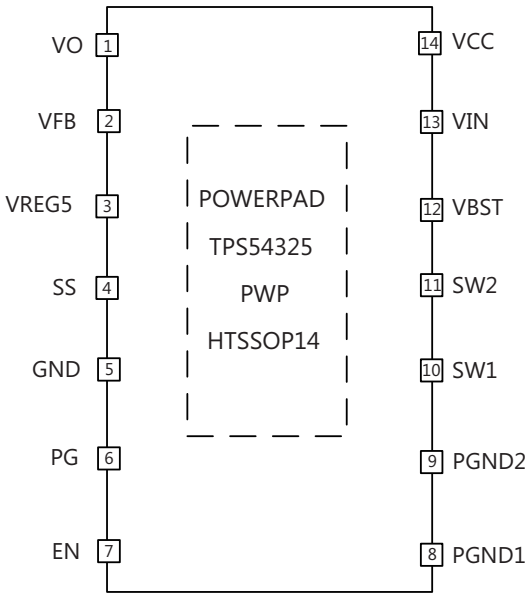
- Changed EN high-level input voltage from min of 2.0 V to min of 1.6 V ... 5
- Changed EN low-level input voltage from max of 0.48 V to max of 0.4 V ... 5

Changes from Original (May 2009) to Revision A — **Page**

- Changed T_A, for the current limit, I_{ocl}, From: 25°C to –40°C To: 85°C and 3.5 A was added at the MIN value ... 6

6 Pin Configuration and Functions

14-Pin
PWP PACKAGE
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VO	1	I	Connect to output of converter. This terminal is used for On-Time Adjustment.
VFB	2	I	Converter feedback input. Connect with feedback resistor divider.
VREG5	3	O	5.5 V power supply output. A capacitor (typical 1µF) should be connected to GND.
SS	4	I	Soft-start control. A external capacitor should be connected to GND.
GND	5	—	Signal ground pin
PG	6	O	Open drain power good output
EN	7	I	Enable control input
PGND1, PGND2	8, 9	—	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2	10, 11	O	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparators.
VBST	12	O	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin.
VIN	13	I	Power input and connected to high side NFET drain
VCC	14	I	Supply input for 5 V internal linear regulator for the control circuitry
PowerPAD™	—	—	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage range	V_{IN}, V_{CC}, EN	–0.3	20	V
		V_{BST}	–0.3	26	V
		V_{BST} (vs SW1, SW2)	–0.3	6.5	V
		V_{FB}, V_O, SS, PG	–0.3	6.5	V
		SW1, SW2	–2	20	V
		SW1, SW2 (10 ns transient)	–3	20	V
V_O	Output voltage range	V_{REG5}	–0.3	6.5	V
		P_{GND1}, P_{GND2}	–0.3	0.3	V
V_{diff}	Voltage from GND to POWERPAD		–0.2	0.2	V
T_J	Operating junction temperature		–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		500	

(1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC(1)		PWP	UNIT
		12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	26.4	
ψ_{JT}	Junction-to-top characterization parameter	1.8	
ψ_{JB}	Junction-to-board characterization parameter	20.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply input voltage range		4.5	18	V
V_{IN}	Power input voltage range		2	18	V
V_I	Input voltage range	V_{BST}	–0.1	24	V
		V_{BST} (vs SW1, SW2)	–0.1	6	
		SS, PG	–0.1	6	
		EN	–0.1	18	
		V_O, V_{FB}	–0.1	5.5	
		SW1, SW2	–1.8	18	
		SW1, SW2 (10 ns transient)	–3	18	
		P_{GND1}, P_{GND2}	–0.1	0.1	
V_O	Output voltage range	V_{REG5}	–0.1	6	V
I_O	Output current range	I_{VREG5}	0	10	mA
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	125	°C

7.5 Electrical Characteristics

over operating free-air temperature range, V_{CC}, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VCC}	Operating - non-switching supply current	V_{CC} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.8 V		850	1300	µA
I_{VCCSDN}	Shutdown supply current	V_{CC} current, T_A = 25°C, EN = 0 V			10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	1.6			V
V_{ENL}	EN low-level input voltage	EN			0.4	V
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V	757	765	773	mV
		T_A = 0°C to 85°C, V_O = 1.05 V(1)	753		777	
		T_A = -40°C to 85°C, V_O = 1.05 V(1)	751		779	
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V, T_A = 25°C		0	±0.1	µA
R_{Dischg}	V_O discharge resistance	EN = 0 V, V_O = 0.5 V, T_A = 25°C		50	100	Ω
V_{REG5} OUTPUT						
V_{VREG5}	V_{REG5} output voltage	T_A = 25°C, 6.0 V < V_{CC} < 18 V, 0 < I_{VREG5} < 5 mA	5.3	5.5	5.7	V
V_{LN5}	Line regulation	6.0 V < V_{CC} < 18 V, I_{VREG5} = 5 mA			20	mV
V_{LD5}	Load regulation	0 mA < I_{VREG5} < 5 mA			100	mV
I_{VREG5}	Output current	V_{CC} = 6 V, V_{REG5} = 4.0 V, T_A = 25°C		70		mA
MOSFET						
R_{dsonh}	High side switch resistance	25°C, V_{BST} - SW1, SW2 = 5.5 V		120		mΩ
R_{dsonl}	Low side switch resistance	25°C		70		mΩ

(1) Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, V_{CC}, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{ocl}	Current limit	T_A = –40°C to 85°C (1)	3.5	4.1	5.5	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (1)		150		°C
		Hysteresis (1)		25		
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		145		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.7 V		260		ns
SOFT START						
I_{SSC}	SS charge current	V_{SS} = 0 V	1.4	2.0	2.6	µA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	0.1	0.2		mA
POWER GOOD						
V_{THPG}	PG threshold	V_{FB} rising (good)	85%	90%	95%	
		V_{FB} falling (fault)		85%		
I_{PG}	PG sink current	PG = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	115%	120%	125%	
T_{OVPDEL}	Output OVP prop delay			5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis		10%		
T_{UVPDEL}	Output UVP delay			0.25		ms
T_{UVPEN}	Output UVP enable delay	Relative to soft-start time		x 1.7		
UVLO						
V_{UVLO}	UVLO threshold	Wake up V_{REG5} voltage	3.45	3.70	3.95	V
		Hysteresis V_{REG5} voltage	0.15	0.25	0.35	

7.6 Typical Characteristics

VIN = 12 V, T_A = 25°C (unless otherwise noted)

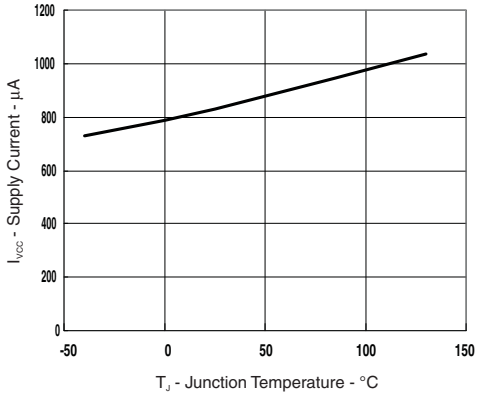


Figure 1. V_{CC} Temperature vs Junction Temperature

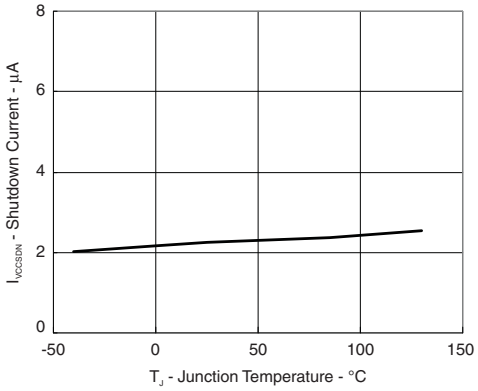


Figure 2. V_{CC} Shutdown Current vs Junction Temperature

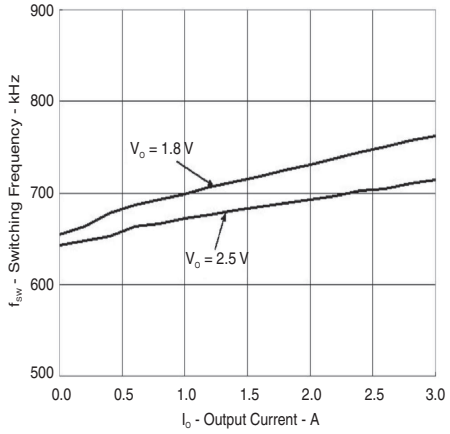


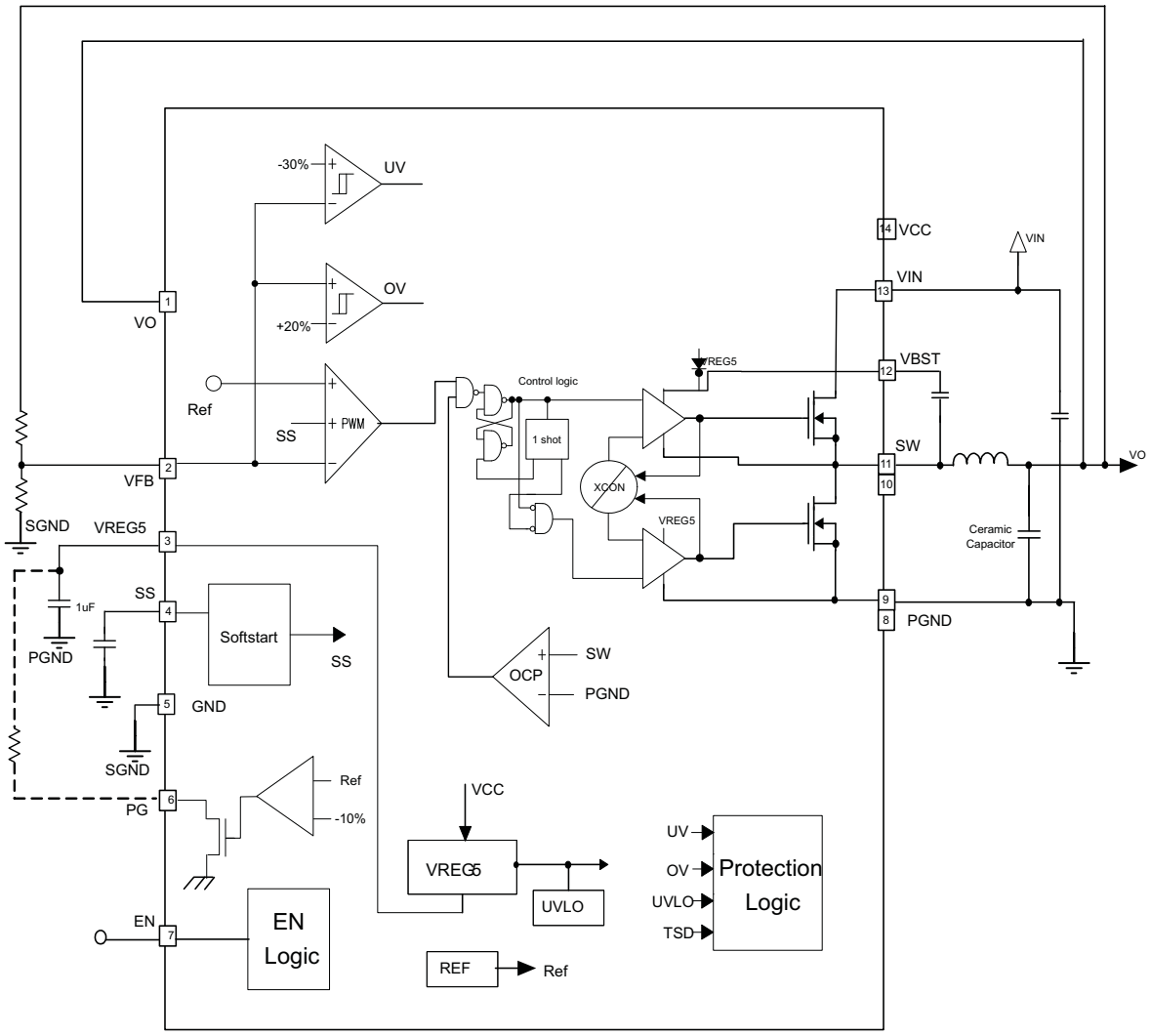
Figure 3. Switching Frequency vs Output Current

8 Detailed Description

8.1 Overview

The TPS54325 is a 3-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Soft Start and Pre-Biased Soft Start

The TPS54325 has an adjustable soft start . When the EN pin becomes high, 2.0-µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 1. VFB voltage is 0.765 V and SS pin source current is 2 µA.

$$Tss(ms) = \frac{C6(nF) \bullet Vref}{Iss(\mu A)} = \frac{C6(nF) \bullet 0.765}{2} \quad (1)$$

The TPS54325 contains a unique circuit to prevent current from being pulled from the output during startup in the condition the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage (V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

8.3.2 Power Good

The TPS54325 has power-good output. The power-good function is activated after soft start has finished. If the output voltage becomes within -10% of the target value, internal comparators detect power good state and the power good signal becomes high. R_{PG} resister value ,which is connected between PG and VREG5, is required from 20 kΩ to 150 kΩ. If the feedback voltage goes under 15% of the target value, the power good signal becomes low after 10 µs internal delay.

8.3.3 Output Discharge Control

The TPS54325 discharges the output when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO and thermal shutdown). The device discharges outputs using an internal 50-Ω MOSFET which is connected to VO and PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

8.3.4 Current Protection

The output over-current protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. If the measured voltage is above the voltage proportional to the current limit, Then , the device constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time.

The converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output under-voltage protection circuit to be activated. When the over current condition is removed, the output voltage will return to the regulated value. This protection is non-latching.

Feature Description (continued)

8.3.5 Overvoltage and Undervoltage Protection

The TPS54325 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET turns on.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 µs, the device latches off both internal top and bottom MOSFET. This function is enabled approximately 1.7 x soft-start time.

8.3.6 UVLO Protection

The TPS54325 has under voltage lock out protection (UVLO) that monitors the voltage of V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS54325 is shut off. This is non-latch protection.

8.3.7 Thermal Shutdown

The TPS54325 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 150°C), the device is shut off. This is non-latch protection.

8.4 Device Functional Modes

8.4.1 PWM Operation

The main control loop of the TPS54325 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot timer is set by the converter input voltage ,VIN, and the output voltage ,VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

8.4.2 PWM Frequency and Adaptive On-Time Control

TPS54325 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54325 runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

8.4.3 Operation with VIN < 4.5 V

The device is recommended to operate with input voltages above 4.5 V. The typical VIN UVLO threshold is 3.7 V and the device can operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device does not switch. If the EN pin is externally pulled up or left floating, the device becomes active when the VIN pin passes the UVLO threshold. Switching begins when the slow-start sequence is initiated.

8.4.4 Operation With EN Control

The enable threshold voltage is 1.6 V (typical). With the EN pin is held below that voltage, the device is disabled and switching is inhibited even if the VIN pin is above the UVLO threshold. The IC quiescent current is reduced in this state. If the EN voltage increases above the threshold while the VIN pin is above the UVLO threshold, the device becomes active. Switching is then enabled and the slow-start sequence is initiated.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS54325 device is typically used as a step-down converter, which converts a voltage in the range of 4.5 V to 18 V to a lower voltage. WEBENCH software is available to aid in the design and analysis of circuits.

9.2 Typical Application

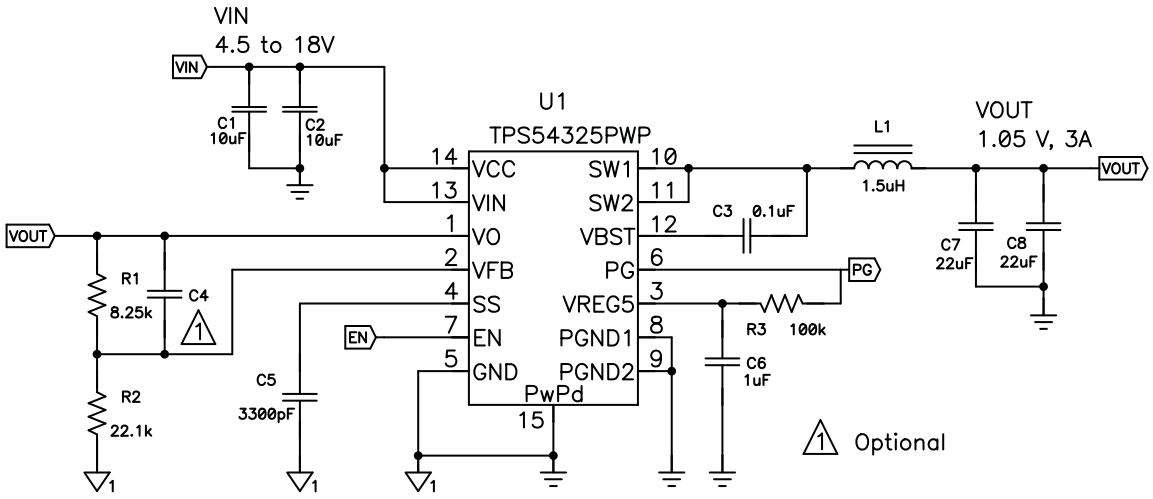


Figure 4. Schematic Diagram for Design Example

9.2.1 Design Requirements

To begin the design process, know the application parameters listed in Table 1:

Table 1. Application Parameters

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		5		17	V
Output voltage			1.05		V
Operating frequency	V_I = 12 V, I_o = 1 A		700		kHz
Output current		0		3	A
Output ripple voltage	V_I = 12 V, I_{out} = 3 A		9		mVpp
Efficiency	V_I = 12 V, V_{out} = 3.3 V, I_{out} = 1.2 A		91%		

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 2 and Equation 3 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

For output voltage from 0.76 V to 2.5 V:

$$V_{OUT} = 0.765 \bullet \left(1 + \frac{R1}{R2}\right) \tag{2}$$

For output voltage over 2.5 V:

$$V_{OUT} = (0.763 + 0.0017 \bullet V_{OUT}) \bullet \left(1 + \frac{R1}{R2}\right) \tag{3}$$

where

- V_{OUT_SET} = Target V_{OUT} voltage

9.2.2.2 Output Filter Selection

The output filter used with the TPS54325 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}} \tag{4}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54325. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to -20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 4 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)(1)	L1 (µH)	C8 + C9 (µF)
1	6.81	22.1		1.5	22 - 68
1.05	8.25	22.1		1.5	22 - 68
1.2	12.7	22.1		1.5	22 - 68
1.8	30.1	22.1	10 - 22	2.2	22 - 68
2.5	49.9	22.1	10 - 22	2.2	22 - 68
3.3	73.2	22.1	10 - 22	2.2	22 - 68
5	121	22.1	10 - 22	3.3	22 - 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 5, Equation 6 and Equation 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 700 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 6 and the RMS current of Equation 7.

$$Ilp\text{-}p = \frac{V_{OUT}}{V_{IN\,(max)}} \bullet \frac{V_{IN\,(max)} - V_{OUT}}{L_O \bullet f_{SW}} \quad (5)$$

$$I_{lpeak} = I_O + \frac{Ilp\text{-}p}{2} \quad (6)$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} Ilp\text{-}p^2} \quad (7)$$

For this design example, the calculated peak current is 3.47 A and the calculated RMS current is 3.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54325 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22 µF to 68 µF. Use Equation 8 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{\sqrt{12} \bullet V_{IN} \bullet L_O \bullet f_{SW}} \quad (8)$$

For this design two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.271 A and each output capacitor is rated for 4 A.

9.2.2.3 Input Capacitor Selection

The TPS54325 requires an input decoupling capacitor, and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10-mF is recommended for the decoupling capacitor. An additional 0.1-µF capacitor from pin 14 to ground is recommended to improve the stability of the over-current limit function. The capacitor voltage rating needs to be greater than the maximum input voltage.

9.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. Using a ceramic capacitor is recommended.

9.2.3 Application Curves

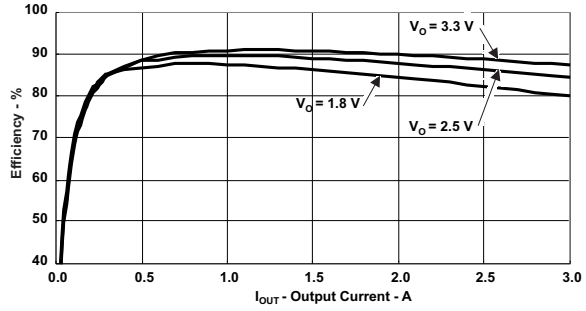


Figure 5. Efficiency vs Output Current
V_O = 3.3 V, 2.5 V, and 1.8 V

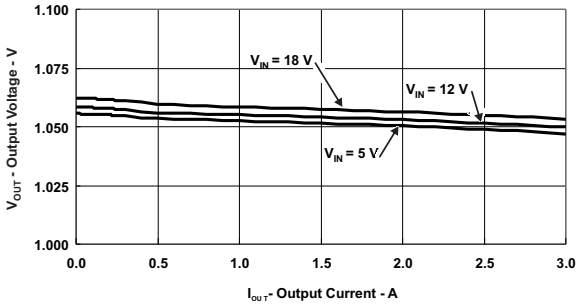


Figure 6. Load Regulation,
1.05-V Output Voltage vs Output Current

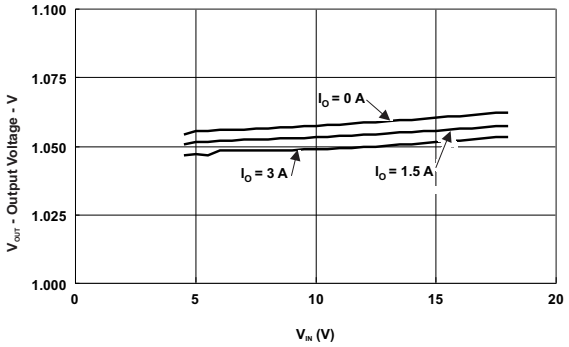


Figure 7. Line Regulation,
1.05-V Output Voltage vs Input Voltage

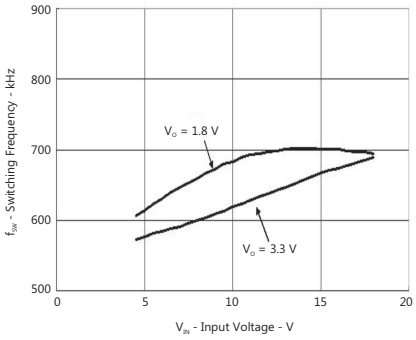


Figure 8. Switching Frequency vs Input Voltage

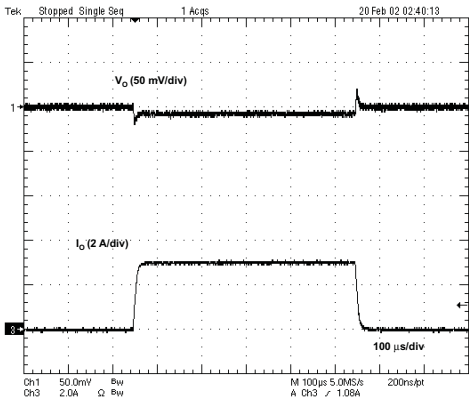


Figure 9. Load Transient Response

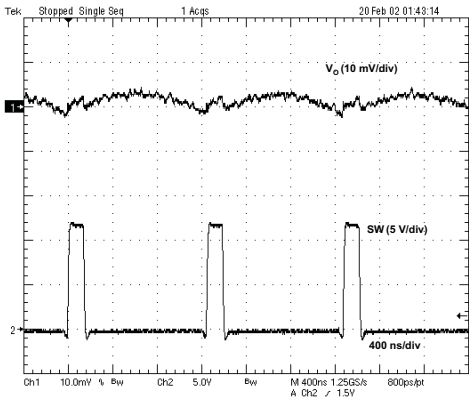


Figure 10. Output Voltage Ripple

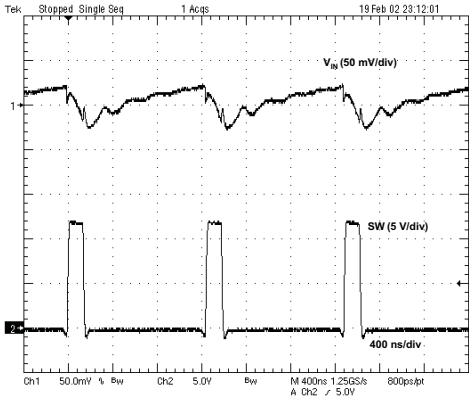


Figure 11. Input Voltage Ripple

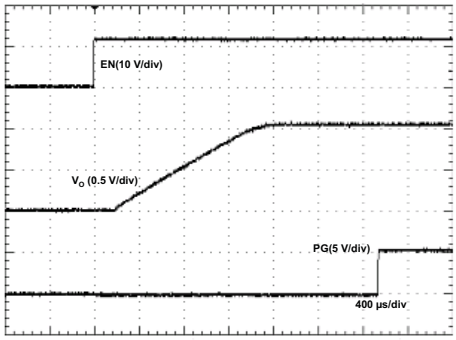


Figure 12. Start Up

10 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 4.5 V and 18 V. This input supply should be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. PCB pattern for VIN, SW, and PGND should be as broad as possible.
14. If VIN and VCC is shorted, VIN and VCC patterns need to be connected with broad pattern lines.
15. VIN Capacitor should be placed as near as possible to the device.

11.2 Layout Example

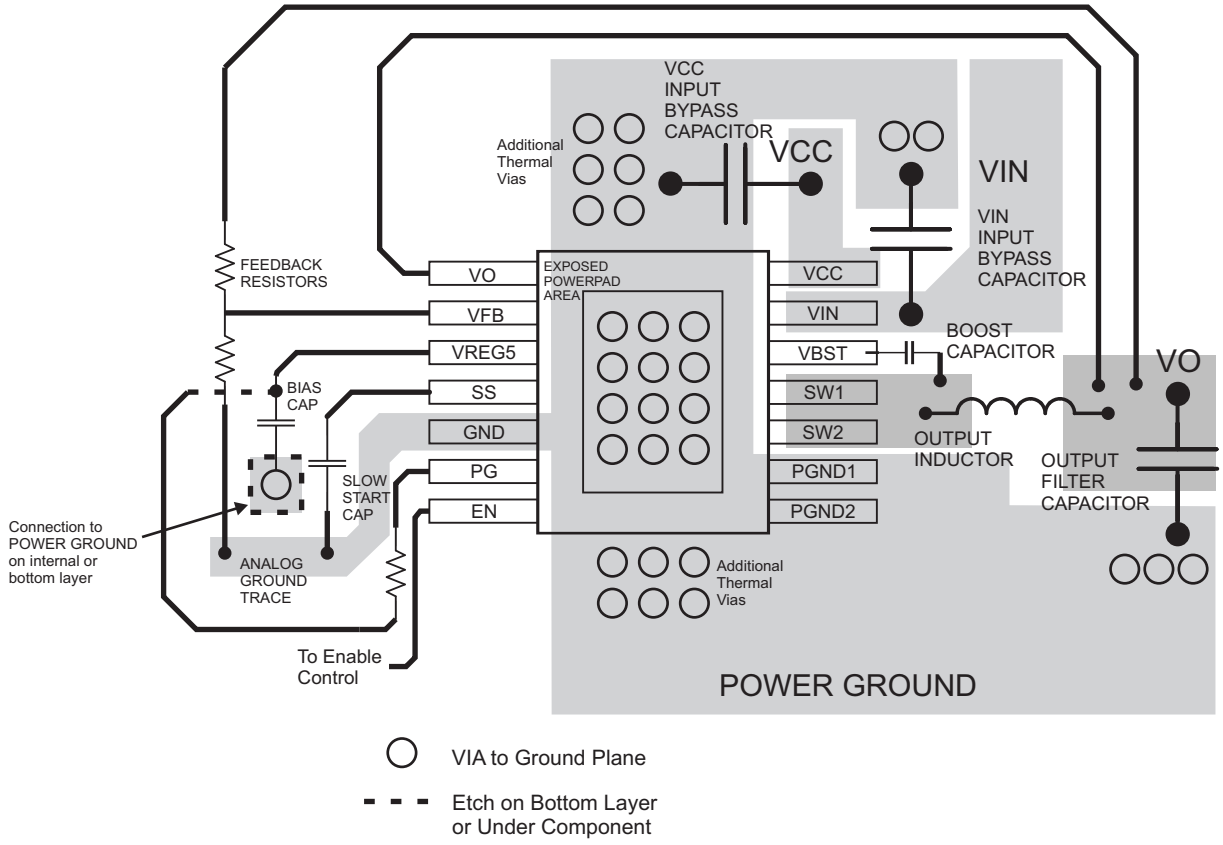


Figure 13. PCB Layout

11.3 Thermal Considerations

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be connected to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to:

- *PowerPAD™ Made Easy* (SLMA004).
- *PowerPAD™ Thermally Enhanced Package*, (SLMA002).

The exposed thermal pad dimensions for this package are shown in Figure 14

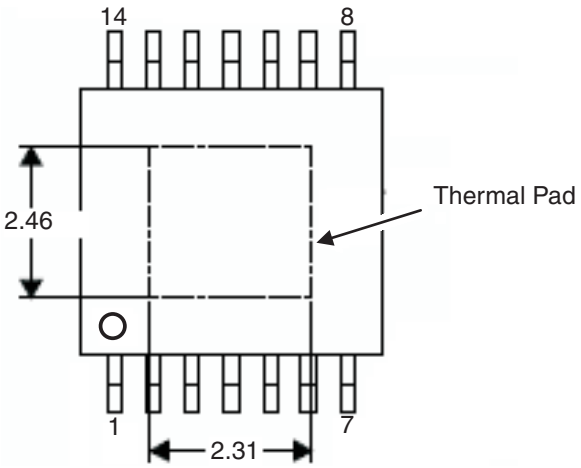


Figure 14. Thermal Pad Dimensions

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

- WEBENCH
- For SWIFT™ Power Products Documentation, see http://www.ti.com/swift

12.2 Documentation Support

12.2.1 Related Documentation

- *Absolute Maximum Ratings for Soldering* (SNOA549).
- *PowerPAD™ Made Easy* (SLMA004).
- *PowerPAD™ Thermally Enhanced Package* (SLMA002).
- *Semiconductor and IC Package Thermal Metrics* (SPRA953).

12.3 Trademarks

D-CAP2, PowerPAD are trademarks of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disc.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54325PWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54325	Samples
TPS54325PWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54325	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS54325 :

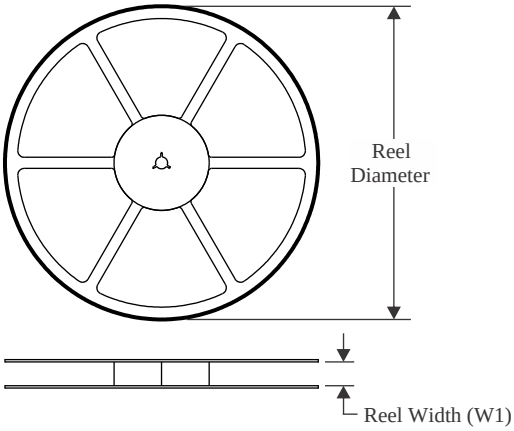
- Automotive: TPS54325-Q1

NOTE: Qualified Version Definitions:

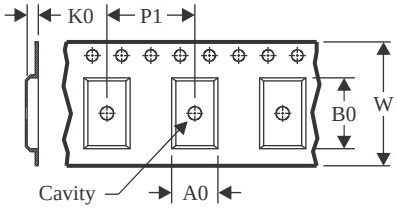
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

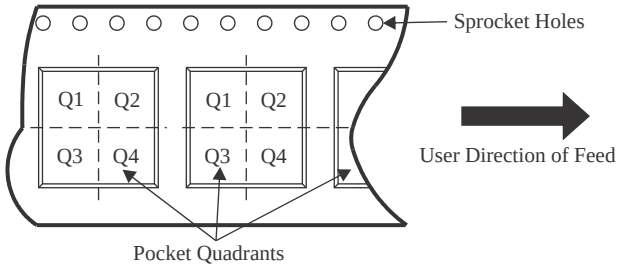


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

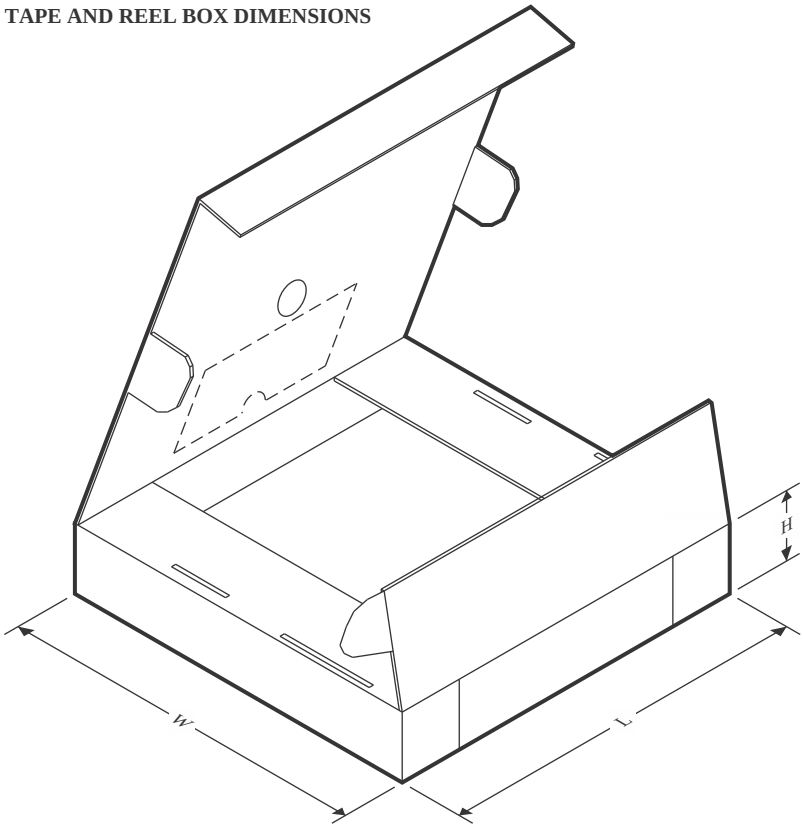
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54325PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

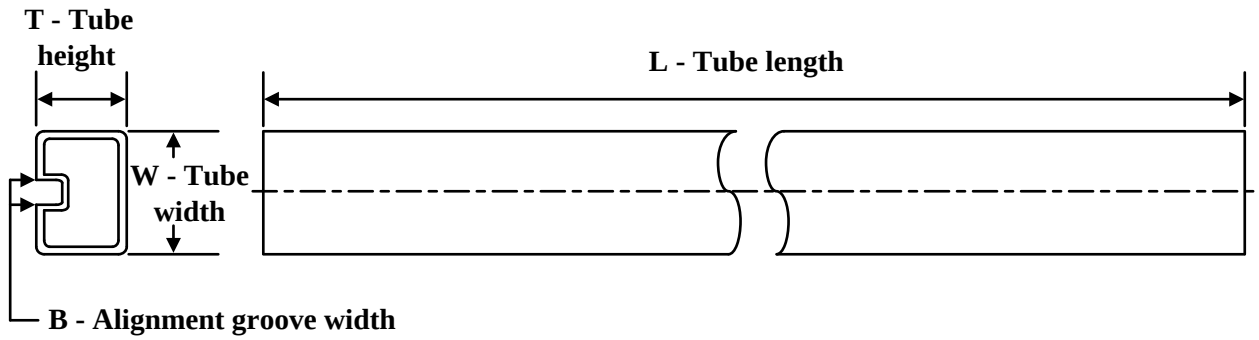
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54325PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54325PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS54325PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

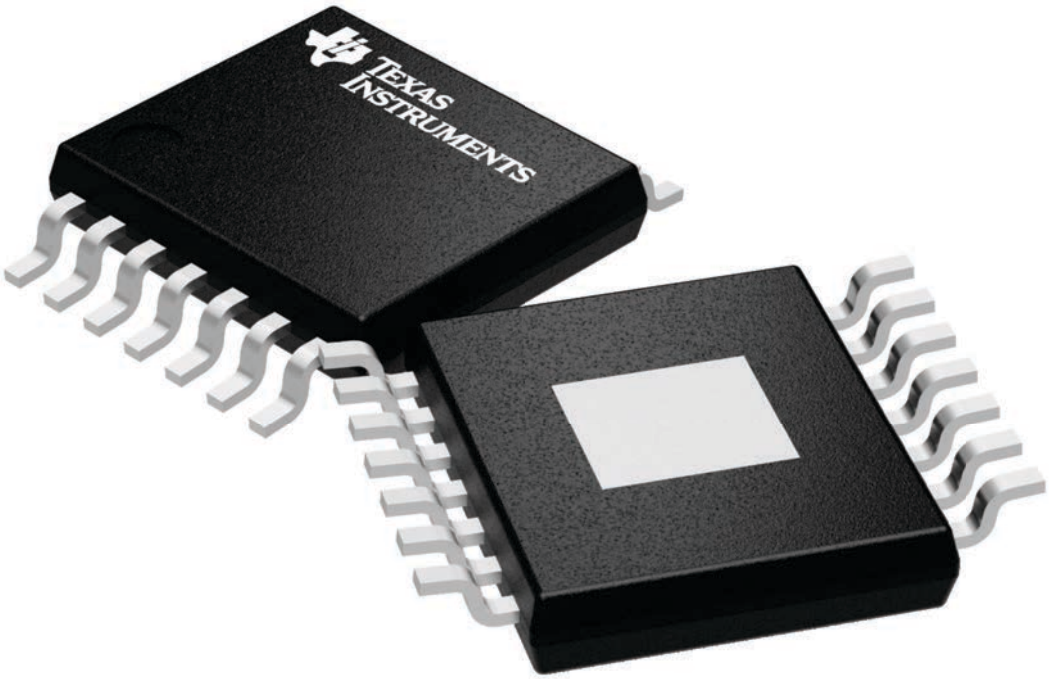
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

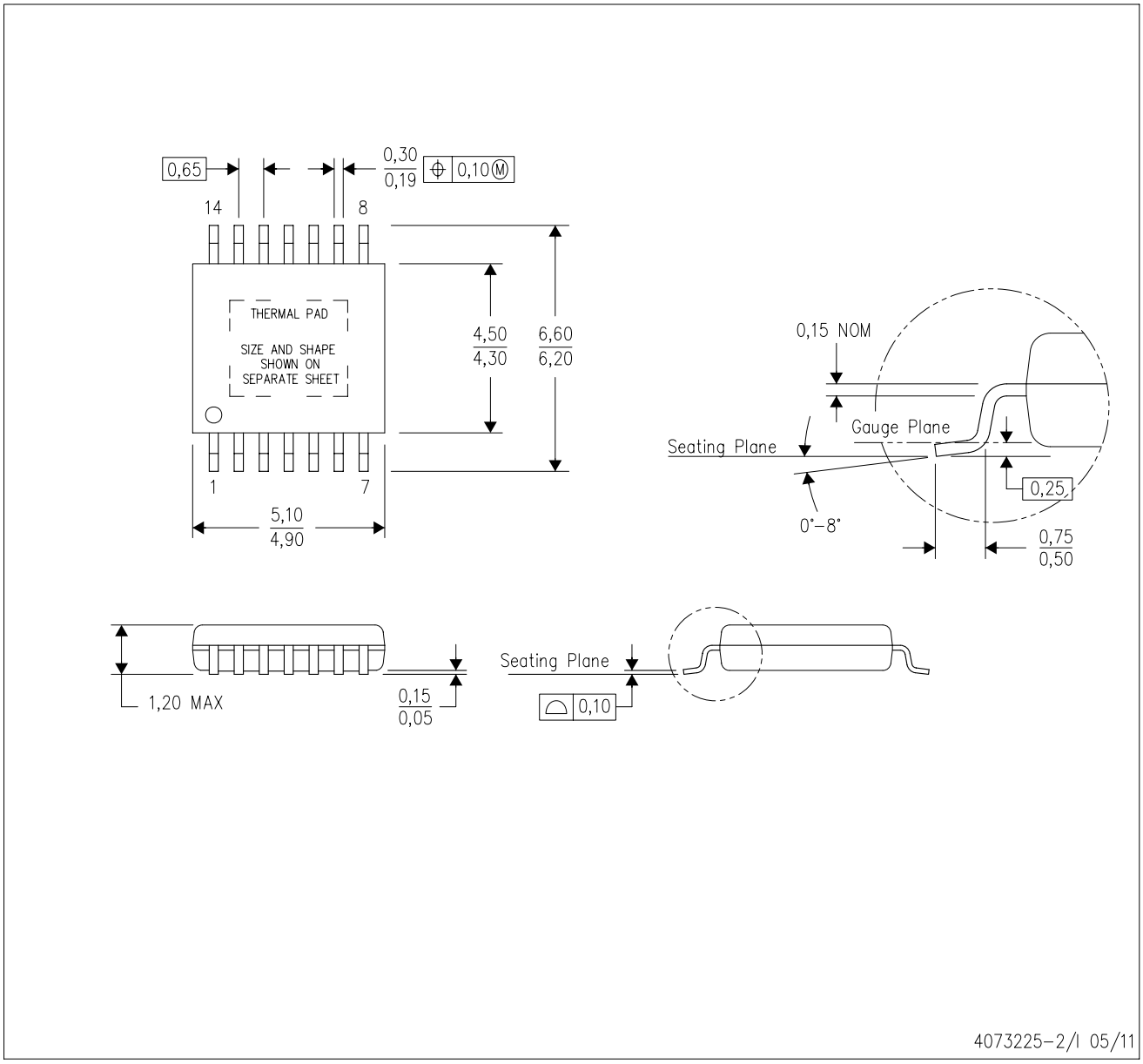
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224995/A

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

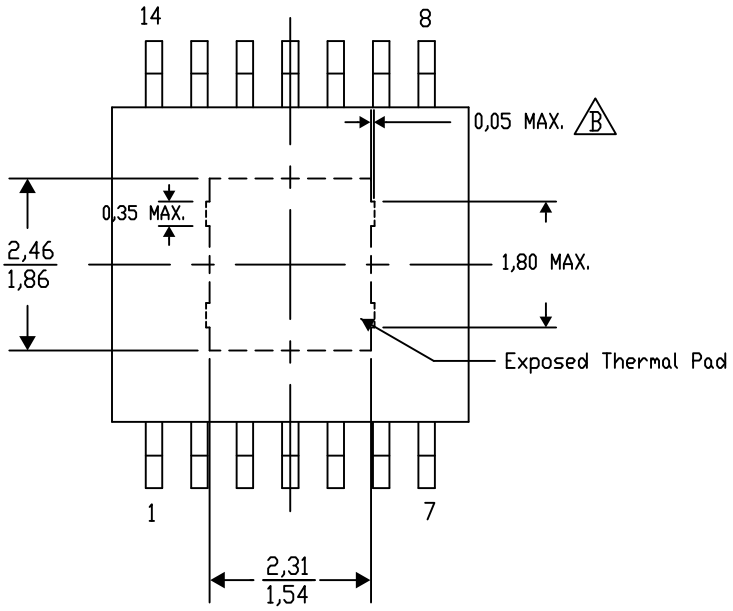
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

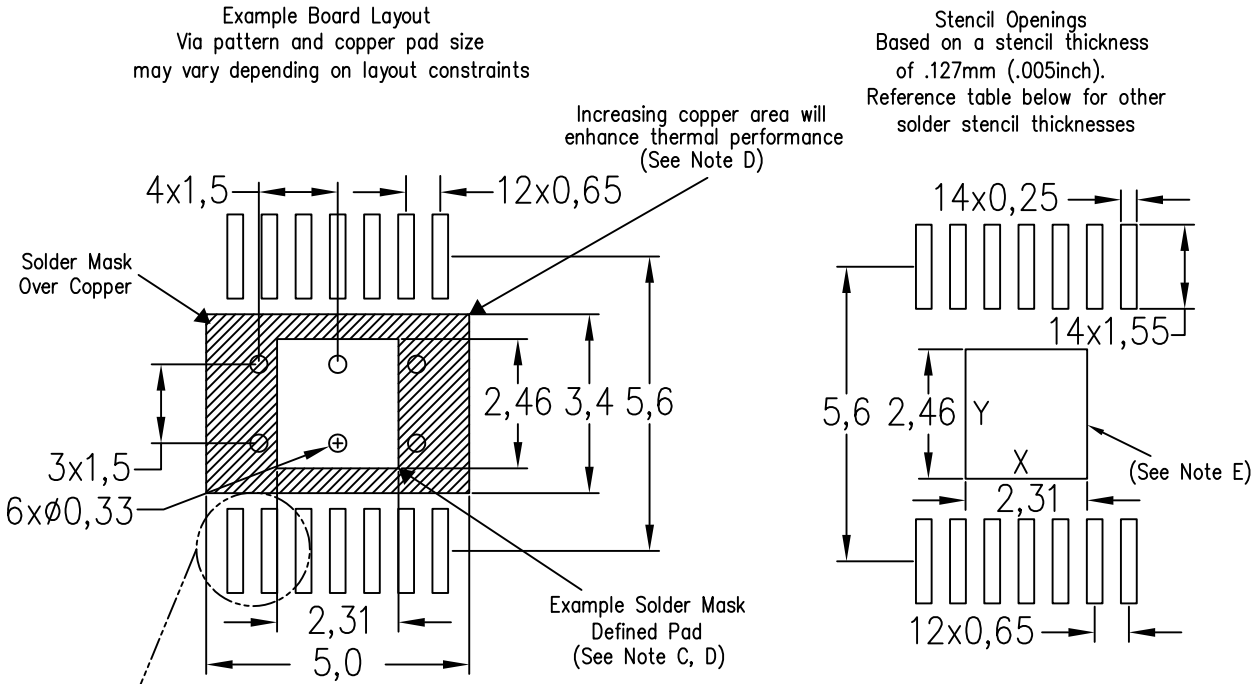
4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

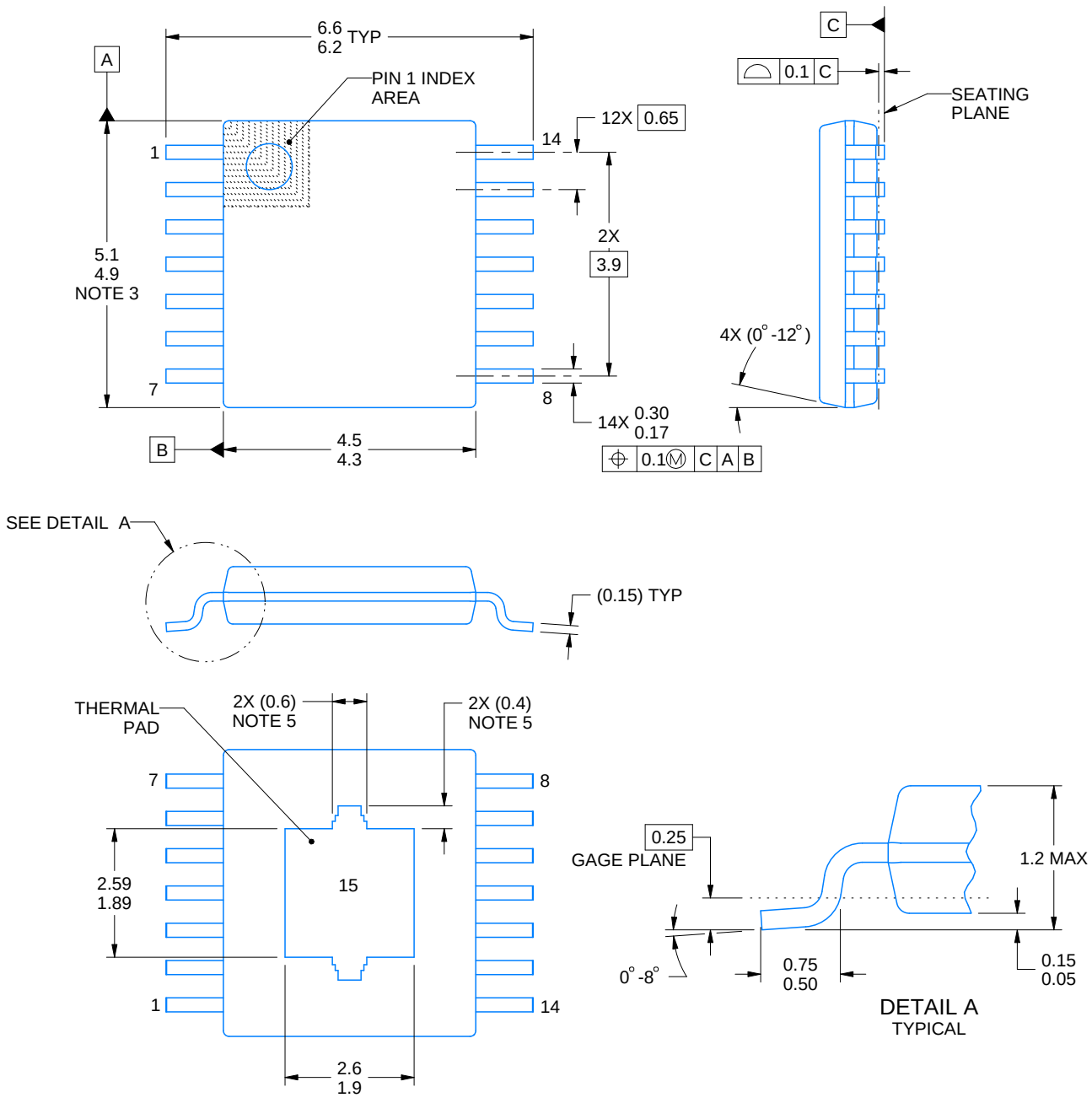
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

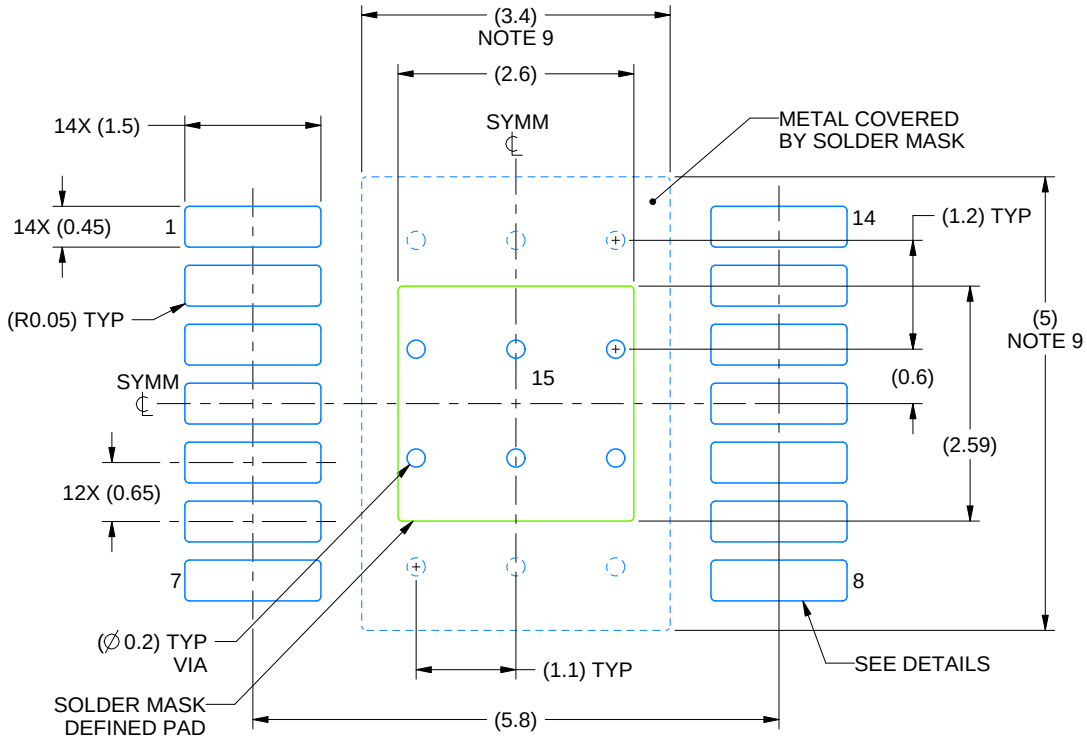
SMALL OUTLINE PACKAGE



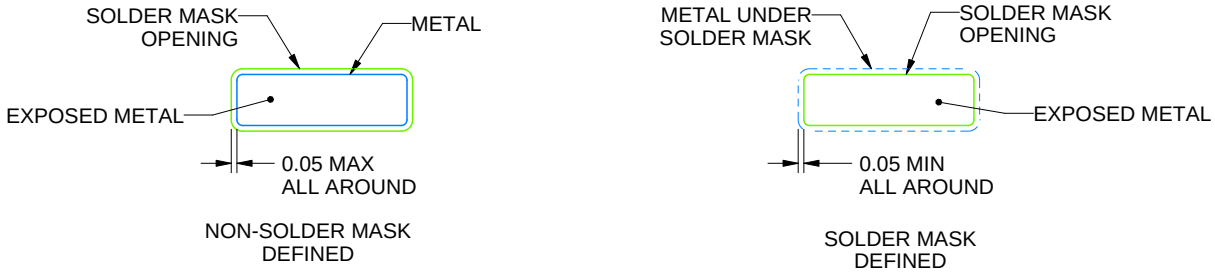
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

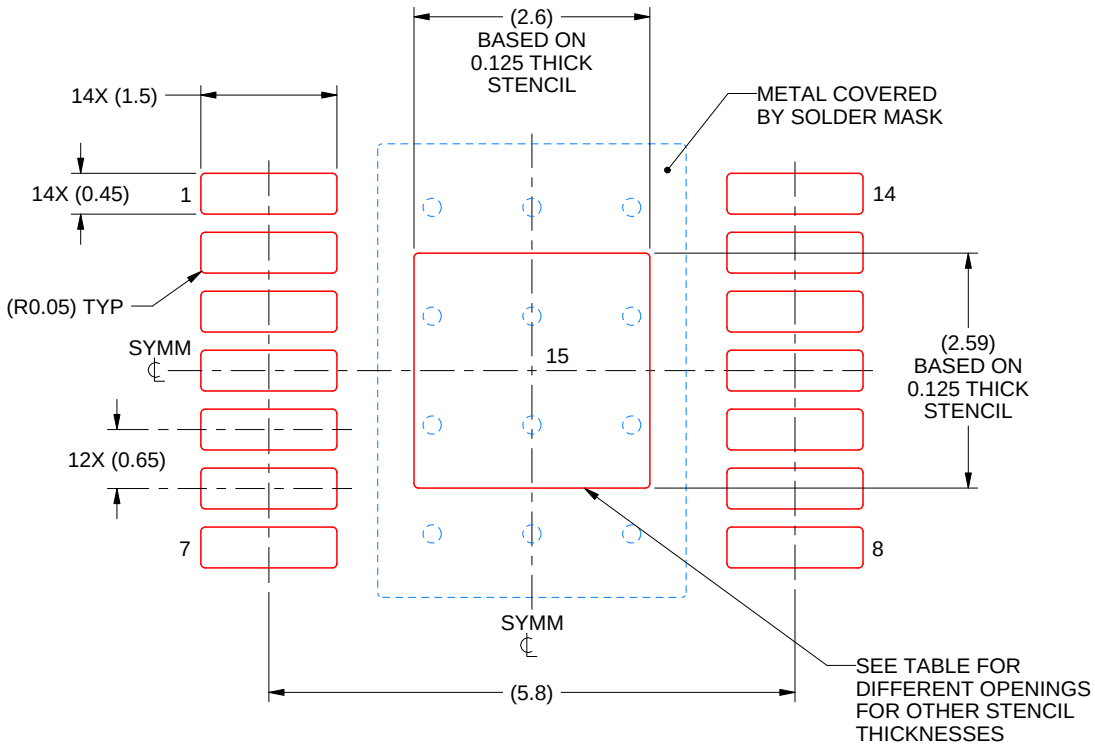


SOLDER MASK DETAILS

4229706/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

4229706/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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