TPS7A4501-SP Low-Dropout Voltage Regulator

1 Features

- QMLV Qualified SMD 5962-12224
- Adjustable Output from 1.21 to 20 V
- Optimized for Fast-Transient Response
- High Output Voltage Accuracy: 1.15% at 25°C (Typical)
- Dropout Voltage: 200 mV With I_{LOAD} = 750 mA (Typical)
- Low Noise: 50 μV_{RMS} (10 Hz to 100 kHz) for V_{OUT} = 5 V
- High Ripple Rejection: 68 dB at 1 kHz
- 1-mA Quiescent Current
- No Protection Diodes Needed
- Stable With Ceramic Output Capacitor
- Reverse-Battery Protection
- Reverse Current Protection
- 5962-1222402VHA:
  - Wide Vin 2.3 to 20 V
  - Output Current: 750 mA
- 5962R1222403VXC:
  - Wide Vin 2.9 to 20 V
  - Output Current: 1.5 A
  - Thermally-Enhanced HKU Package
  - Radiation Hardness Assurance (RHA) up to Total Ionizing Dose (TID) 100 krad (Si)
  - Exhibits Low Dose Rate Sensitivity But Remains Within the Pre-Radiation Electrical Limits at 100 krad Total Dose Level, as Allowed by MIL-STD-883, TM1019

2 Applications

- RF Components VCOs, Receivers, ADCs, Amplifiers and Clock Distributions
- Clean Analog Supply Requirements
- Available in Military (–55°C to 125°C) Temperature Range
- Engineering Evaluation (/EM) Samples are Available

(1) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (for example, no burn-in, and so forth) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not specified for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

3 Description

The TPS7A4501-SP is a low-dropout (LDO) regulator optimized for fast-transient response. The 5962-1222402VHA can supply 750 mA of output current with a dropout voltage of 300 mV. The 5962R1222403VXC can supply 1.5 A of output current with a dropout voltage of 320 mV. Quiescent current is well controlled; it does not rise in dropout, as with many other regulators. In addition to fast transient response, the TPS7A4501-SP regulator has very-low output noise, which makes it ideal for sensitive RF supply applications.

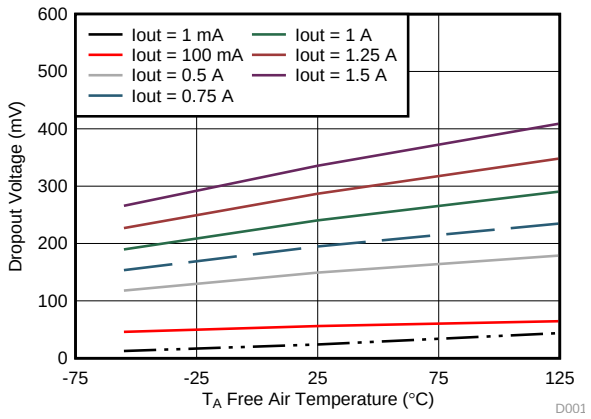
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A4501-SP	CFP [U] (10)	6.35 mm × 6.35 mm
	CFP [HKU] (10)	7.02 mm × 6.86 mm
	KGD	N/A(2)

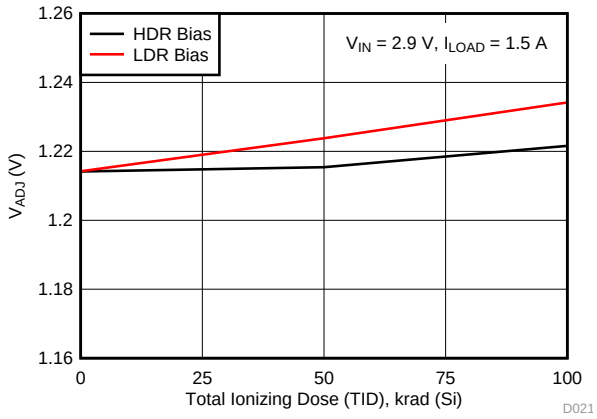
(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Bare die in waffle pack

Dropout Voltage vs Temperature



V_{ADJ} Radiation Drift Curve



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2014) to Revision D — **Page**

- Replaced the *Dissipation Ratings* table with the *Thermal Information* table ... 5
- Added 5962-1222402V9A to *Electrical Characteristics (5962-1222402VHA and 5962-1222402V9A)* ... 6
- Added new part 5962R1222403V9A to *Electrical Characteristics (5962R1222403VXC and 5962R1222403V9A)* ... 7

Changes from Revision B (October 2014) to Revision C — **Page**

- Removed V_{DO}, dropout voltage with test condition V_{OUT} = 2.4 V ... 6
- Added thermal shutdown temperature ... 6
- Added thermal shutdown temperature ... 8
- Added thermal shutdown information to *Protection Features* ... 15

Changes from Revision A (January 2014) to Revision B — **Page**

- Added limits for the new device type, 5962R1222 ... 1
- Added *Handling Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added thermal information for the HKU package ... 5

Changes from Original (December 2013) to Revision A — **Page**

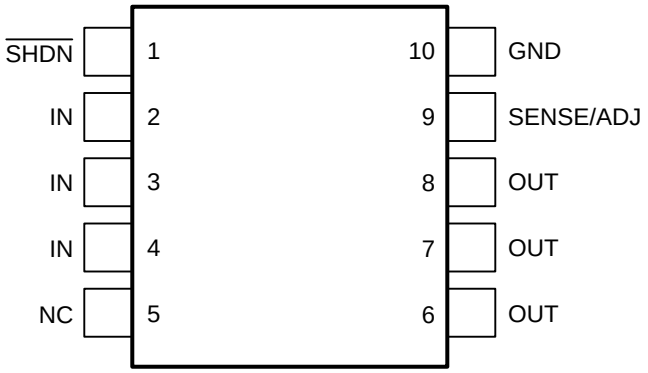
- Changed Product Status from Product Preview to Production Data ... 1

5 Description (continued)

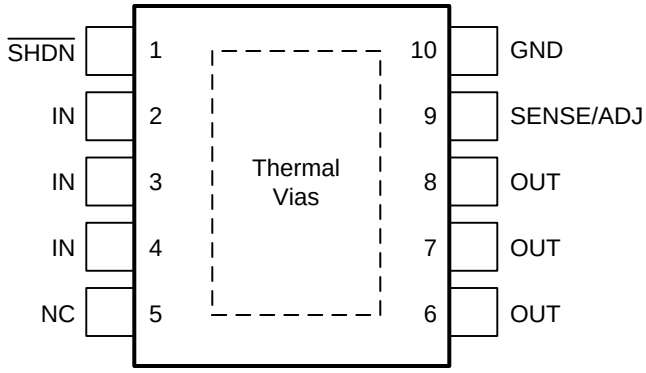
Output voltage range is from 1.21 to 20 V. The TPS7A4501-SP is stable with output capacitance as low as 10 µF. Small ceramic capacitors can be used without the necessary addition of ESR, as is common with other regulators. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting, and reverse-current protection. The device is available as an adjustable device with a 1.21-V reference voltage. The 5962-1222402VHA is available in 10-pin CFP (U) package and 5962R1222403VXC is available in thermally-enhanced 10-pin CFP (HKU) package. Known good die (KGD) option is available for both 5962-1222402V9A for non-RHA version and 5962R1222403V9A for RHA.

6 Pin Configuration and Functions

U Package
10-Pin CFP
Top View



HKU Package
10-Pin CFP
Top View



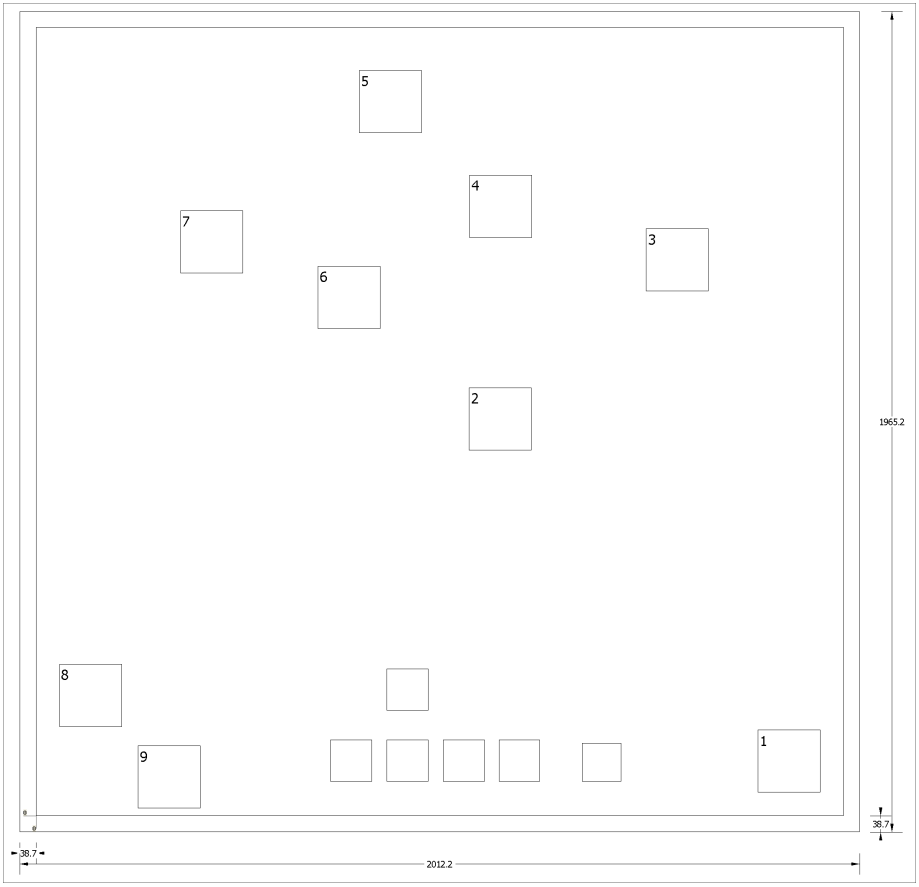
Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{SHDN}}$	1	I	Shutdown. $\overline{\text{SHDN}}$ is used to put the TPS7A4501 regulator into a low-power shutdown state. The output is off when $\overline{\text{SHDN}}$ is pulled low. $\overline{\text{SHDN}}$ can be driven by 5-V logic, 3-V logic, or open-collector logic with a pullup resistor. The pullup resistor is required to supply the pullup current of the open-collector gate, normally several microamperes, and $\overline{\text{SHDN}}$ current, typically 3 µA. If unused, the user must connect $\overline{\text{SHDN}}$ to V_{IN}. The device is in the low-power shutdown state if $\overline{\text{SHDN}}$ is not connected.
IN	2	I	Input. Power is supplied to the device through IN. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor (ceramic) in the range of 1 to 10 µF is sufficient. The TPS7A4501 regulator is designed to withstand reverse voltages on IN with respect to ground and on OUT. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device functions as if there is a diode in series with its input. No reverse current flows into the regulator, and no reverse voltage appears at the load. The device protects both itself and the load.
	3		
	4		
NC	5	NC	This pin is not connected to any internal circuitry. It can be left floating or tied to VIN or GND.
OUT	6	O	Output. The output supplies power to the load. To prevent oscillations, use a minimum output capacitor (ceramic) of 10 µF. Applications with large transient loads to limit peak voltage transients require larger output capacitors.
	7		
	8		
ADJ	9	I	Adjust. This is the input to the error amplifier. ADJ is internally clamped to ±7 V. It has a bias current of 3 µA that flows into the pin. ADJ voltage is 1.21 V referenced to ground, and the output voltage range is 1.21 to 20 V.
GND	10	—	Ground
Thermal Vias(1)	—	—	The exposed thermal vias of the HKU package should be connected to a wide ground plane for effective heat dissipation. Refer to Figure 30 and Figure 31 for the typical footprint of the HKU package.

(1) For HKU package

Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Floating	TiW/AlCu2	1627 nm



Bond Pad Coordinates in Microns(1)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
$\overline{\text{SHDN}}$	1	1729.25	55.5	1879.25	205.5
IN	2	1037.25	875	1187.25	1025
IN	3	1460.75	1255.5	1610.75	1405.5
IN	4	1037.75	1384.5	1187.75	1534.5
OUT	5	774.25	1634.75	924.25	1784.75
OUT	6	675.25	1166	825.25	1316
OUT	7	345.5	1299.25	495.5	1449.25
SENSE/ADJ	8	55.5	213	205.5	363
GND	9	244	17.5	394	167.5

(1) Substrate is not to be connected.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{IN}	Input voltage	IN	–22	22	V
		OUT	–22	22	
		Input-to-output differential (2)	–22	22	
		ADJ	–7	7	
		$\overline{SHDN}$	–22	22	
T_{lead}	Maximum lead temperature (10-s soldering time)			260	°C
T_J	Maximum operating junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum input-to-output differential voltage cannot be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 22 V, the OUT pin may not be pulled below 0 V. The total measured voltage from IN to OUT can not exceed ±22 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	–55		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS7A4501-SP		UNIT
		U (CFP)	HKU (CFP)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.6	51.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance (2)	10.3	6.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.6	31.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.7	5.42	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.5	31	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics (5962-1222402VHA and 5962-1222402V9A)

over operating junction temperature range T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP(1)	MAX	UNIT
V_{IN}	Minimum input voltage(2) (3)	I_{LOAD} = 500 mA	25°C		1.9	2.3	V
		I_{LOAD} = 750 mA	Full range		2.1	2.5	
V_{ADJ}	ADJ pin voltage(2) (4)	V_{IN} = 2.21 V, I_{LOAD} = 1 mA	25°C	1.196	1.21	1.224	V
		V_{IN} = 2.5 to 20 V, I_{LOAD} = 1 to 750 mA	Full range	1.174	1.21	1.246	
	Line regulation(2)	ΔV_{IN} = 2.21 to 20 V, I_{LOAD} = 1 mA	Full range		1.5	4.5	mV
	Load regulation(2)	V_{IN} = 2.5 V, ΔI_{LOAD} = 1 to 750 mA	25°C		2	8	mV
			Full range			18	
V_{DO}	Dropout voltage (V_{OUT} = 2.4 V) (5) (6)	I_{LOAD} = 1 mA	25°C		0.02	0.05	V
			Full range			0.07	
		I_{LOAD} = 100 mA	25°C		0.085	0.10	
			Full range			0.13	
		I_{LOAD} = 500 mA	25°C		0.17	0.21	
			Full range			0.27	
		I_{LOAD} = 750 mA	25°C		0.20	0.27	
			Full range			0.33	
I_{GND}	GND pin current(6) (7) V_{IN} = 2.5 V	I_{LOAD} = 0 mA,	Full range		1	1.5	mA
		I_{LOAD} = 1 mA	Full range		1.1	1.6	
		I_{LOAD} = 100 mA	Full range		3.3	7	
		I_{LOAD} = 500 mA	Full range		15	30	
		I_{LOAD} = 750 mA	Full range		28	45	
e_N (8)	Output voltage noise	C_{OUT} = 22 µF, I_{LOAD} = 750 mA, V_{IN} = 7 V, V_{OUT}= 5 V B_W = 10 Hz to 100 kHz	25°C		50		μV_{RMS}
I_{ADJ}	ADJ pin bias current(2) (9)		25°C		3	7	µA
	Shutdown threshold	V_{OUT} = OFF to ON	Full range		0.9	2	V
		V_{OUT} = ON to OFF	Full range	0.15	0.75		
$I_{\overline{SHDN}}$	$\overline{SHDN}$ pin current	$V_{\overline{SHDN}}$ = 0 V	25°C		0.01	1	µA
		$V_{\overline{SHDN}}$ = 20 V	25°C		3	20	
	Quiescent current in shutdown	V_{IN} = 6 V, $V_{\overline{SHDN}}$ = 0 V	25°C		0.01	1	µA
	Ripple rejection(10)	$V_{IN} - V_{OUT}$ = 1.5 V (avg), V_{RIPPLE} = 0.5 V_{P-P}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 0.75 A	25°C	60	68		dB
I_{LIMIT}	Current limit(10)	V_{IN} = 7 V, V_{OUT} = 0 V	25°C	1.7	1.9		A
		V_{IN} = 2.5 V	Full range	1.6	1.9		
I_{IL}	Input reverse leakage current	V_{IN} = –20 V, V_{OUT} = 0 V	Full range			300	µA
I_{RO}	Reverse output current(11)	V_{OUT} = 1.21 V, V_{IN} < 1.21 V	25°C		300	500	µA
TSD	Thermal shutdown temperature				175		°C

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) The TPS7A4501 is tested and specified for these conditions with the ADJ pin connected to the OUT pin.
(3) Dropout voltages are limited by the minimum input voltage specification under some output voltage/load conditions.
(4) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, limit the output current range. When operating at maximum output current, limit the input voltage range.
(5) Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to: $V_{IN} - V_{DROPOUT}$.
(6) To satisfy requirements for minimum input voltage, the TPS7A4501 is tested and specified for these conditions with an external resistor divider (two 4.12-kΩ resistors) for an output voltage of 2.4 V. The external resistor divider adds a 300-µA DC load on the output.
(7) GND pin current is tested with V_{IN} = 2.5 V and a current source load. The GND pin current decreases at higher input voltages.
(8) Parameter is specified by bench characterization and is not tested in production.
(9) ADJ pin bias current flows into the ADJ pin.
(10) Parameter is specified by characterization for KGD and is not tested in production.
(11) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

7.6 Electrical Characteristics (5962R1222403VXC and 5962R1222403V9A)

Over operating junction temperature range T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP(1)	MAX	UNIT
V_{IN}	Minimum input voltage(2) (3)	I_{LOAD} = 1.5 A	Full range		2.1	2.9	V
V_{ADJ}	ADJ pin voltage(2) (4)	V_{IN} = 2.9 to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	1.174	1.21	1.246	V
	Line regulation(2)	ΔV_{IN} = 2.9 to 20 V, I_{LOAD} = 1 mA	Full range		2.5	6.5	mV
	Load regulation(2)	V_{IN} = 2.9 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		2	10	mV
			Full range			18	
V_{DO}	Dropout voltage (V_{OUT} = 19.3 V)(5) (6)	I_{LOAD} = 1 mA	25°C		0.08	0.32	V
			Full range			0.40	
		I_{LOAD} = 100 mA	25°C		0.14	0.40	
			Full range			0.58	
		I_{LOAD} = 500 mA	25°C		0.25	0.40	
			Full range			0.60	
		I_{LOAD} = 750 mA	25°C		0.30	0.40	
			Full range			0.62	
		I_{LOAD} = 1 A	25°C		0.34	0.45	
			Full range			0.65	
		I_{LOAD} = 1.25 A	25°C		0.40	0.50	
			Full range			0.68	
		I_{LOAD} = 1.5 A	25°C		0.45	0.60	
			Full range			0.75	

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) The TPS7A4501 is tested and specified for these conditions with the ADJ pin connected to the OUT pin.
(3) Dropout voltages are limited by the minimum input voltage specification under some output voltage/load conditions.
(4) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, limit the output current range. When operating at maximum output current, limit the input voltage range.
(5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to: $V_{IN} – V_{DROPOUT}$.
(6) To satisfy requirements for minimum input voltage, the TPS7A4501 is tested and specified for these conditions with an external resistor divider (one 4.12-kΩ resistor and one 61.9-kΩ) for an output voltage of 19.3 V. The external resistor divider adds a 300-µA DC load on the output.

Electrical Characteristics (5962R1222403VXC and 5962R1222403V9A) (continued)

Over operating junction temperature range T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP(1)	MAX	UNIT
I_{GND}	GND pin current(7) (8) V_{IN} = 2.9 V	I_{LOAD} = 0 mA	Full range		1	1.5	mA
		I_{LOAD} = 1 mA	Full range		1.1	1.6	
		I_{LOAD} = 100 mA	Full range		3.3	7	
		I_{LOAD} = 500 mA	Full range		8.5	30	
		I_{LOAD} = 750 mA	Full range		15	45	
		I_{LOAD} = 1 A	Full range		25	50	
		I_{LOAD} = 1.25 A	Full range		36	80	
		I_{LOAD} = 1.5 A	Full range		53	105	
e_N (9)	Output voltage noise	C_{OUT} = 22 µF, I_{LOAD} = 1.5 A, V_{IN} = 5.5 V, V_{OUT} = 5 V B_W = 10 Hz to 100 kHz	25°C		50		μV_{RMS}
I_{ADJ}	ADJ pin bias current(2) (10)		25°C		3	7	µA
			Full range		5.5	15	
	Shutdown threshold	V_{OUT} = OFF to ON	Full range		0.9	2	V
		V_{OUT} = ON to OFF	Full range	0.15	0.75		
$I_{\overline{SHDN}}$	$\overline{SHDN}$ pin current	$V_{\overline{SHDN}}$ = 0 V	Full range		0.01	1	µA
		$V_{\overline{SHDN}}$ = 20 V	Full range		3	20	
	Quiescent current in shutdown	V_{IN} = 6 V, $V_{\overline{SHDN}}$ = 0 V	Full range		0.01	10	µA
		V_{IN} = 6 V, $V_{\overline{SHDN}}$ = 0 V, Post 100kRads (si), T_J = 25°C(11)	25°C		15	50	
	Ripple rejection(12)	$V_{IN} – V_{OUT}$ = 1.5 V (avg), V_{RIPPLE} = 0.5 V_{P-P}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 0.75 A	25°C	60	68		dB
			Full range	58	63		
		$V_{IN} – V_{OUT}$ = 1.5 V (avg), V_{RIPPLE} = 0.5 V_{P-P}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 1.5 A	25°C	50	60		
			Full range	44	52		
I_{LIMIT}	Current limit(12)	V_{IN} = 7 V, V_{OUT} = 0 V	Full range	1.7	1.9		A
		V_{IN} = 2.9 V	Full range	1.6	1.9		
I_{IL}	Input reverse leakage current	V_{IN} = –20 V, V_{OUT} = 0 V	Full range			300	µA
I_{RO}	Reverse output current(13)	V_{OUT} = 1.21 V, V_{IN} < 1.21 V	Full range		300	500	µA
TSD	Thermal shutdown temperature				175		°C

(7) To satisfy requirements for minimum input voltage, the TPS7A4501 is tested and specified for these conditions with an external resistor divider (two 4.12-kΩ resistors) for an output voltage of 2.4 V. The external resistor divider adds a 300-µA DC load on the output.
(8) GND pin current is tested with V_{IN} = 2.9 V and a current source load. The GND pin current decreases at higher input voltages.
(9) Parameter is specified by bench characterization and is not tested in production.
(10) ADJ pin bias current flows into the ADJ pin.
(11) This maximum limit applies to SMD 5962R1222403VXC post 100kRads (Si) test at 25°C.
(12) Parameter is specified by characterization for KGD and is not tested in production.
(13) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

7.7 Typical Characteristics

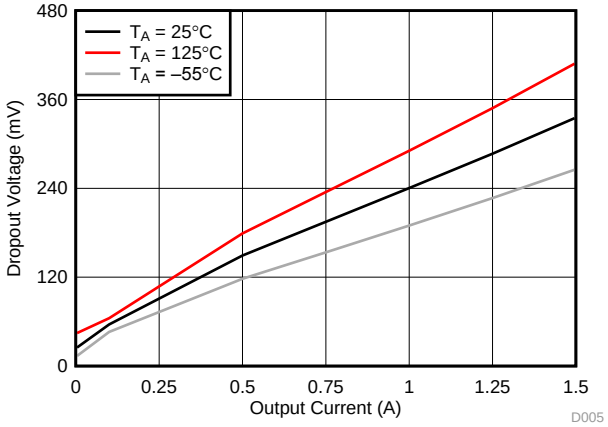
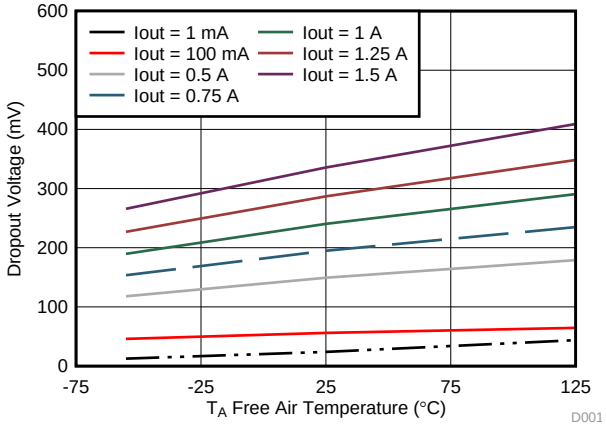
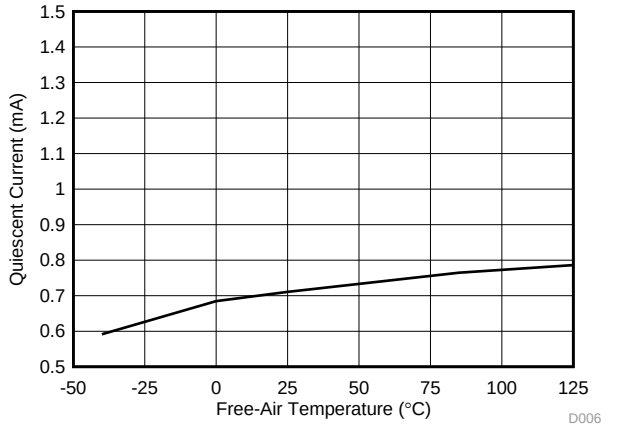


Figure 1. Dropout Voltage vs Output Current



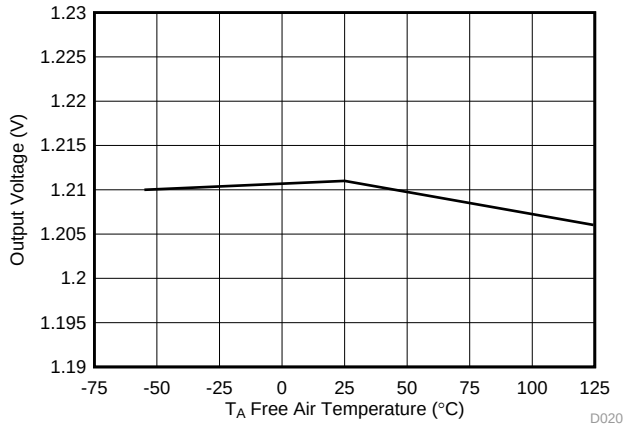
V_{OUT} = 2.4 V

Figure 2. Dropout Voltage vs Temperature



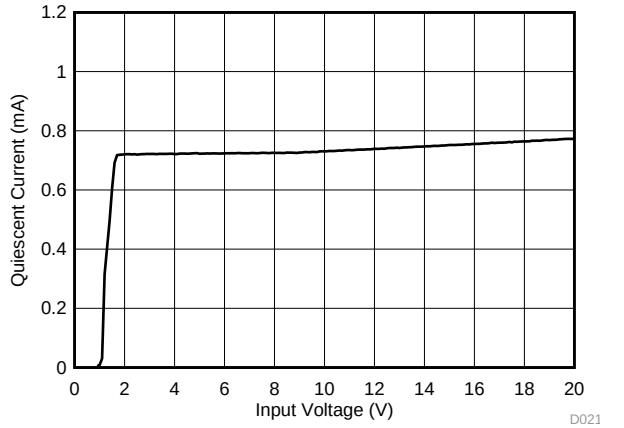
V_{IN} = 6 V I_{OUT} = 0 A V_{SHDN} = V_{IN}

Figure 3. Quiescent Current vs Temperature



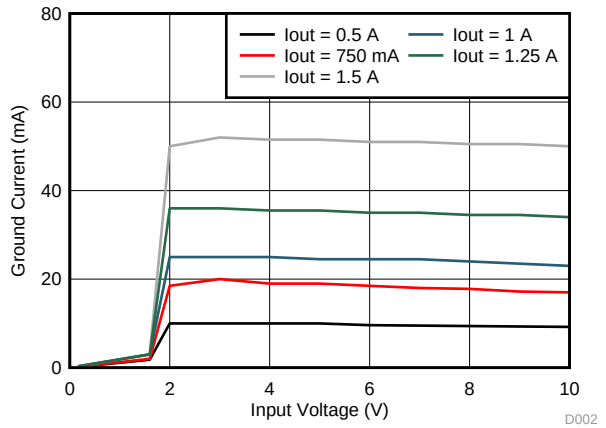
I_{OUT} = 1 mA V_{IN} = 2.9 V

Figure 4. Output Voltage vs Temperature



T_J = 25°C R_{OUT} = 4.3 kΩ V_{SHDN} = V_{IN}

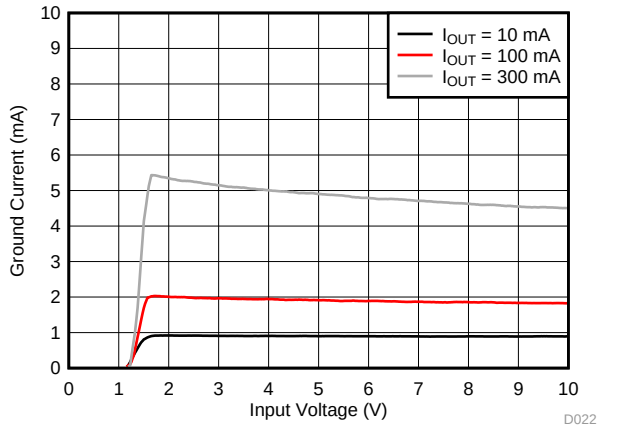
Figure 5. Quiescent Current vs Input Voltage



T_J = 25°C V_{SHDN} = V_{IN}
V_{OUT} = 1.21 V

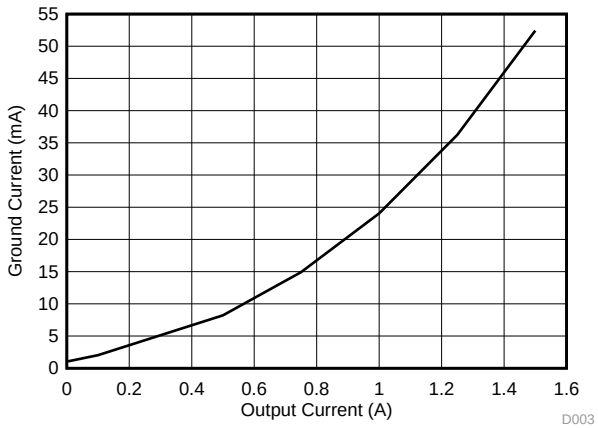
Figure 6. Ground Current vs Input Voltage

Typical Characteristics (continued)



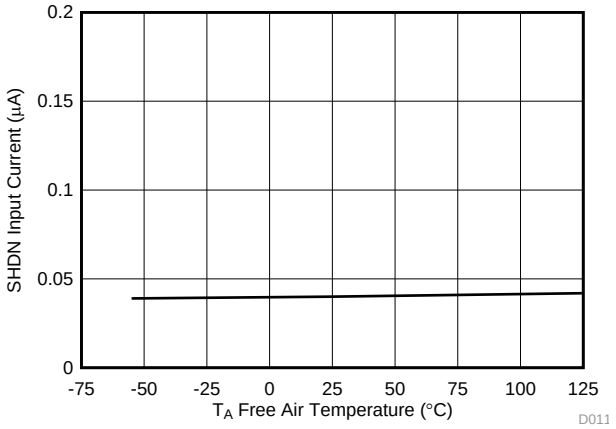
T_J = 25°C V_{SHDN} = V_{IN} V_{OUT} = 1.21 V

Figure 7. Ground Current vs Input Voltage



V_{IN} = V_{OUT}(nom) + 1

Figure 8. Ground Current vs Output Current



V_{SHDN} = 0 V

Figure 9. SHDN Input Current vs Temperature

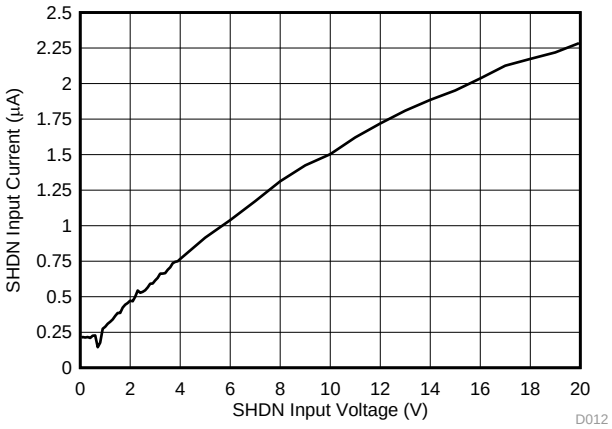
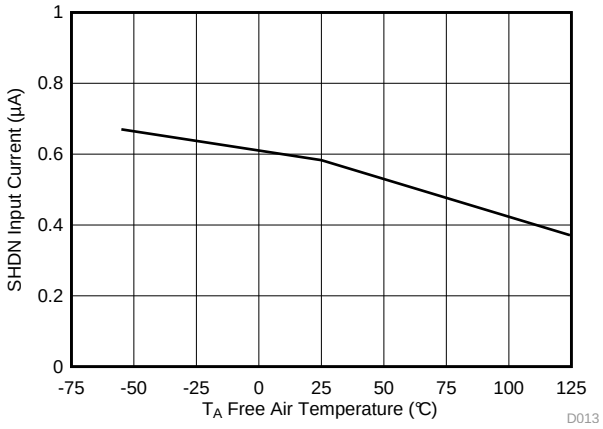
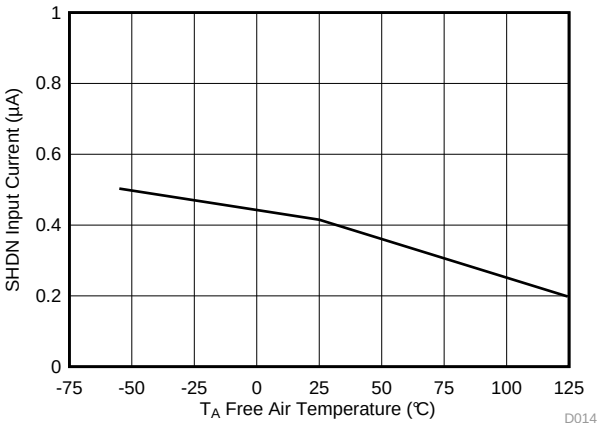


Figure 10. SHDN Input Current vs SHDN Input Voltage



I_{OUT} = 1 mA

Figure 11. SHDN Threshold (Off To On) vs Temperature



I_{OUT} = 1 mA

Figure 12. SHDN Threshold (On to Off) vs Temperature

Typical Characteristics (continued)

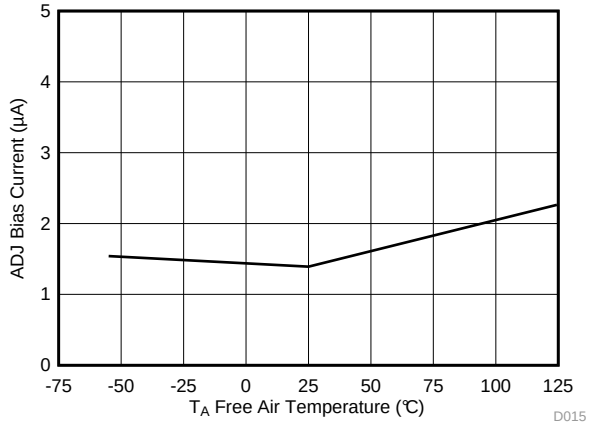
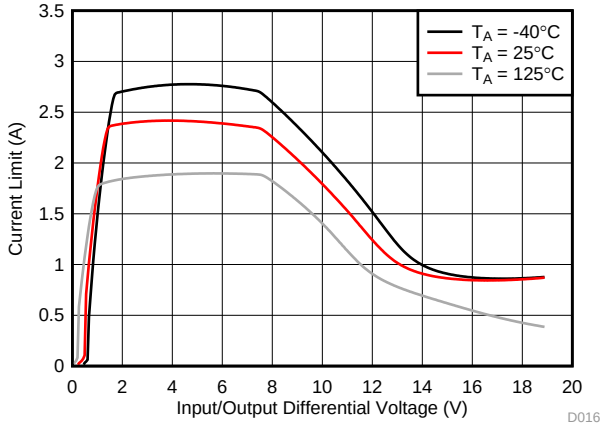
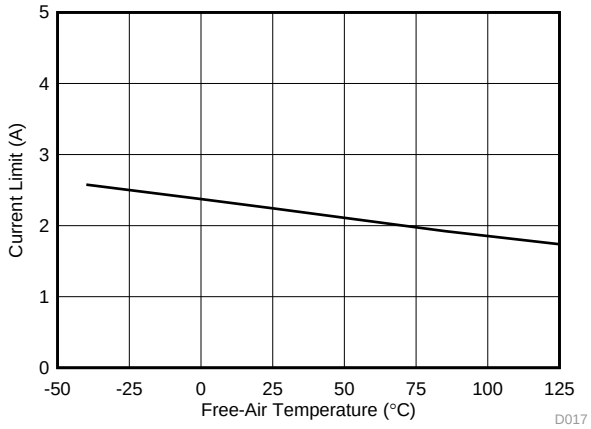


Figure 13. ADJ Bias Current vs Temperature



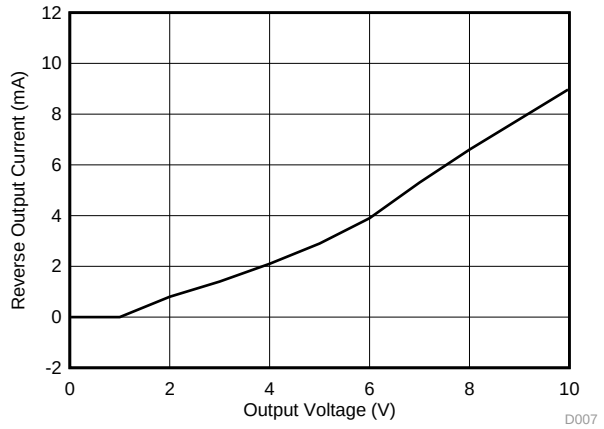
ΔV_{OUT} = 100 mV

Figure 14. Current Limit vs Input/Output Differential Voltage



V_{IN} = 7 V V_{OUT} = 0 V

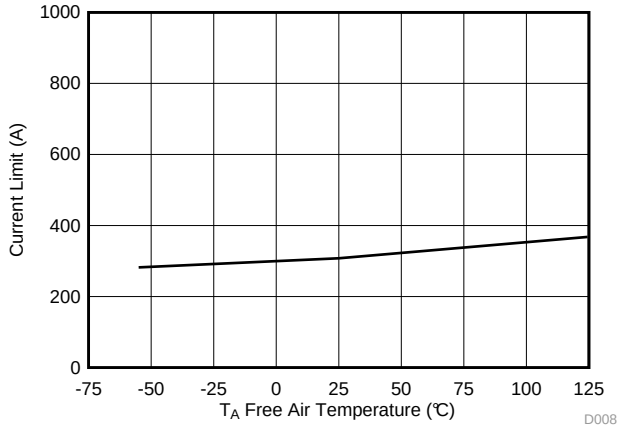
Figure 15. Current Limit vs Temperature



T_J = 25°C V_{IN} = 0 V V_{OUT} = V_{ADJ}

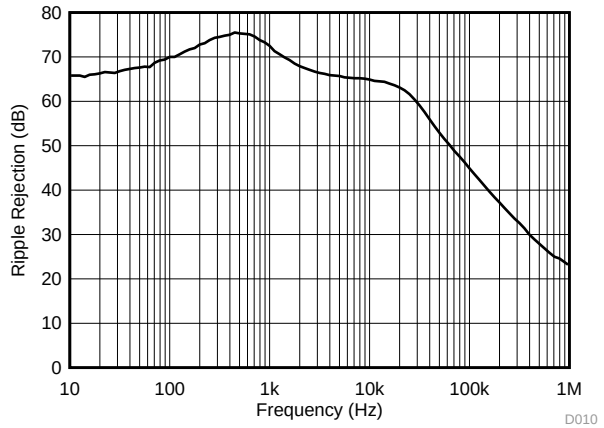
Current flows into OUT pin

Figure 16. Reverse Output Current vs Output Voltage



V_{IN} = 0 V V_{OUT} = 1.21 V

Figure 17. Reverse Output Current vs Temperature



V_{IN} = 2.7 V C_{IN} = 0 C_{OUT} = 10 µF (ceramic)

I_{OUT} = 750 mA V_{Ripple} = 0.05 V_{PP} T_A = 25°C

Figure 18. Ripple Rejection vs Frequency

Typical Characteristics (continued)

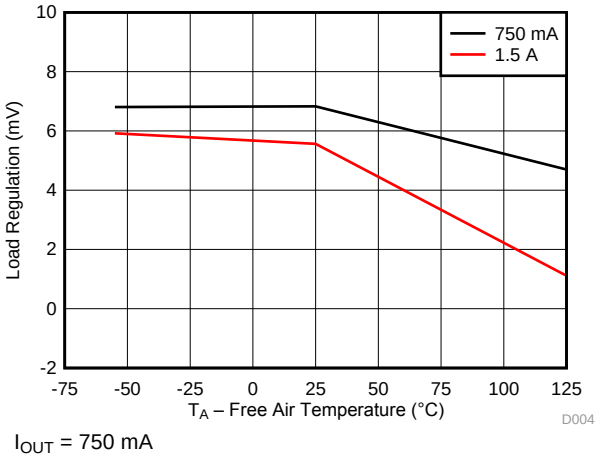


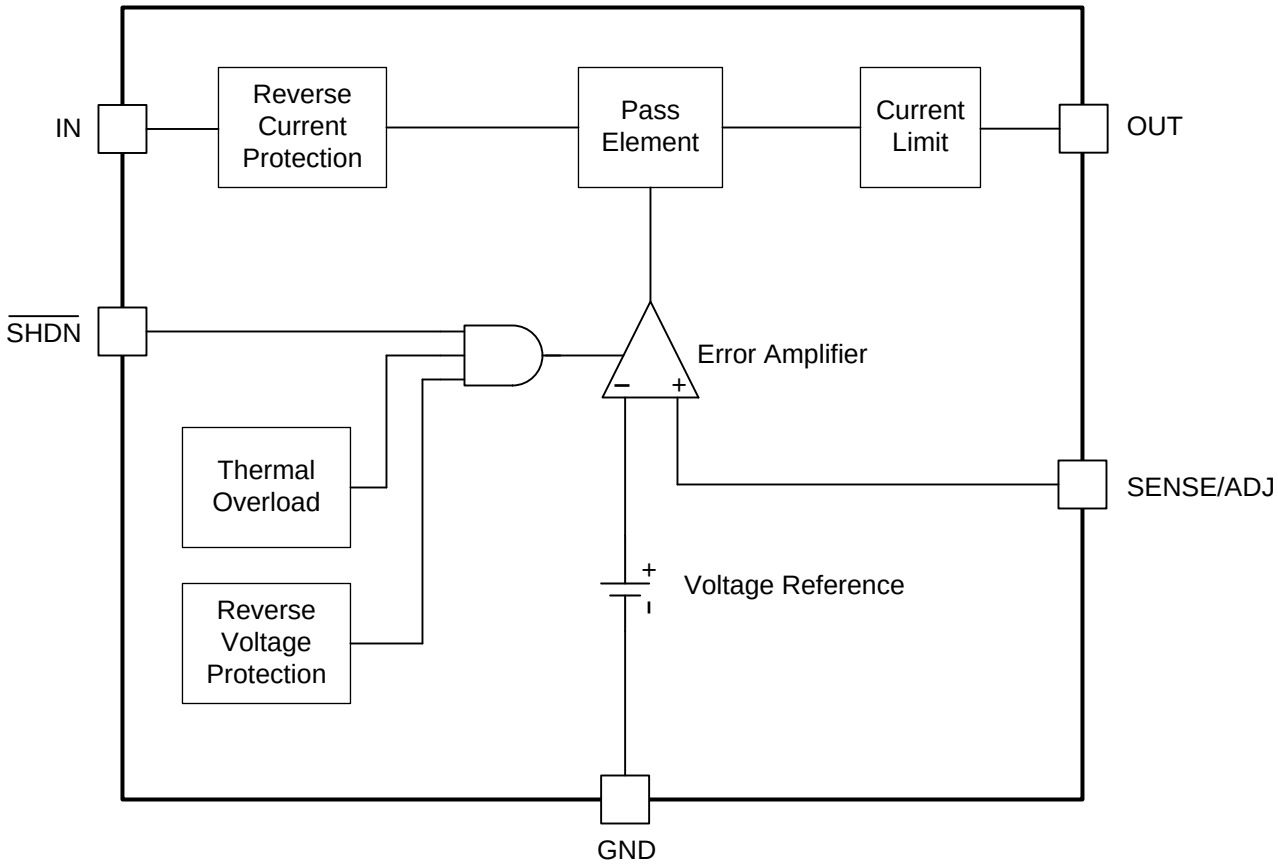
Figure 19. Load Regulation vs Temperature

8 Detailed Description

8.1 Overview

The TPS7A4501-SP is a 1.5-A LDO regulator optimized for fast-transient response. The devices are capable of supplying 1.5 A at a dropout voltage of 320 mV. The low operating quiescent current (1 mA) drops to less than 50 µA in shutdown. In addition to the low quiescent current, the TPS7A4501-SP regulators incorporate several protection features that make them ideal for use in battery-powered systems. The devices are protected against both reverse input and reverse output voltages. In battery-backup applications where the output can be held up by a backup battery when the input is pulled to ground, the TPS7A4501-SP functions as if it has a diode in series with its output and prevents reverse current flow. Additionally, in dual-supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as (20 V – VIN) and still allow the device to start and operate.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjustable Operation

The adjustable TPS7A4501-SP has an output voltage range of 1.21 to 20 V. The output voltage is set by the ratio of two external resistors as shown in Figure 20. The device maintains the voltage at the ADJ pin at 1.21 V referenced to ground. The current in R1 is then equal to (1.21 V/R1), and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3 µA at 25°C, flows through R2 into the ADJ pin. Calculate the output voltage using the formula shown in Figure 20. The value of R1 should be less than 4.17 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown, the output is turned off, and the divider current is zero.

Feature Description (continued)

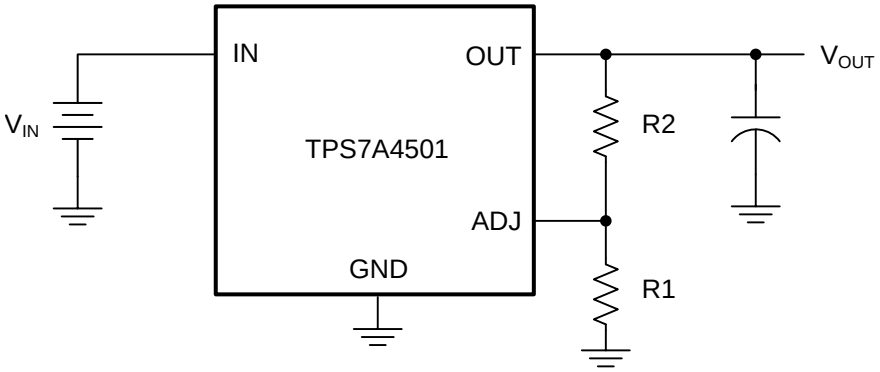


Figure 20. Adjustable Operation Schematic

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 1.21 V. Specifications for output voltages greater than 1.21 V are proportional to the ratio of the desired output voltage to 1.21 V: V_{OUT} / 1.21 V. For example, load regulation for an output current change of 1 mA to 1.5 A is –3 mV (typical) at V_{OUT} = 1.21 V. At V_{OUT} = 5 V, load regulation is:

(5 V / 1.21 V)(–3 mV) = –12.4 mV (1)

8.3.2 Fixed Operation

The TPS7A4501-SP can be used in a fixed-voltage configuration. Connect the SENSE/ADJ pin to OUT for proper operation. Figure 21 shows an example of this for a fixed output voltage of 1.21 V. During fixed voltage operation, the SENSE/ADJ pin can be used for a Kelvin connection if routed separately to the load. This allows the regulator to compensate for voltage drop across parasitic resistances (RP) between the output and the load. This compensation becomes more crucial with higher-load currents.

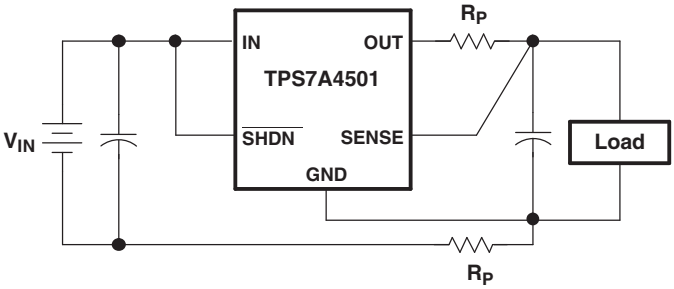


Figure 21. Kelvin Sense Connection

8.3.3 Overload Recovery

Like many IC power regulators, the TPS7A4501-SP has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very-heavy loads. During start up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so it is not unique to the TPS7A4501-SP.

Feature Description (continued)

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short circuit or when the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to 0 and brought up again to make the output recover.

8.3.4 Output Voltage Noise

The TPS7A4501-SP regulator is designed to provide low output voltage noise over the 10-Hz to 100-kHz bandwidth while operating at full load. Output voltage noise is typically 50 μV/√Hz over this frequency bandwidth for the TPS7A4501-SP. For higher output voltages (generated by using a resistor divider), the output voltage noise is gained up accordingly.

Higher values of output voltage noise may be measured when care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TPS7A4501-SP. The user must also consider power-supply ripple rejection; the TPS7A4501-SP regulator does not have unlimited power-supply rejection and passes a small portion of the input noise through to the output.

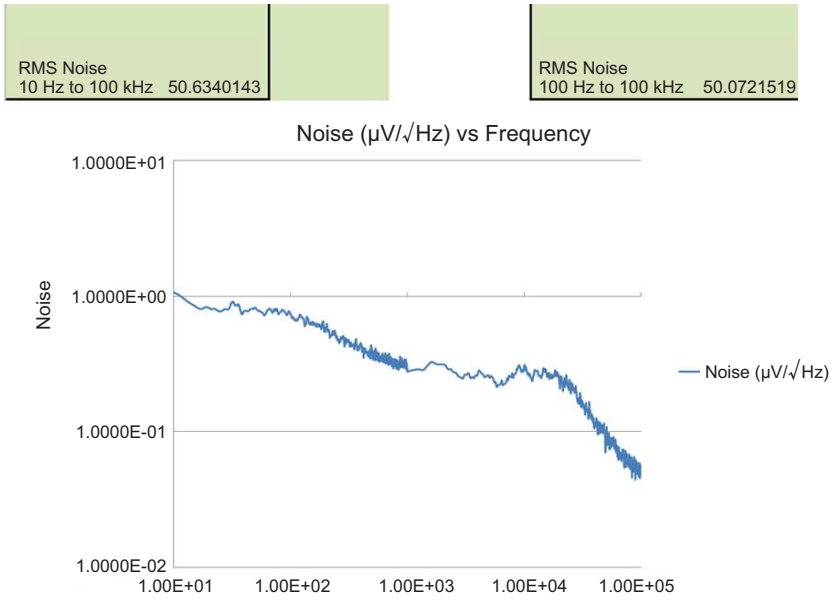


Figure 22. Output Noise Plot, V_{IN} = 7 V, V_{OUT} = 5 V At 750 mA , C_{OUT} = 22 μF Tantalum Capacitor

8.3.5 Protection Features

The TPS7A4501-SP regulator incorporates several protection features, which makes the regulator ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages, reverse output voltages, and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C. TPS7A4501-SP incorporates thermal protection which disables the output when the junction temperature rises approximately 175°C, allowing the device to cool.

The input of the device withstands reverse voltages of 20 V. Current flow into the device is limited to less than 1 mA (typically less than 100 μA), and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries that can be plugged in backward.

Feature Description (continued)

The output of the TPS7A4501-SP can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20 V. The output acts like an open circuit; no current flows out of the pin. If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case, grounding the $\overline{\text{SHDN}}$ pin turns off the device and stops the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the ADJ pin acts like an open circuit when pulled below ground and like a large resistor (typically 5 kΩ) in series with a diode when pulled above ground.

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7-V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5-V output from the 1.21-V reference when the output is forced to 20 V. Choose the top resistor of the resistor divider so as to limit the current into the ADJ pin to <5 mA when the ADJ pin is at 7 V. The 13-V difference between OUT and ADJ divided by the 5-mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6 kΩ.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit.

When the IN pin of the TPS7A4501-SP is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2 µA. This can happen if the input of the device is connected to a discharged (low-voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the $\overline{\text{SHDN}}$ pin has no effect on the reverse output current when the output is pulled above the input.

8.4 Device Functional Modes

Table 1 shows the device modes.

Table 1. Device Modes

SHDN	DEVICE STATE
H	Regulated voltage
L	Shutdown

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7A4501-SP regulator has very-low output noise, which makes it ideal for sensitive RF supply applications.

9.2 Typical Application

This section highlights some of the design considerations when implementing this device in various applications.

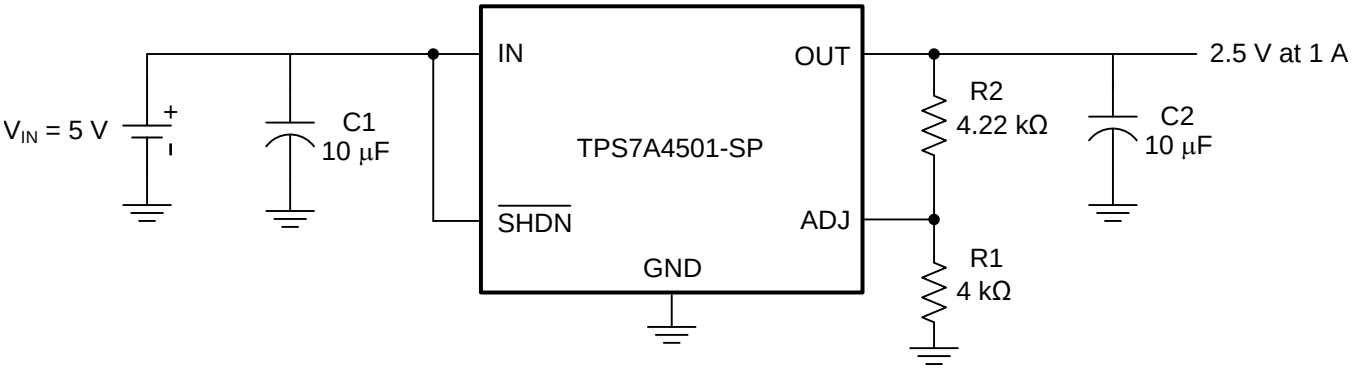


Figure 23. Adjustable Output Voltage Operation

9.2.1 Design Requirements

Table 2 shows the design requirements.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (VIN)	5 V
Output voltage (VOUT)	2.5 V
Output current (IOUT)	0 to 1 A
Load regulation	1%

9.2.2 Detailed Design Procedure

The TPS7A4501-SP has an adjustable output voltage range of 1.21 to 20 V. The output voltage is set by the ratio of two external resistors, R1 and R2, as shown in Figure 23. The device maintains the voltage at the ADJ pin at 1.21 V referenced to ground. The current in R1 is then equal to (1.21 V/R1), and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3 µA at 25°C, flows through R2 into the ADJ pin. Calculate the output voltage using Equation 2.

$$V_{OUT} = 1.21V\left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2 \quad (2)$$

The value of R1 should be less than 4.17 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off, and the divider current is zero. For an output voltage of 2.50 V, R1 is set to 4 kΩ. R2 is then found to be 4.22 kΩ using Equation 2.

$$V_{OUT} = 1.21V\left(1 + \frac{4.22k\Omega}{4.0k\Omega}\right) + 3\mu A \times 4.22k\Omega \quad (3)$$

V_{OUT} = 2.50 V (4)

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 1.21 V. Specifications for output voltages greater than 1.21 V are proportional to the ratio of the desired output voltage to 1.21 V: V_{OUT} / 1.21 V. For example, load regulation for an output current change of 1 mA to 1.5 A is –2 mV (typical) at V_{OUT} = 1.21 V. At V_{OUT} = 2.50 V, the typical load regulation is:

(2.50 V / 1.21 V)(–2 mV) = –4.13 mV (5)

shows the actual change in output is about 3 mV for a 1-A load step. The maximum load regulation at 25°C is –8 mV. At V_{OUT} = 2.50 V, the maximum load regulation is:

(2.50 V / 1.21 V)(–8 mV) = –16.53 mV (6)

Because 16.53 mV is only 0.7% of the 2.5-V output voltage, the load regulation meets the design requirements.

9.2.2.1 Output Capacitance and Transient Response

The TPS7A4501-SP regulator is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. TI recommends a minimum output capacitor of 10 µF with an ESR of 3 Ω or less to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS7A4501-SP, increase the effective output capacitor value.

Give extra consideration to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectric used for a harsh environment is X7R. Ceramic capacitors lose capacitance when DC bias is applied across the capacitor. This capacitance loss is due to the polarization of the ceramic material. The capacitance loss is not permanent: after a large DC bias is applied, reducing the DC bias reduces the degree of polarization and capacitance increases. DC bias effects vary dramatically with voltage rating, case size, capacitor value, and capacitor manufacturer. Because a capacitor could lose more than 50% of its capacitance with DC bias voltages near the voltage rating of the capacitor, it is important to consider DC bias when selecting a ceramic capacitor for an application.

Ceramic capacitors' dielectric also changes over the temperature range. For example X7R, the first letter **X** denotes lower temperature range –55°C whereas 7 denotes a higher temperature range 125°C and R denotes capacitance variation over the temperature range (±15%). For harsh environment applications, minimum dielectric thickness must be 1 mil for 100-V DC-rated capacitor and 0.8 mil for 50-V DC-rated capacitors.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

Tantalum capacitors can provide higher capacitance per unit volume. Tantalum capacitors can be either manganese dioxide (MNO2)-based capacitors where the cathode is MN02 or polymer. MN02-based tantalum capacitors exhibit high ESR as compared to polymer-based tantalum capacitors. MN02-based tantalum capacitors require in excess of 60% voltage derating. Thus, a 10-V rated capacitor can only be used for 3.3-V application. Whereas polymer-based capacitors only require 10% voltage derating. Paralleling ceramic and tantalum capacitors provide optimum balance between capacitance and ESR.

Table 3 highlights some of the capacitors used in the device.

Table 3. TPS7A4501-SP Capacitors

CAPACITOR PART NUMBER	CAPACITOR DETAILS TYPE VENDOR (CAPACITOR, VOLTAGE, ESR)	TYPE	VENDOR
T493X226M025AH6x20	22 µF, 25 V, 35 mΩ	Tantalum - MnO2	Kemet
T525D476M016ATE035	47 µF, 10 V, 35 mΩ	Tantalum - Polymer	Kemet
T525D107M010ATE025	100 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T541X337M010AH6720	330 µF, 10 V, 6 mΩ	Tantalum - Polymer	Kemet
T525D227M010ATE025	220 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T495X107K016ATE100	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
CWR29FK227JTHC	220 µF, 10 V, 180 mΩ	Tantalum - MnO2	AVX
THJE107K016AJH	100 µF, 16 V, 58 mΩ	Tantalum	AVX
THJE227K010AJH	220 µF, 10 V, 40 mΩ	Tantalum	AVX
SR2225X7R335K1P5#M123	3.3 µF, 25 V, 10 mΩ	Ceramic	Presidio Components Inc

9.2.2.2 Compensation

TPS7A4501-SP is internally compensated. However, the user can implement a lead network using C_3 to boost the phase margin as well as reduce output noise.

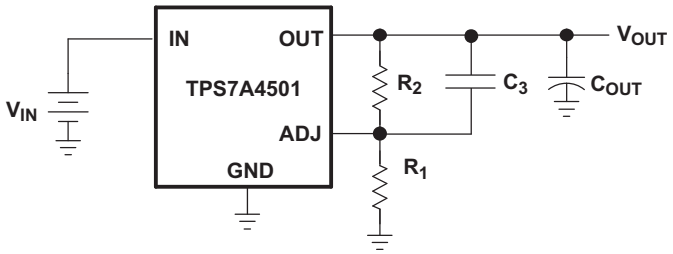


Figure 24. Compensation Schematic

R_1, the bottom resistor, and R_2, the top resistor, form the output voltage divider network. C_3 across R_2 adds a lead network.

For R_1 = 3.2 kΩ and R_2 = 10 kΩ, V_{OUT} is set at 5 V and C_3 = 470 pF.

Zero and pole can be calculated as shown in the following equations.

$$f_{z2} = \frac{1}{2 \times \pi \times R_2 \times C_3} \quad (7)$$

$$f_{z2} = 33.863 \text{ kHz} \quad (8)$$

$$R_{1p} = \frac{R_1 \times R_2}{R_1 + R_2} \quad (9)$$

$$R_{1p} = 2.424 \text{ k}\Omega \quad (10)$$

$$f_{p2} = \frac{1}{2 \times \pi \times R_{1p} \times C_3} \quad (11)$$

$$f_{p2} = 139.684 \text{ kHz} \quad (12)$$

9.2.3 Application Curves

The following waveforms indicate the transient behavior of the TPS7A4501-SP.

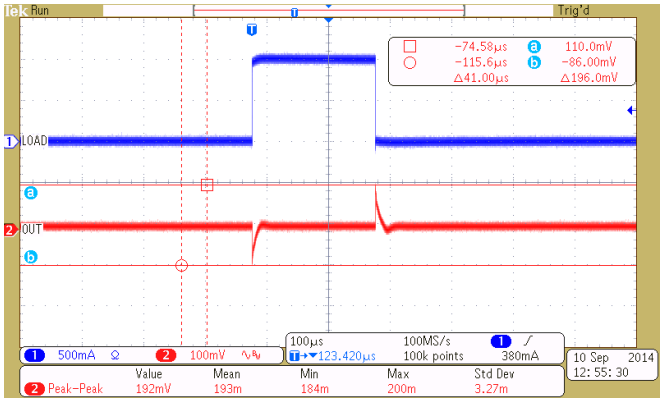


Figure 25. 1-A Load Transient Response, Step Load is from 0.1 to 1.1 A, Vin = 5 V, Vout = 2.5 V

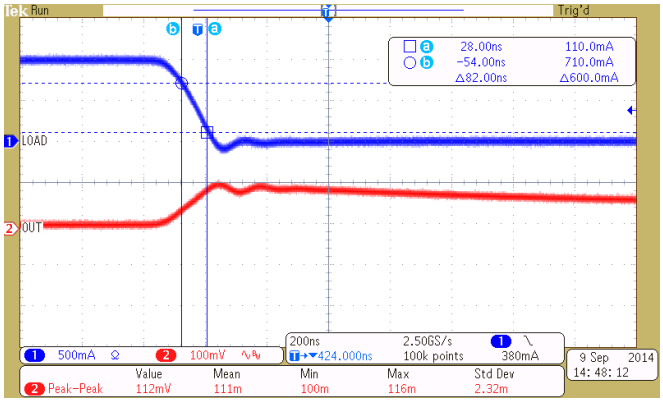


Figure 26. 1-A Load, Expanded View (High to Low), Slew Rate = 7.3 A/µS

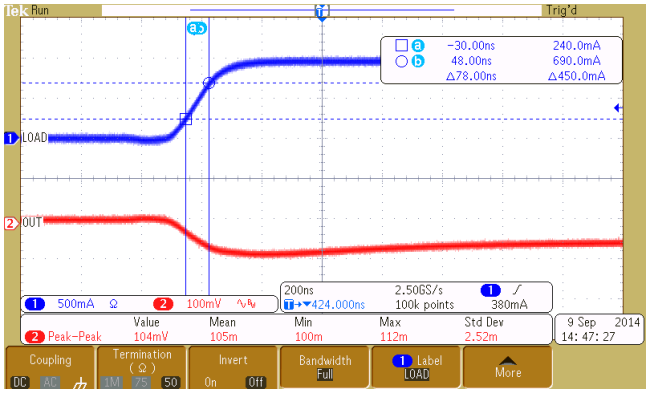


Figure 27. 1-A Load, Expanded View (Low to High), Slew Rate = 5.8 A/µS

10 Power Supply Recommendations

The device is designed to operate with an input voltage supply up to 20 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

11 Layout

11.1 Layout Guidelines

- For best performance, all traces should be as short as possible.
- Use wide traces for IN, OUT, and GND to minimize the parasitic electrical effects.
- TI recommends a minimum output capacitor of 10 µF with an ESR of 3 Ω or less to prevent oscillations. X7R dielectrics are preferred.
- Place the output capacitor (COUT) as close as possible to the OUT pin of the device.
- $\overline{\text{SHDN}}$ can be driven by 5-V logic, 3-V logic, or open-collector logic with a pullup resistor.The device is in the low-power shutdown state if $\overline{\text{SHDN}}$ is not connected.
- The exposed thermal vias of the HKU package should be connected to a wide ground plane for effective heat dissipation. Refer to Figure 29, Figure 30, and Figure 31 for the typical footprint of the HKU package.

11.2 Layout Example

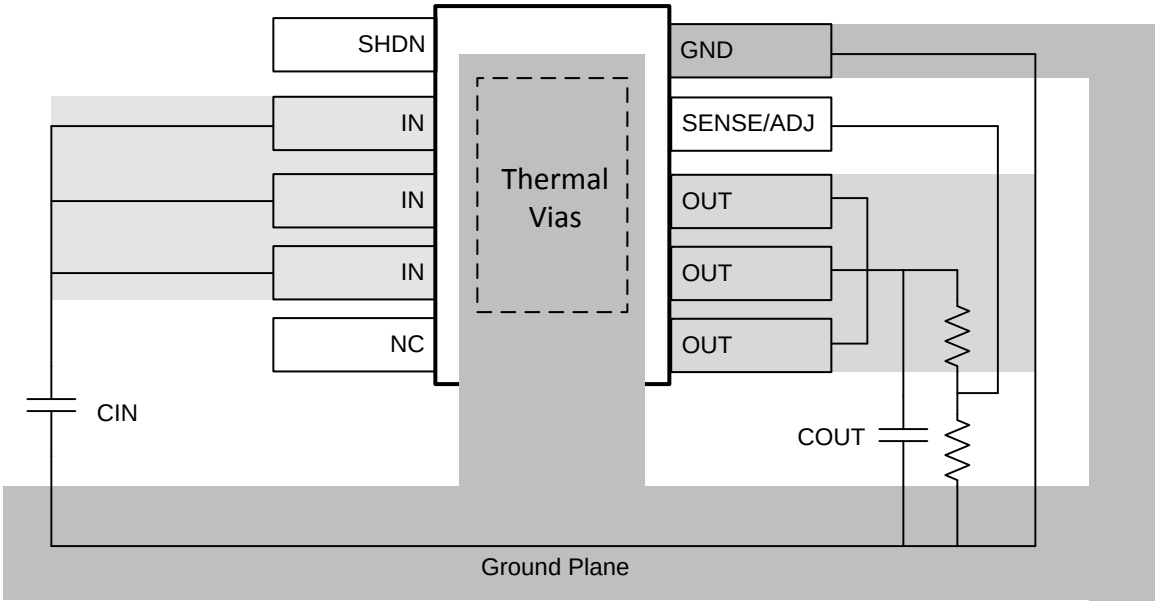


Figure 28. Example of Layout

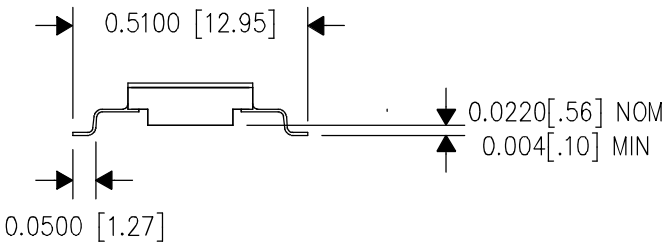


Figure 29. Typical HKU Package With Leads Form

Layout Example (continued)

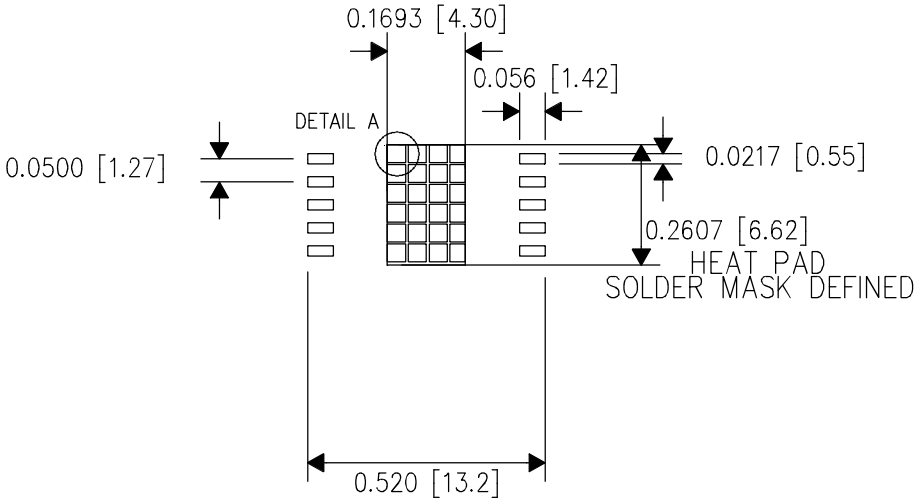


Figure 30. Typical Thermal Vias Footprint

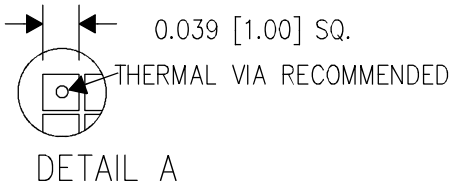


Figure 31. Typical Thermal Vias Details

11.3 Thermal Considerations

The power-handling capability of the device is limited by the maximum-rated junction temperature (125°C). The power dissipated by the device is made up of two components:

- Output current multiplied by the input/output voltage differential: $I_{OUT}(V_{IN} – V_{OUT})$
- GND pin current multiplied by the input voltage: $I_{GND}V_{IN}$.

Find the GND pin current by using the GND pin current graphs in *Typical Characteristics*. Power dissipation is equal to the sum of the two components listed previously.

The TPS7A4501-SP regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, do not exceed the maximum junction temperature rating of 125°C. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Also consider additional heat sources mounted nearby.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

11.3.1 Calculating Junction Temperature

Example: Given an output voltage of 3.3 V, an input voltage range of 4 to 6 V, an output current range of 0 to 500 mA, and a maximum case temperature of 50°C, what is the maximum junction temperature?

The power dissipated by the device is equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} – V_{OUT}) + I_{GND}(V_{IN(MAX)})$$

where

- $I_{OUT(MAX)}$ = 500 mA
- $V_{IN(MAX)}$ = 6 V

Thermal Considerations (continued)

- I_{GND} at (I_{OUT} = 500 mA, V_{IN} = 6 V) = 10 mA (13)

So,

$$P = 500\ mA \times (6\ V - 3.3\ V) + 10\ mA \times 6\ V = 1.41\ W \quad (14)$$

Using a U package, the thermal resistance is about 10.3°C/W. So the junction temperature rise above case is approximately equal to:

$$1.41\ W \times 10.3°C/W = 14.5°C \quad (15)$$

The maximum junction temperature is then equal to the maximum junction-temperature rise above case plus the maximum case temperature or:

$$T_{JMAX} = 50°C + 14.5°C = 64.5°C \quad (16)$$

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1222402V9A	ACTIVE	XCEPT	KGD	0	100	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962-1222402VHA	ACTIVE	CFP	U	10	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	1222402VHA 7A4501-SP	Samples
5962R1222403V9A	ACTIVE	XCEPT	KGD	0	50	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962R1222403VXC	ACTIVE	CFP	HKU	10	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	R1222403VXC 7A4501-RHA	Samples
TPS7A4501HKU/EM	ACTIVE	CFP	HKU	10	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	25 to 25	7A4501HKU/EM EVAL ONLY	Samples
TPS7A4501U/EM	ACTIVE	CFP	U	10	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	25 to 25	7A4501U/EM EVAL ONLY	Samples
TPS7A4501Y/EM	ACTIVE	XCEPT	KGD	0	5	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

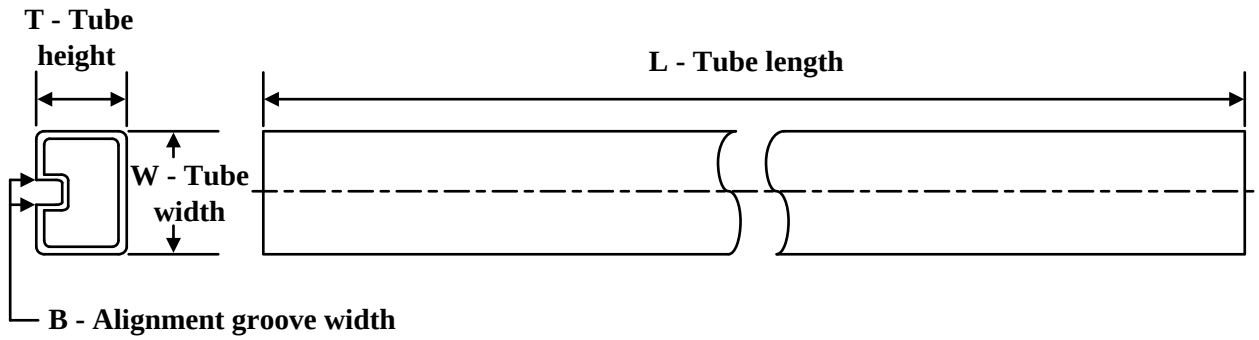
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



*All dimensions are nominal

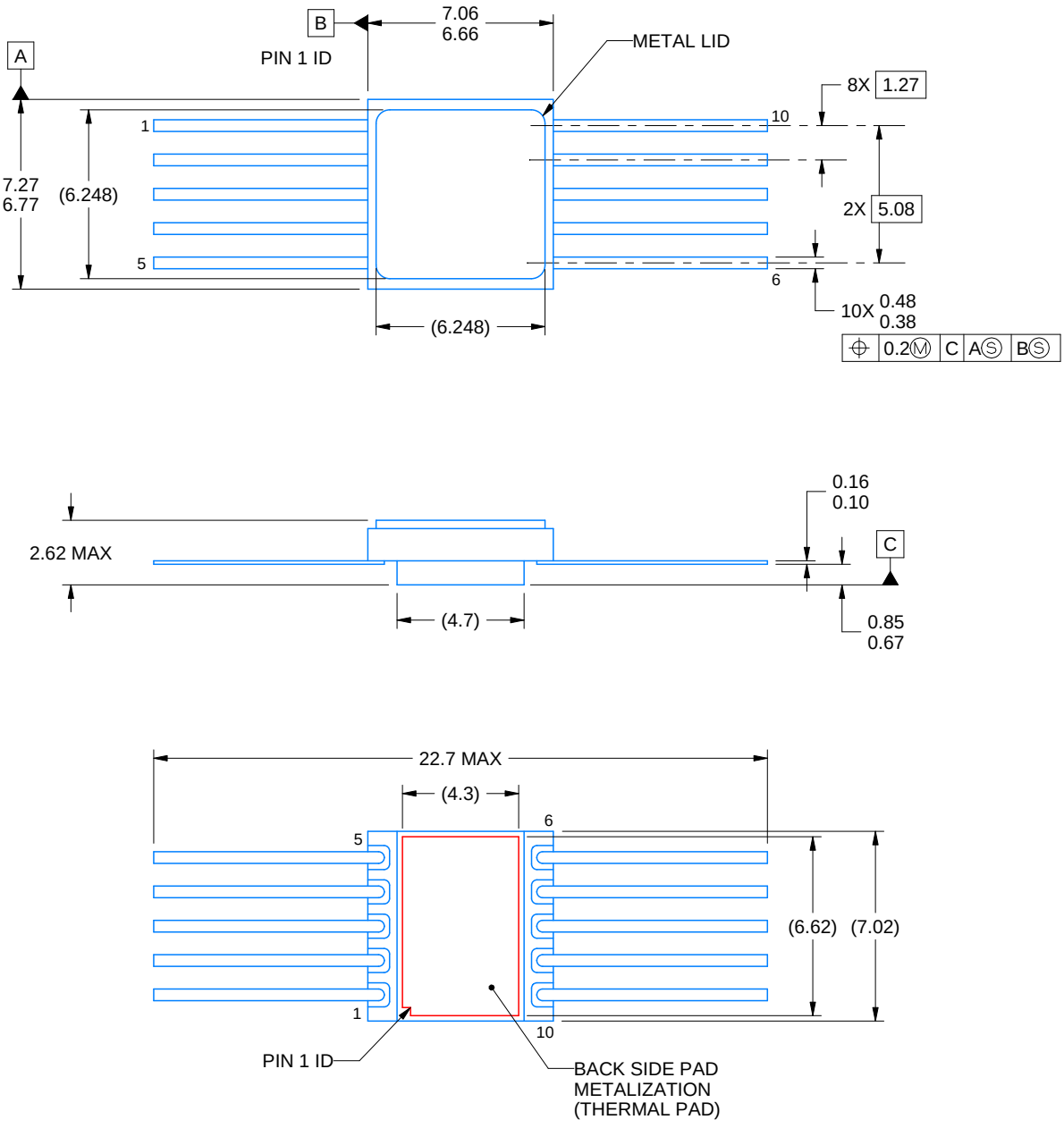
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1222402VHA	U	CFP	10	25	506.98	26.16	6220	NA
5962R1222403VXC	HKU	CFP	10	25	506.98	26.16	6220	NA
TPS7A4501HKU/EM	HKU	CFP	10	25	506.98	26.16	6220	NA
TPS7A4501U/EM	U	CFP	10	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

HKU0010A

CFP - 2.63mm max height

CERAMIC DUAL FLATPACK



4226200/A 09/2020

NOTES:

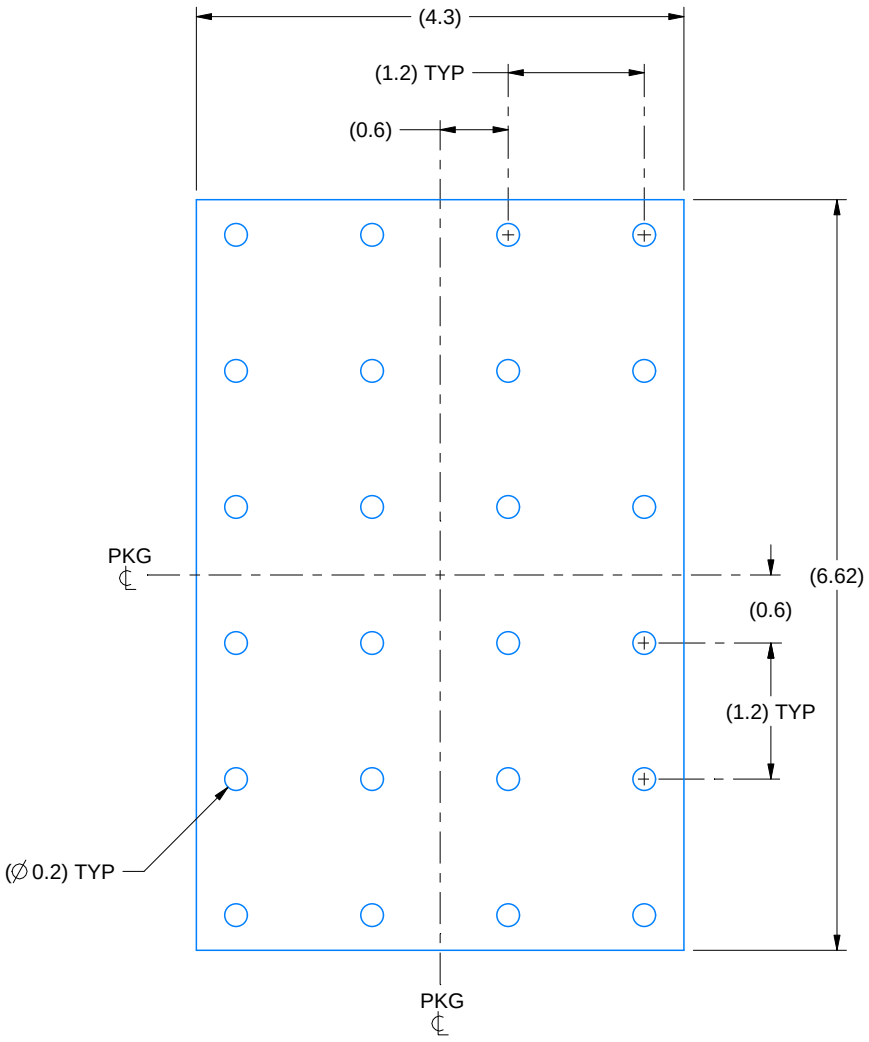
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The terminals are gold plated.
5. This drawing does not comply with MIL STD 1835. Do not use this package for compliant product.
6. Metal lid is connected to back side pad metalization.

EXAMPLE BOARD LAYOUT

HKU0010A

CFP - 2.63mm max height

CERAMIC DUAL FLATPACK



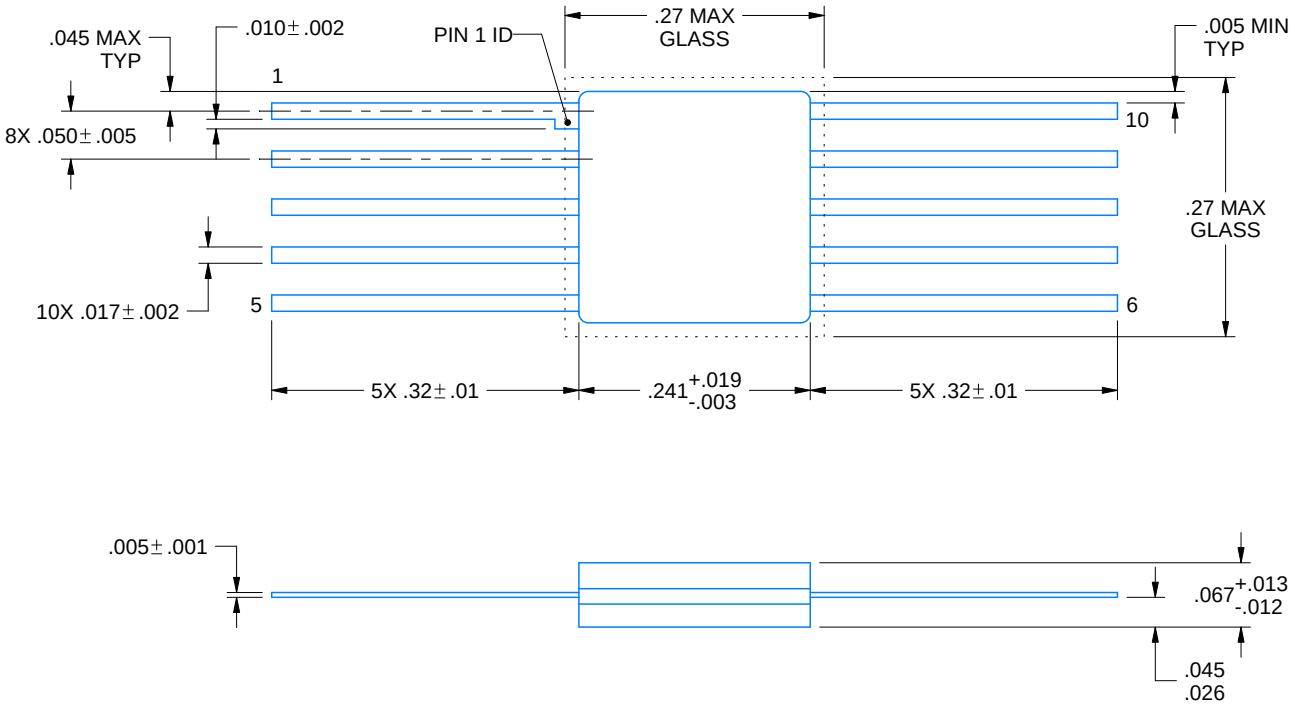
HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

U0010A

PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK



4225582/A 01/2020

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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