Test Report: PMP41150

1000W, 48V Switched Capacitor Converter Reference Design

Description

This reference design utilizes an inductor-less switch capacitor convert topology for both high-power-density and a compact power stage (70mm × 55mm × 2.85mm). A simple control scheme utilizing a TLC555-Q1 timer enables a fixed conversion ratio output with either 4:1 or 3:1 conversion ratio and can be set for different power distribution requirements. For 4:1 conversion ratio, the full load efficiency is at 96.7% while the peak efficiency is at 98.5% (I_{out} = 30A). For 3:1 conversion ratio, the full load efficiency is at 97.6% while the peak efficiency is at 98.7% (I_{out} = 25A).

Features

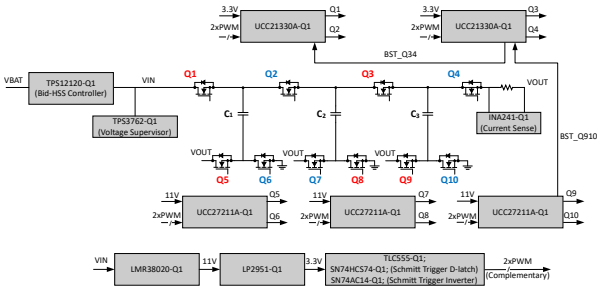
- High-power-density switched capacitor converter
- High-efficiency
- Simple open-loop control
- Self-variable frequency to improve light load efficiency
- Small form factor; power stage size at 70mm × 55mm × 2.85mm
- Configurable conversion ratio; either 4:1 or 3:1

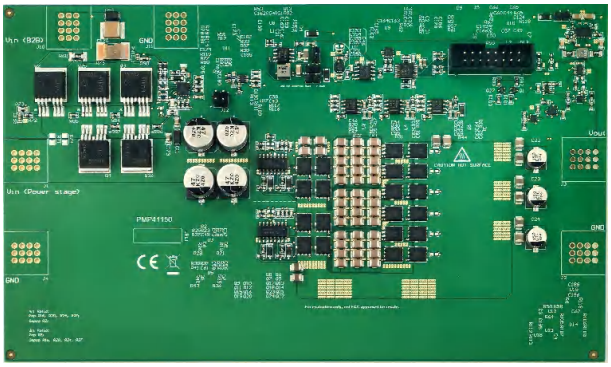
Applications

- 12V-48V power distribution box
- Zone control module

Resources

PMP41150	Design Folder
UCC21330-Q1	Product Folder
UCC27211A-Q1	Product Folder
TPS1212-Q1	Product Folder





1 System Description

With the emergence of the 48V low voltage power net in battery electric vehicles (48V white paper: 48V Automotive Systems: Why Now?), a closer examination of the overall low-voltage system is underway. The shift from 12V to 48V does transition most of the high power (≥60W) low voltage loads to the 48V rail; however, 12V legacy loads still remain. When implementing a 48V low voltage rail in a zone architecture, each zone control module needs 500W to 1000W for the 12V loads for power switches and motor drives, as shown in Figure 1-1. And this power requirement still demands high-performance converters that address efficiency and power density challenges, as the efficiency and power density have a major impact in the total footprint and heat loss of the zonal control modules. Smaller footprints and less thermal dissipation help save cost in the board manufacturing as well as the mechanical and cooling design of the module. In addition to the cost aspect, higher efficiency and lighter total weight can also help extend the range of a battery electric vehicle, which is yet another critical parameter from user perspective.

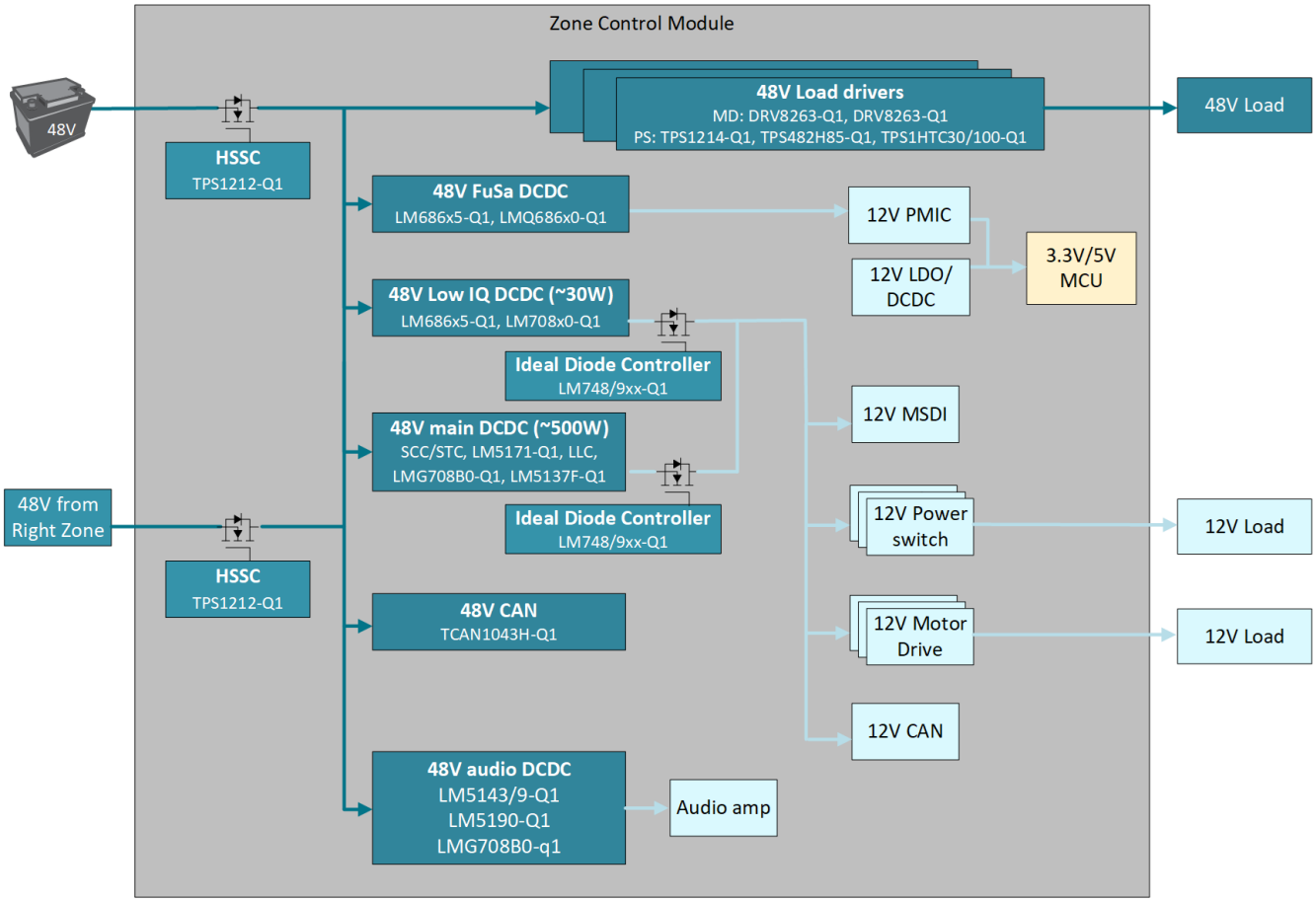


Figure 1-1. Typical Power Tree for 48V Zonal Architecture

The reference design describes a Switched Capacitor Converter (SCC) that can be used in 48V zonal control modules (*TIDA-020094 reference design*). The converter operates over a wide range of 36V to 52V (absolute max at 70V) to deliver either 4:1 or 3:1 conversion ratio for different choices of output rails. The converter can achieve as high as 96.7% and 97.6% full-load (960W) efficiency under 4:1 and 3:1 conversion ratio, respectively. The switched capacitor converter power stage size is only 70mm × 55mm × 2.85mm providing a smaller design size compared to other high power DC-DC topologies that require an inductor. In addition, 48V zonal control module often requires bidirectional power flow to encounter system challenges in jump-start by external 12V battery and collecting back EMF from high-power inductive loads. The SCC topology is bi-directional by design and supports these system challenges.

The reference design uses TLC555-Q1 to generate a PWM control signal, where the switching frequency is able to adjust based on the output load. At lighter load, the switching frequency is decreased to about 140kHz

to reduce gate drive loss and switching loss. The flying capacitors (C1, C2 and C3 in Figure 2-1) can utilize the parasitic inductance and produce resonance current waveform, enabling soft switching for higher efficiency. Therefore, at higher load the switching frequency is increased to resonance (about 300kHz) where switching loss can be even lower.

1.1 Key System Specifications

Table 1-1. Key System Specifications

Parameters	Test Condition	Min	Nom	Max	Unit
INPUT CONDITIONS					
Input voltage	/	36	48	52 (absmax70)	Volt
Input current	/	/	20	25	Ampere
OUTPUT CONDITIONS					
Output voltage	3:1 conversion ratio	12	16	17.33	Volt
	4:1 conversion ratio	9	12	13	Volt
Output current	3:1 conversion ratio	/	/	65	Ampere
	4:1 conversion ratio	/	/	80	Ampere
Output voltage ripple	3:1 conversion ratio	/	/	270	millivolt
	4:1 conversion ratio	/	/	250	millivolt
Output power	/	/	960	2000 (transient, 2s)	Watt
SYSTEM CHARACTERISTICS					
Efficiency% (power stage only; bias is not included)	3:1 conversion ratio; V_{in} = 48V, V_{out} = 15.81V, I_{out} = 25A (max efficiency)		98.69		%
	3:1 conversion ratio; V_{in} = 48V, V_{out} = 15.77V, I_{out} = 30A (half load)		98.62		%
	3:1 conversion ratio; V_{in} = 48V, V_{out} = 15.51V, I_{out} = 60A (full load)		97.56		%
	4:1 conversion ratio; V_{in} = 48V, V_{out} = 11.84V, I_{out} = 30A (max efficiency)		98.54		%
	4:1 conversion ratio; V_{in} = 48V, V_{out} = 11.78V, I_{out} = 40A (half load)		98.33		%
	4:1 conversion ratio; V_{in} = 48V, V_{out} = 11.52V, I_{out} = 80A (full load)		96.68		%
Operating ambient		-40	25	105	Deg C
Switching frequency	/	140	/	320	kHz
Load transient	3:1 conversion ratio; 0A to 60A; dI/dt = 0.1A/us	-3.13		1.56	%
	4:1 conversion ratio 0A to 80A; dI/dt = 0.1A/us	-2.78		2.08	%

2 System Overview

This section shows the block diagram of this switched capacitor converter design.

2.1 Block Diagram

Figure 2-1 shows the high-level block diagram of this reference design. TPS12120-Q1 is used for capacitive charging for soft-start considerations. UCC21330A-Q1 and UCC27211A-Q1 are used for the main power stage MOSFETs gate drive control. LMR38020-Q1 and LP2951-Q1 are used for the gate drive bias supply as well as discrete logic supply. TPS3762-Q1 and INA241-Q1 are used for voltage and current sensing of the system. Finally TLC555-Q1, Sn74HCS74-Q1 and SN74AC14-Q1 are used to generate complementary PWM signal with deadband.

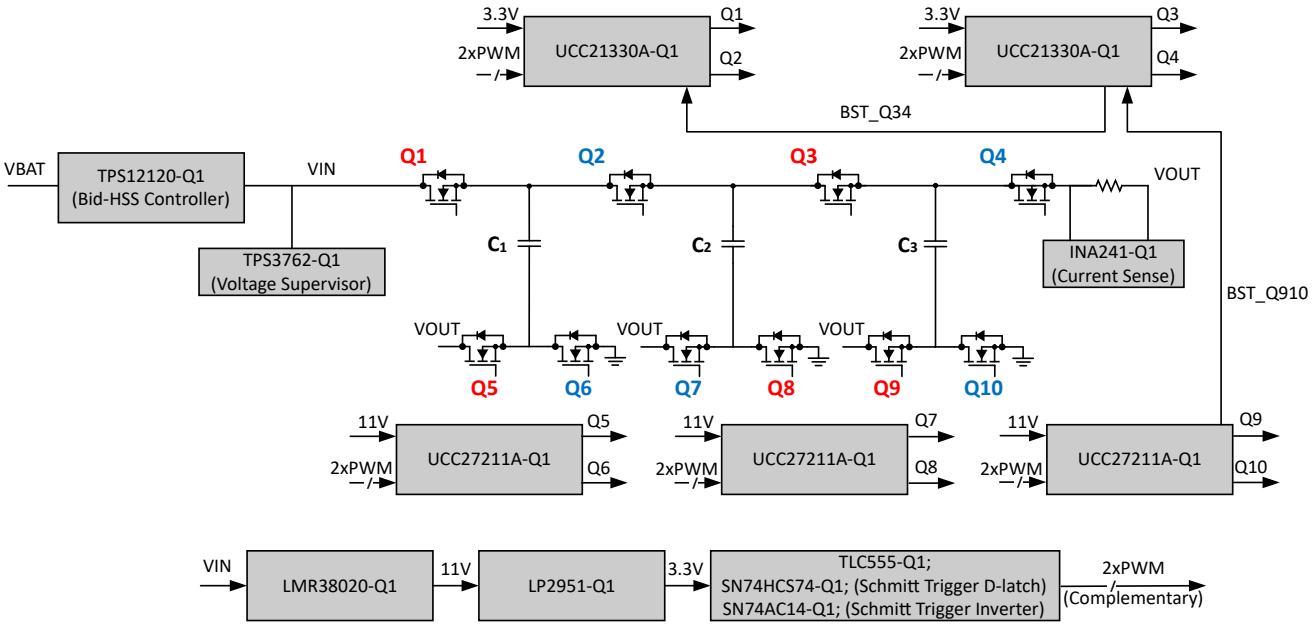


Figure 2-1. Block Diagram

2.2 Design Considerations

2.2.1 High Side Gate Drive Circuit

In this reference design, Q5 to Q10 can be regarded as three half-bridges with the low-side FET ground referenced; hence gate driving is much more straight forward and can be done with half-bridge gate driver like UCC27211A-Q1 used in the system.

However, Q1, Q2, Q3, and Q4 in the circuit need special gate drive strategy, since the source of these four switches is not ground-referenced. Therefore, an isolated dual-channel gate driver UCC21330A-Q1 is used to drive these four switches.

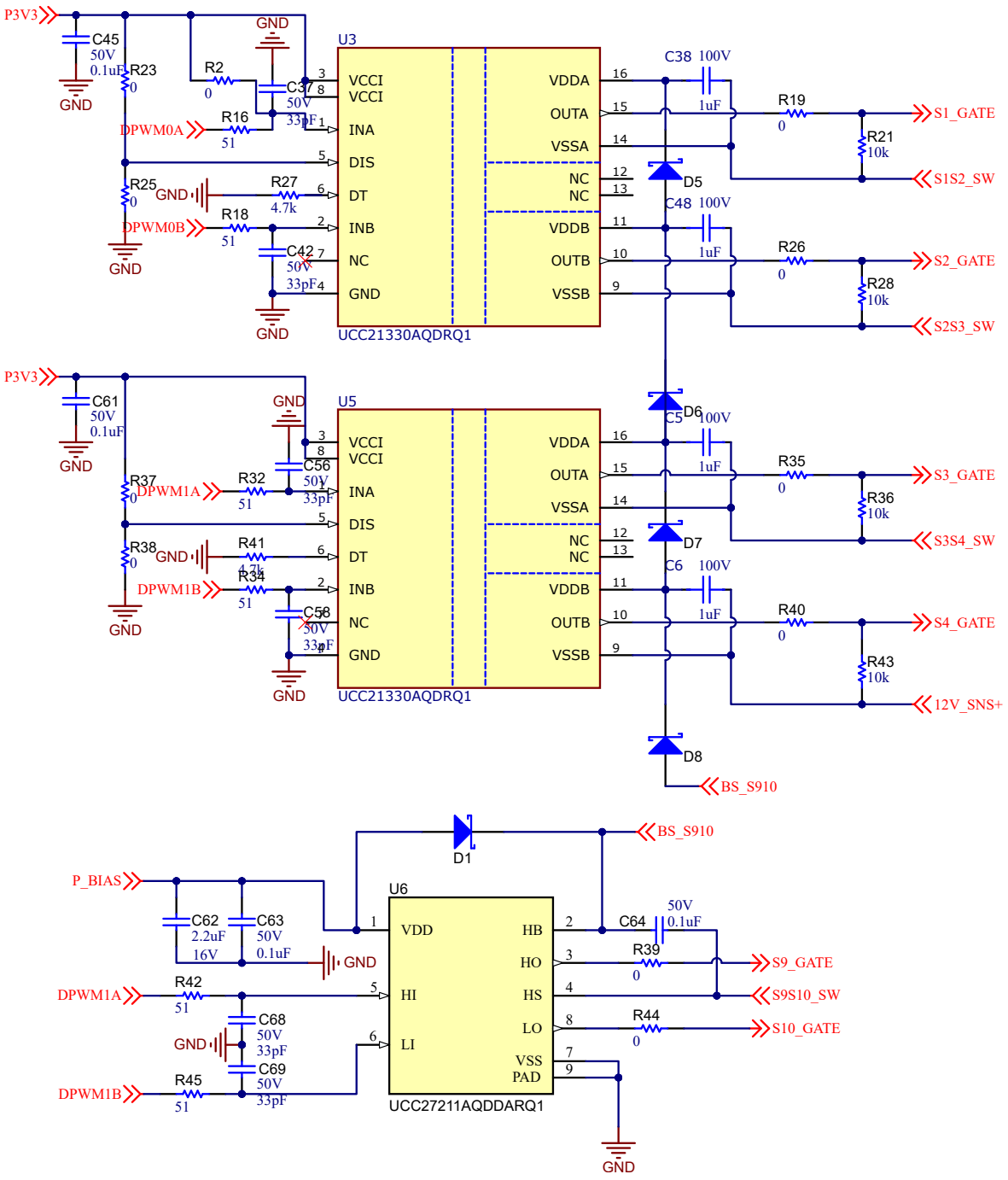


Figure 2-2. High Side Gate Drive Circuit

In addition, a cascaded bootstrap circuit is needed. D8, D7, D6 and D5 are used to provide stable gate drive bias voltage for driving Q1, Q2, Q3 and Q4. To encounter the voltage drop in diode along the cascaded bootstrap path, UCC21330A-Q1 is selected due to having the lowest UVLO voltage at 5V compared to other versions in UCC21330-Q1 family.

An optional diode D1 is also added in parallel to the internal diode within UCC27211-Q1. Due to the high switching frequency and the number of high side MOSFETs, the current stress of internal bootstrap diode is higher than the usual use case. An additional parallel diode can help with the resulting increased voltage drop.

2.2.2 PWM Generation Circuit

In this reference design, TLC555-Q1 is used to generate a pair of complementary PWM signal, of which the switching frequency can be self-adjustable. At lighter load the switching frequency is decreased to about 140kHz to reduce gate drive loss and switching loss, and at higher load the switching frequency is increased to resonance (about 300kHz) where switching loss can be even lower.

The output current of the SCC power stage is first sensed by the bidirectional current sense INA241-Q1 (not shown in Figure 2-3). Then the rail-to-rail amplifier TLV6001-Q1 creates an output voltage:

V_{amp} = 3.3V – I_LV_SNS (1)

Since for PNP transistor $V_e - V_b$ = 0.6V, two equations for the PNP transistor Q1 on the left can be derived to associate the amplifier output with the bias current I_{ec}:

3.3V – 680Ω × I_{ec} = V_e (2)

(V_e – 0.6V) – 1kΩ × I_{ec} = V_{amp} (3)

Then the following equation can be derived:

V_{amp} = 2.7V – 1.68kΩ × I_{ec} (4)

Further combining with (1), the final relationship of I_LV_SNS and I_{ec} are:

I_LV_SNS = 0.6V + 1.68kΩ × I_{ec} (5)

(5) demonstrates that the higher the output current, the higher the bias current injecting into the charging and discharging circuit of TLC555-Q1 is, and hence higher output frequency.

Also note that due to the nature of the astable operation of TLC555-Q1, the duty ratio of the PWM output of TLC555-Q1 here is not 50%. Therefore, the current mirror section of this circuit is deliberately set to be twice the desired frequency (280kHz to 640kHz), and a following frequency divider by two using the D-latch can reduce the frequency by half (down to 140kHz to 320kHz) and also reset the duty ratio to 50%.

For further information on the astable operation of TLC555-Q1, read the datasheet for more detailed discussions.

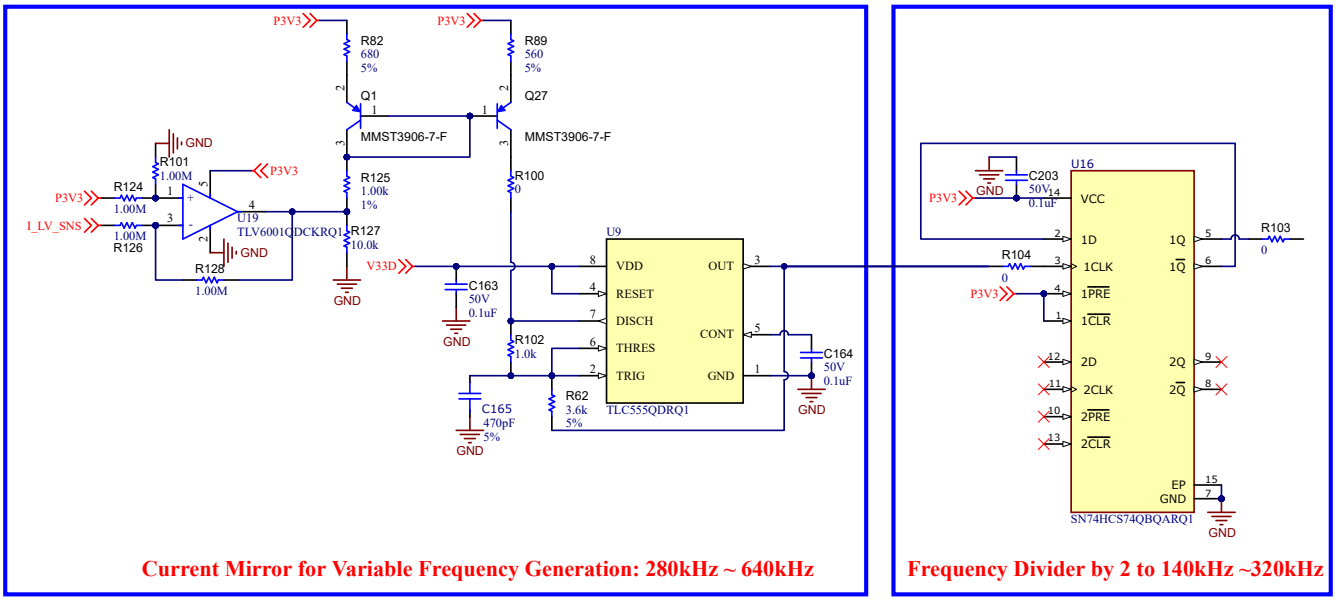


Figure 2-3. PWM Generation Circuit

2.3 Highlighted Products

2.3.1 UCC21330-Q1 Overview

The UCC21330-Q1 is an isolated dual channel gate driver family with programmable dead time and wide temperature range. The UCC21330-Q1 is designed with 4A peak-source and 6A peak-sink current to drive power MOSFET, SiC, GaN, and IGBT transistors.

The UCC21330-Q1 can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. The input side is isolated from the two output drivers by a 3kVRMS isolation barrier, with a minimum of 125V/ns common-mode transient immunity (CMTI).

Protection features include: resistor programmable dead time, disable feature to shut down both outputs simultaneously, and integrated de-glitch filter that rejects input transients shorter than 5ns. All supplies have UVLO protection.

Features:

- Universal: dual low-side, dual high-side or half bridge driver
- AEC-Q100 qualified with the following results
- Device temperature grade 1
- Junction temperature range –40 to +150°C
- Up to 4A peak source and 6A peak sink output
- Common-mode transient immunity (CMTI) greater than 125V/ns
- Up to 25V VDD output drive supply
- 5V, 8V, 12V VDD UVLO options
- Switching parameters:
- 33ns typical propagation delay
- 5ns maximum pulse-width distortion
- 10µs maximum VDD power-up delay
- UVLO protection for all power supplies
- Fast disable for power sequencing

2.3.2 UCC27211A-Q1 Overview

The UCC27211A-Q1 device driver is based on the popular UCC27201 MOSFET drivers; but, this device offers several significant performance improvements.

The peak output pullup and pulldown current has been increased to 3.7A source and 4.5A sink and thereby allows for driving large power MOSFETs with minimized switching losses during the transition through the Miller Plateau of the MOSFET. The input structure can directly handle –10VDC, which increases robustness and also allows direct interface to gate-drive transformers without using rectification diodes. The inputs are also independent of supply voltage and have a 20V maximum rating.

The switching node of the UCC27211A-Q1 (HS pin) can handle –(24 - VDD) V maximum, which allows the high-side channel to be protected from inherent negative voltages caused by parasitic inductance and stray capacitance. The UCC27211A-Q1 (TTL inputs) has increased hysteresis that allows for interface to analog or digital PWM controllers with enhanced noise immunity.

The low-side and high-side gate drivers are independently controlled and matched to 4ns between the turn on and turn off of each other. An on-chip 120V rated bootstrap diode eliminates the external discrete diodes. Undervoltage lockout is provided for both the high-side and the low-side drivers which provides symmetric turn on and turn off behavior and forces the outputs low if the drive voltage is below the specified threshold.

Features:

- AEC-Q100 Qualified for Automotive Applications: Device Temperature Grade 1
- –40°C to +150°C junction temperature range
- Drives two N-channel MOSFETs in high-side and low-side configuration with independent inputs
- Maximum boot voltage 120V DC × 3.7A source, 4.5A sink output currents
- Input pins can tolerate –10V to +20V and are independent of supply voltage range
- TTL compatible inputs
- 8V to 17V VDD operating range, (20V ABS MAX)
- 7.2ns rise and 5.5ns fall time with 1000pF load
- Fast propagation delay times (20ns typical)
- 4ns delay matching
- Symmetrical undervoltage lockout for high-side and low-side driver
- Available in the industry standard SO-PowerPAD SOIC-8 package

2.3.3 TPS1212-Q1 Overview

TPS1212-Q1 is a family of low IQ smart high side drivers with protection and diagnostics. With wide operating voltage range of 3.5V to 73V (74V absmax), the device is designed for 12V, 24V, and 48V automotive system designs.

The devices have two integrated gate drives with 0.5A/2A (GATE) and 100µA/0.39A (G). With LPM low, the low power path is kept ON and the main FETs are turned OFF with IQ of 20µA (typ). The auto load wakeup threshold is adjusted using RBYPASS resistor placed across DRN and CS2–. IQ reduces to 1µA (typ) with EN/UVLO low.

The device has accurate bi-directional current sensing (±2%) output (IMON) with adjustable I2t based overcurrent and short circuit protection using an external RSNS resistor and FLT indication. Auto-retry and latch-off fault behavior can be configured. The device also has NTC based temperature sensing (TMP) and monitoring output (ITMPO) output for overtemperature detection of external FETs.

The TPS1212-Q1 is available in 23-pin VQFN package.

Features:

- AEC-Q100 automotive qualified for grade 1 temperature
- Functional Safety-Capable
- Documentation available to aid functional safety system design
- 3.5V to 73V input range (74V absolute maximum)
- Reverse input and output protection down to –65V
- Integrated 12V charge pump
- Low IQ = 20µA in low power mode (LPM = Low)

- Low 1µA shutdown current (EN/UVLO = Low)
- Dual gate drive: GATE: 0.5A src/2A sink, G: 100µA src/0.39A sink
- Accurate I2t overcurrent protection (IOC) with adjustable circuit breaker timer (I2t)
- Accurate and fast (5µs) short-circuit protection
- Fast transition (5µs) from low power mode to active mode using adjustable load wakeup threshold or LPM trigger with WAKE indication
- Accurate analog bi-directional current monitor output (IMON, I_DIR): ±2% at 30mV VSNS
- NTC based overtemperature sensing (TMP) and monitoring output (ITMPO)
- Fault indication (FLT) during short circuit fault, I2t, charge pump UVLO, overtemperature
- TPS12120-Q1 (I2t enabled), TPS12121-Q1 (I2t disabled)
- Accurate (±2%) and adjustable undervoltage lockout (UVLO)

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The following hardware is required for this reference design:

- PMP41150 board

The following test equipment is needed to power and evaluate the DUT:

- DC Source: Chroma 62012P-100-50;
- DC Load: Chroma 6312A+63103A
- Multimeter: Fluke 287C
- Oscilloscope: Tektronix DPO3054
- Electrical thermography: Fluke TiS55

A heatsink is used at the bottom side of the board. The dimension of the heatsink is shown in Figure 3-1. The groove in the heat sink is designed so that the height of the capacitors does't interfere with the installation.

Thermal interface material (TIM) needs to be applied in between the aluminum heatsink and the exposed copper plane to maintain proper contact between surfaces and also avoid direct short across different power nets.

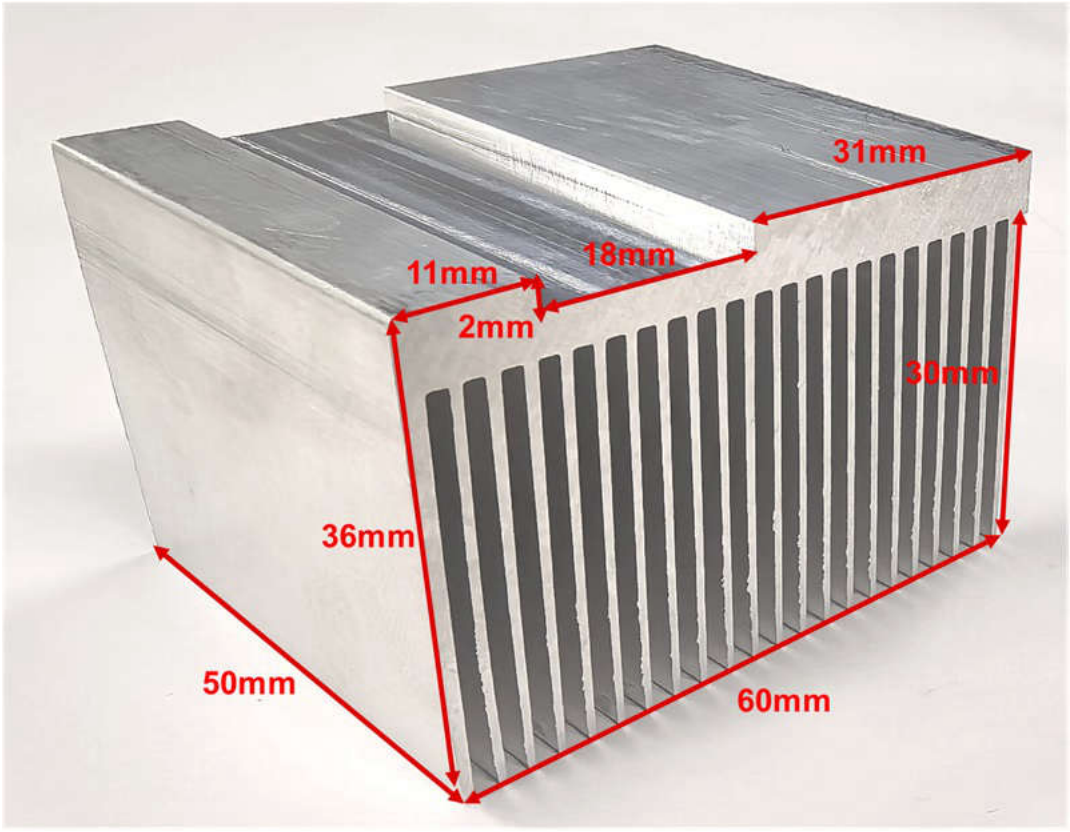


Figure 3-1. Dimension of the Heatsink

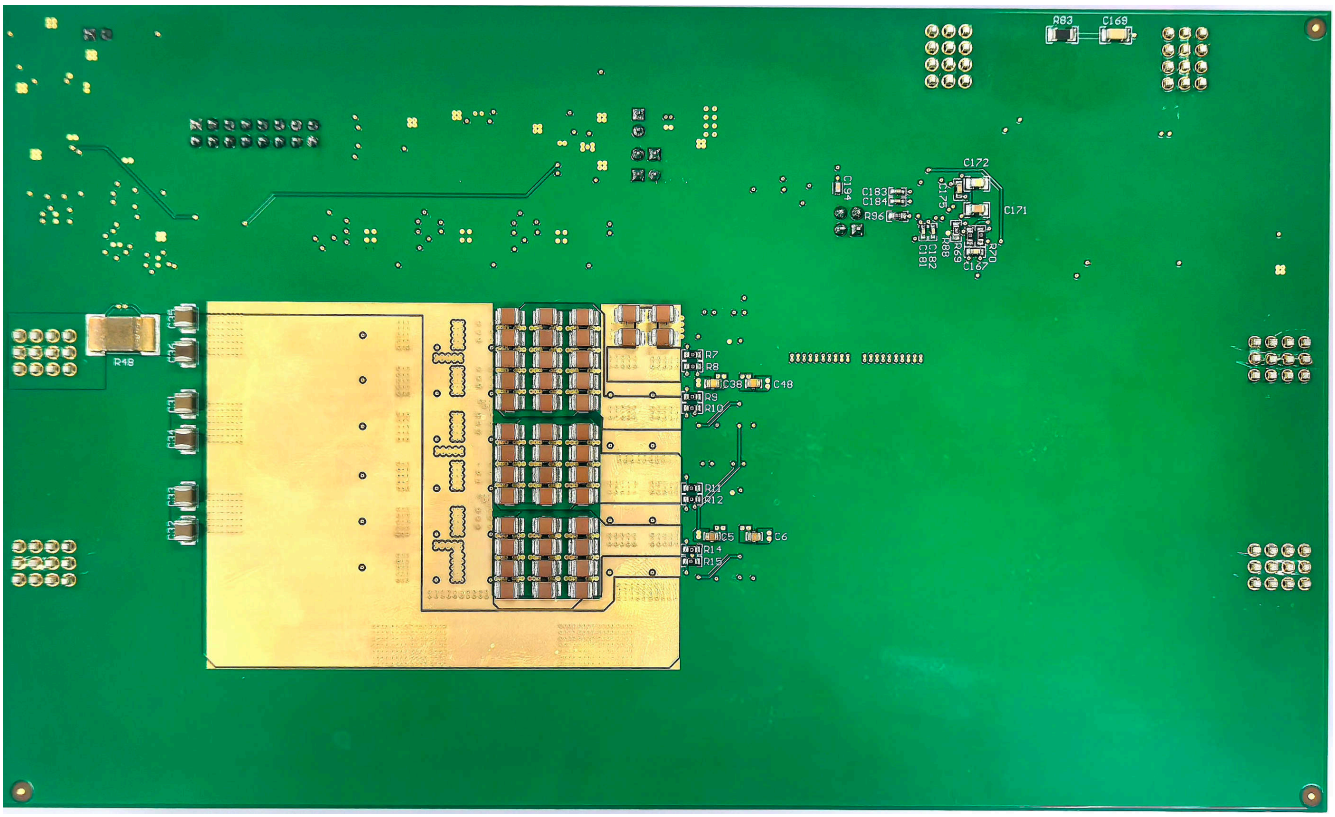


Figure 3-2. Bottom Side of PMP41150

3.2 Test Setup

- 1.2kW DC power supply: 48V, 25A
- 2.5kW electronic load: 60A / 80A (depending on the output conversion ratio; 3:1 and 4:1 respectively here)
- Oscilloscope with passive probes for voltage and current

3.3 Test Results

3.3.1 Efficiency Data

Efficiency data is shown in Table 3-1. Test condition is room temperature, no air flow. Note that the power stage efficiency is calculated with the bias power excluded, while the overall efficiency is calculated with the bias power included.

Table 3-1. Efficiency at 36V_{in}, Conversion Ratio = 4:1

V_{bias}	I_{bias}	V_{in}	I_{in}	V_{out}	I_{out}	P_{in}	P_{bias}	P_{out}	P_{loss}	Overall Efficiency	Power Stage Efficiency
10.89	0.21	36.00	0.048	8.994	0.000	1.74	2.29	0.00	1.74	0.00%	0.00%
10.89	0.21	36.00	0.301	8.988	1.006	10.84	2.29	9.04	1.79	70.24%	80.90%
10.89	0.21	36.00	0.549	8.982	2.006	19.77	2.29	18.02	1.75	82.44%	89.46%
10.89	0.21	35.99	0.798	8.976	3.006	28.72	2.29	26.98	1.74	87.62%	92.82%
10.89	0.21	35.99	1.053	8.970	4.030	37.91	2.29	36.15	1.76	90.64%	94.75%
10.89	0.21	35.99	1.302	8.964	5.031	46.86	2.29	45.10	1.76	92.23%	95.66%
10.89	0.21	35.99	1.550	8.958	6.019	55.78	2.29	53.92	1.87	93.29%	96.21%
10.89	0.21	35.99	1.798	8.952	7.019	64.72	2.29	62.83	1.89	94.07%	96.64%
10.89	0.21	35.99	2.047	8.945	8.017	73.67	2.29	71.71	1.96	94.76%	97.04%
10.89	0.21	35.99	2.294	8.939	9.016	82.58	2.29	80.59	1.98	95.31%	97.37%
10.96	0.22	35.99	2.549	8.935	10.040	91.73	2.41	89.71	2.03	95.69%	97.57%
10.96	0.23	36.00	3.787	8.910	15.028	136.31	2.52	133.90	2.41	96.95%	98.27%
10.96	0.23	36.00	5.032	8.883	20.046	181.13	2.52	178.07	3.07	97.46%	98.49%
10.95	0.24	36.00	6.276	8.853	25.062	225.92	2.63	221.87	4.05	97.67%	98.50%
10.95	0.24	36.00	7.520	8.823	30.087	270.73	2.63	265.46	5.28	97.83%	98.54%
10.95	0.24	36.00	8.764	8.791	35.106	315.51	2.63	308.62	6.90	97.83%	98.45%
10.95	0.25	36.00	10.000	8.759	40.096	360.00	2.74	351.20	8.80	97.78%	98.33%
10.95	0.25	36.00	11.243	8.724	45.112	404.75	2.74	393.56	11.19	97.70%	98.19%
10.95	0.25	36.00	12.487	8.722	50.131	449.53	2.74	437.24	12.29	97.56%	98.00%
10.95	0.25	36.00	13.732	8.720	55.153	494.35	2.74	480.93	13.42	97.42%	97.82%
10.95	0.25	36.00	14.974	8.694	60.168	539.06	2.74	523.10	15.96	97.27%	97.63%
10.95	0.25	36.00	16.217	8.680	65.187	583.81	2.74	565.82	17.99	97.10%	97.43%
10.95	0.25	36.00	17.456	8.663	70.178	628.42	2.74	607.95	20.46	96.32%	96.74%
10.95	0.25	36.00	18.697	8.635	75.196	673.09	2.74	649.32	23.77	96.08%	96.47%
10.82	0.22	36.00	19.934	8.579	80.215	717.62	2.38	688.16	29.46	95.58%	95.89%

Table 3-2. Efficiency at 48V_{in}, Conversion Ratio = 4:1

V_{bias}	I_{bias}	V_{in}	I_{in}	V_{out}	I_{out}	P_{in}	P_{bias}	P_{out}	P_{loss}	Overall Efficiency	Power Stage Efficiency
10.93	0.21	48.02	0.059	12.002	0.00	2.83	2.27	0.00	2.83	0.00%	0.00%
10.93	0.21	48.02	0.312	12	1.01	14.98	2.27	12.12	2.86	70.24%	80.90%
10.93	0.21	48.02	0.561	11.99	2.01	26.94	2.30	24.10	2.84	82.44%	89.46%
10.93	0.21	48.02	0.809	11.98	3.01	38.85	2.31	36.06	2.79	87.62%	92.82%
10.93	0.21	48.01	1.064	11.98	4.04	51.08	2.32	48.40	2.68	90.64%	94.75%
10.93	0.21	48.01	1.311	11.97	5.03	62.94	2.34	60.21	2.73	92.23%	95.66%
10.93	0.22	48.01	1.56	11.97	6.02	74.90	2.35	72.06	2.84	93.29%	96.21%
10.93	0.22	48.01	1.809	11.96	7.02	86.85	2.37	83.94	2.91	94.07%	96.64%

Table 3-2. Efficiency at $48V_{in}$, Conversion Ratio = 4:1 (continued)

V_{bias}	I_{bias}	V_{in}	I_{in}	V_{out}	I_{out}	P_{in}	P_{bias}	P_{out}	P_{loss}	Overall Efficiency	Power Stage Efficiency
10.93	0.22	48.01	2.056	11.95	8.02	98.71	2.38	95.79	2.92	94.76%	97.04%
10.93	0.22	48.01	2.304	11.95	9.01	110.62	2.39	107.71	2.91	95.31%	97.37%
10.93	0.22	48.01	2.559	11.94	10.04	122.86	2.42	119.88	2.98	95.69%	97.57%
10.93	0.23	48	3.798	11.92	15.03	182.30	2.48	179.16	3.15	96.95%	98.27%
10.92	0.23	47.99	5.044	11.89	20.05	242.06	2.53	238.39	3.67	97.46%	98.49%
10.92	0.24	47.99	6.289	11.86	25.07	301.81	2.59	297.29	4.51	97.67%	98.50%
10.92	0.24	47.98	7.535	11.84	30.09	361.53	2.62	356.27	5.26	97.83%	98.54%
10.92	0.24	47.97	8.78	11.81	35.11	421.18	2.65	414.64	6.54	97.83%	98.45%
10.92	0.25	47.96	10.017	11.78	40.10	480.42	2.68	472.38	8.04	97.78%	98.33%
10.92	0.25	47.95	11.261	11.75	45.12	539.96	2.68	530.17	9.79	97.70%	98.19%
10.92	0.25	47.95	12.505	11.72	50.14	599.61	2.70	587.61	12.01	97.56%	98.00%
10.92	0.25	47.94	13.75	11.69	55.16	659.18	2.71	644.80	14.38	97.42%	97.82%
10.92	0.25	47.93	14.994	11.66	60.18	718.66	2.70	701.66	17.00	97.27%	97.63%
10.92	0.25	47.92	16.239	11.63	65.19	778.17	2.70	758.19	19.98	97.10%	97.43%
10.92	0.25	47.91	17.474	11.6	70.18	837.18	2.68	814.13	23.04	96.94%	97.25%
10.92	0.24	47.9	18.717	11.57	75.20	896.54	2.64	870.10	26.45	96.77%	97.05%
10.93	0.24	47.89	19.96	11.52	80.22	955.88	2.60	924.13	31.75	96.42%	96.68%

Table 3-3. Efficiency at $52V_{in}$, Conversion Ratio = 4:1

V_{bias}	I_{bias}	V_{in}	I_{in}	V_{out}	I_{out}	P_{in}	P_{bias}	P_{out}	P_{loss}	Overall Efficiency	Power Stage Efficiency
10.83	0.21	52.00	0.0633	12.999	0.000	3.29	2.27	0.00	3.29	0.00%	0.00%
10.83	0.21	52.00	0.3153	12.991	1.009	16.40	2.27	13.11	3.28	70.23%	79.97%
10.83	0.21	51.99	0.564	12.983	2.009	29.32	2.27	26.09	3.24	82.56%	88.97%
10.83	0.22	51.99	0.8126	12.975	3.009	42.25	2.38	39.05	3.20	87.49%	92.42%
10.83	0.22	51.99	1.0681	12.968	4.034	55.53	2.38	52.32	3.21	90.34%	94.21%
10.83	0.22	51.99	1.3166	12.96	5.023	68.45	2.38	65.10	3.35	91.91%	95.11%
10.83	0.22	51.99	1.5651	12.953	6.016	81.37	2.38	77.92	3.45	93.04%	95.76%
10.83	0.22	51.99	1.8138	12.946	7.016	94.30	2.38	90.82	3.48	93.94%	96.31%
10.83	0.22	51.99	2.062	12.939	8.013	107.20	2.38	103.67	3.53	94.61%	96.71%
10.83	0.22	51.99	2.3101	12.933	9.009	120.10	2.38	116.52	3.58	95.13%	97.02%
10.83	0.22	51.99	2.5651	12.926	10.037	133.36	2.38	129.74	3.62	95.58%	97.28%
10.82	0.23	52.00	3.804	12.9	15.028	197.81	2.49	193.86	3.95	96.79%	98.00%
10.81	0.24	52.00	5.05	12.873	20.046	262.60	2.59	258.05	4.55	97.31%	98.27%
10.81	0.24	52.00	6.295	12.845	25.062	327.34	2.59	321.92	5.42	97.57%	98.34%
10.80	0.25	52.00	7.5403	12.818	30.087	392.10	2.70	385.66	6.44	97.69%	98.36%
10.80	0.25	52.00	8.7846	12.791	35.106	456.80	2.70	449.04	7.76	97.72%	98.30%
10.80	0.25	52.00	10.021	12.764	40.096	521.09	2.70	511.79	9.31	97.71%	98.21%
10.80	0.25	52.00	11.265	12.735	45.117	585.78	2.70	574.56	11.22	97.64%	98.09%
10.80	0.25	52.00	12.509	12.709	50.134	650.47	2.70	637.15	13.31	97.55%	97.95%
10.80	0.25	52.00	13.752	12.677	55.153	715.10	2.70	699.17	15.93	97.40%	97.77%
10.79	0.26	52.00	14.994	12.647	60.171	779.69	2.81	760.98	18.71	97.25%	97.60%
10.79	0.26	52.00	16.237	12.607	65.187	844.32	2.81	821.81	22.51	97.01%	97.33%
10.79	0.26	52.00	17.474	12.572	70.178	908.65	2.81	882.28	26.37	96.80%	97.10%
10.81	0.24	52.00	18.716	12.556	75.198	973.23	2.59	944.19	29.05	96.76%	97.02%
10.84	0.21	52.00	19.949	12.405	80.218	1037.35	2.28	995.10	42.24	95.72%	95.93%

Table 3-4. Efficiency at 36Vin, Conversion Ratio = 3:1

V_{bias}	I_{bias}	V_{in}	I_{in}	V_{out}	I_{out}	P_{in}	P_{bias}	P_{out}	P_{loss}	Overall Efficiency	Power Stage Efficiency
10.79	0.16	36.00	0.05	11.999	0.000	1.80	1.73	0.00	1.80	0.00%	0.00%
10.79	0.16	35.99	0.3858	11.991	1.009	13.88	1.73	12.10	1.78	77.52%	87.16%
10.79	0.16	35.99	0.7173	11.982	2.006	25.82	1.73	24.04	1.78	87.28%	93.12%
10.79	0.17	35.99	1.0483	11.974	3.006	37.73	1.83	36.00	1.73	90.99%	95.41%
10.79	0.17	35.99	1.389	11.966	4.034	49.99	1.83	48.27	1.72	93.15%	96.57%
10.79	0.17	35.99	1.7196	11.958	5.025	61.89	1.83	60.09	1.80	94.30%	97.09%
10.79	0.17	35.99	2.0511	11.951	6.019	73.82	1.83	71.93	1.89	95.08%	97.44%
10.79	0.17	35.99	2.3813	11.943	7.016	85.70	1.83	83.79	1.92	95.72%	97.76%
10.79	0.17	36.00	2.7113	11.942	8.013	97.61	1.83	95.69	1.92	96.22%	98.03%
10.79	0.17	36.00	3.0422	11.934	9.009	109.52	1.83	107.52	2.00	96.56%	98.17%
10.79	0.17	36.00	3.3818	11.926	10.037	121.74	1.83	119.70	2.04	96.86%	98.32%
10.78	0.18	36.00	5.0325	11.893	15.025	181.17	1.94	178.69	2.48	97.59%	98.63%
10.78	0.18	36.00	6.6928	11.856	20.046	240.94	1.94	237.67	3.28	97.85%	98.64%
10.77	0.19	36.00	8.3524	11.823	25.062	300.69	2.05	296.31	4.38	97.88%	98.54%
10.77	0.19	36.00	10.012	11.789	30.086	360.43	2.05	354.68	5.75	97.85%	98.41%
10.77	0.19	36.00	11.671	11.755	35.106	420.16	2.05	412.67	7.48	97.74%	98.22%
10.77	0.19	36.00	13.318	11.721	40.096	479.45	2.05	469.97	9.48	97.61%	98.02%
10.77	0.19	36.00	14.977	11.683	45.114	539.17	2.05	527.07	12.11	97.39%	97.75%
10.78	0.20	36.00	16.636	11.640	50.134	598.90	2.16	583.56	15.34	97.09%	97.44%
10.78	0.20	36.00	18.294	11.602	55.153	658.58	2.16	639.89	18.70	96.84%	97.16%
10.78	0.20	36.00	19.951	11.561	60.167	718.24	2.16	695.59	22.65	96.56%	96.85%
10.78	0.20	36.00	21.609	11.513	65.187	777.92	2.16	750.50	27.43	96.21%	96.47%

Table 3-5. Efficiency at 48Vin, Conversion Ratio = 3:1

V_{bias}	I_{bias}	V_{in}	I_{in}	V_{out}	I_{out}	P_{in}	P_{bias}	P_{out}	P_{loss}	Overall Efficiency	Power Stage Efficiency
10.95	0.16	48.02	0.067	16	0.00	3.22	1.77	0.00	3.22	0.00%	0.00%
10.95	0.16	48.02	0.403	16	1.02	19.35	1.78	16.27	3.08	76.98%	84.08%
10.95	0.16	48.02	0.734	15.99	2.02	35.25	1.80	32.24	3.01	87.02%	91.46%
10.95	0.17	48.02	1.066	15.98	3.01	51.19	1.81	48.15	3.04	90.85%	94.06%
10.95	0.17	48.01	1.405	15.97	4.04	67.45	1.82	64.49	2.97	93.09%	95.60%
10.95	0.17	48.01	1.736	15.96	5.03	83.35	1.83	80.31	3.03	94.29%	96.36%
10.94	0.17	48.01	2.068	15.95	6.02	99.28	1.84	96.05	3.23	94.98%	96.74%
10.95	0.17	48.01	2.398	15.95	7.02	115.13	1.85	111.95	3.17	95.70%	97.24%
10.95	0.17	48.01	2.728	15.94	8.02	130.97	1.86	127.79	3.18	96.20%	97.57%
10.95	0.17	48.00	3.059	15.93	9.02	146.83	1.87	143.62	3.21	96.58%	97.82%
10.95	0.17	48.00	3.400	15.92	10.04	163.20	1.88	159.84	3.36	96.82%	97.94%
10.94	0.18	47.99	5.050	15.89	15.03	242.35	1.94	238.83	3.52	97.77%	98.55%
10.94	0.18	47.98	6.712	15.85	20.05	322.04	1.98	317.79	4.25	98.08%	98.68%
10.94	0.18	47.97	8.372	15.81	25.07	401.60	2.01	396.36	5.25	98.20%	98.69%
10.94	0.19	47.96	10.033	15.77	30.09	481.18	2.05	474.52	6.66	98.20%	98.62%
10.94	0.19	47.95	11.692	15.73	35.11	560.63	2.06	552.31	8.32	98.16%	98.52%
10.94	0.19	47.94	13.343	15.69	40.10	639.66	2.08	629.17	10.49	98.04%	98.36%
10.94	0.19	47.93	15.000	15.65	45.12	718.95	2.08	706.13	12.82	97.93%	98.22%
10.94	0.19	47.92	16.661	15.61	50.14	798.40	2.05	782.69	15.71	97.78%	98.03%
10.95	0.19	47.9	18.320	15.55	55.16	877.53	2.06	857.72	19.81	97.51%	97.74%
10.95	0.19	47.88	19.980	15.51	60.18	956.64	2.07	933.35	23.30	97.35%	97.56%

Table 3-5. Efficiency at 48Vin, Conversion Ratio = 3:1 (continued)

V_{bias}	I_{bias}	V_{in}	I_{in}	V_{out}	I_{out}	P_{in}	P_{bias}	P_{out}	P_{loss}	Overall Efficiency	Power Stage Efficiency
10.95	0.19	47.87	21.637	15.46	65.19	1035.76	2.06	1007.88	27.88	97.12%	97.31%

Table 3-6. Efficiency at 52V_{in}, Conversion Ratio = 3:1

V_{bias}	I_{bias}	V_{in}	I_{in}	V_{out}	I_{out}	P_{in}	P_{bias}	P_{out}	P_{loss}	Overall Efficiency	Power Stage Efficiency
10.84	0.17	52.00	0.0773	17.334	0.000	4.02	1.84	0.00	4.02	0.00%	0.00%
10.84	0.17	52.00	0.4141	17.323	1.016	21.53	1.84	17.59	3.94	75.26%	81.70%
10.84	0.17	51.99	0.7456	17.313	2.013	38.76	1.84	34.84	3.92	85.81%	89.88%
10.84	0.17	51.99	1.0774	17.303	3.009	56.01	1.84	52.07	3.94	90.00%	92.96%
10.84	0.17	51.99	1.4178	17.293	4.034	73.71	1.84	69.77	3.95	92.34%	94.65%
10.84	0.17	51.99	1.7494	17.283	5.029	90.95	1.84	86.92	4.03	93.67%	95.57%
10.84	0.17	51.99	2.0808	17.273	6.022	108.18	1.84	104.01	4.17	94.54%	96.15%
10.84	0.17	51.99	2.4113	17.263	7.019	125.36	1.84	121.16	4.20	95.25%	96.65%
10.82	0.18	52.00	2.7419	17.260	8.016	142.58	1.95	138.35	4.23	95.73%	97.03%
10.82	0.18	52.00	3.0726	17.251	9.013	159.78	1.95	155.47	4.30	96.14%	97.31%
10.82	0.18	52.00	3.4129	17.240	10.040	177.47	1.95	173.09	4.38	96.47%	97.53%
10.82	0.18	52.00	5.0651	17.201	15.030	263.39	1.95	258.53	4.85	97.44%	98.16%
10.82	0.18	52.00	6.7269	17.159	20.050	349.80	1.95	344.04	5.76	97.81%	98.35%
10.79	0.19	52.00	8.3868	17.119	25.067	436.11	2.05	429.12	6.99	97.94%	98.40%
10.79	0.19	52.00	10.048	17.083	30.089	522.50	2.05	514.01	8.49	97.99%	98.38%
10.79	0.19	52.00	11.708	17.044	35.109	608.82	2.05	598.40	10.42	97.96%	98.29%
10.79	0.20	52.00	13.356	17.005	40.100	694.51	2.16	681.90	12.61	97.88%	98.18%
10.79	0.20	52.00	15.015	16.960	45.118	780.78	2.16	765.20	15.58	97.73%	98.00%
10.79	0.20	52.00	16.675	16.918	50.137	867.10	2.16	848.22	18.88	97.58%	97.82%
10.79	0.20	52.00	18.332	16.906	55.156	953.26	2.16	932.47	20.80	97.60%	97.82%
10.70	0.21	52.00	19.988	16.872	60.171	1039.38	2.25	1015.21	24.17	97.46%	97.67%
10.70	0.21	52.00	21.647	16.830	65.189	1125.64	2.25	1097.13	28.51	97.27%	97.47%

3.3.2 Efficiency Graphs

Efficiency is shown in Figure 3-3 through Figure 3-6. Test condition is room temperature, no air flow.

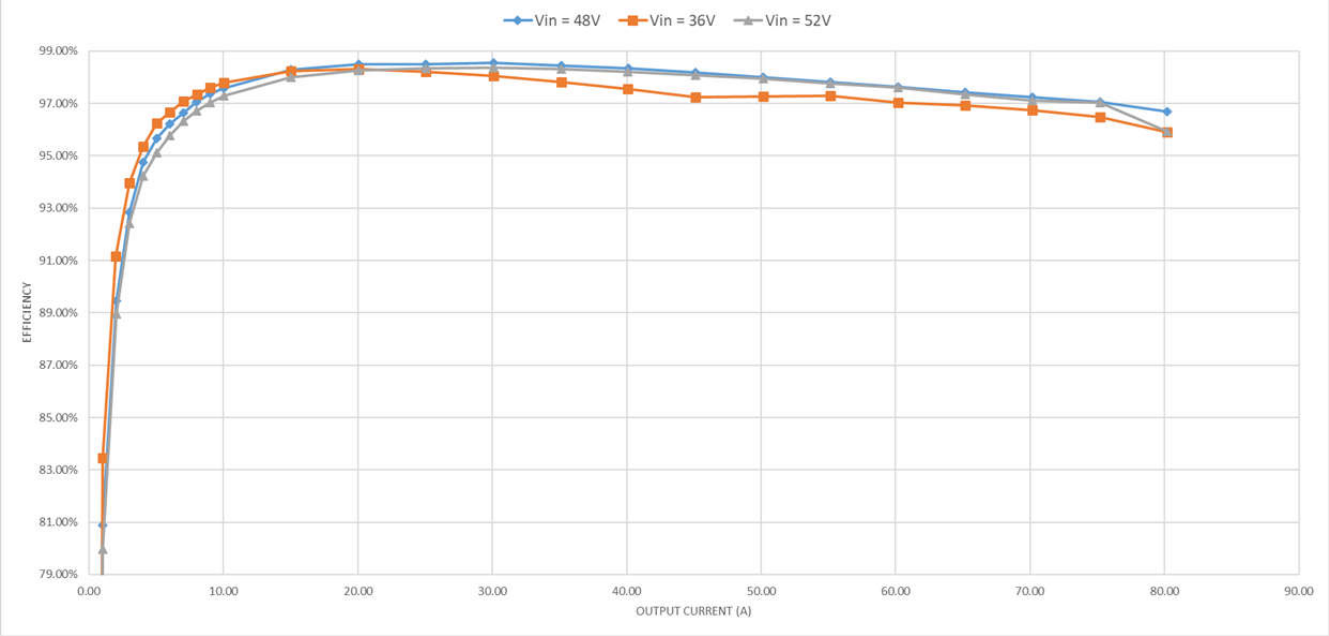


Figure 3-3. 4:1 Conversion Ratio, Power Stage Efficiency vs I_{out}, Full Current Range

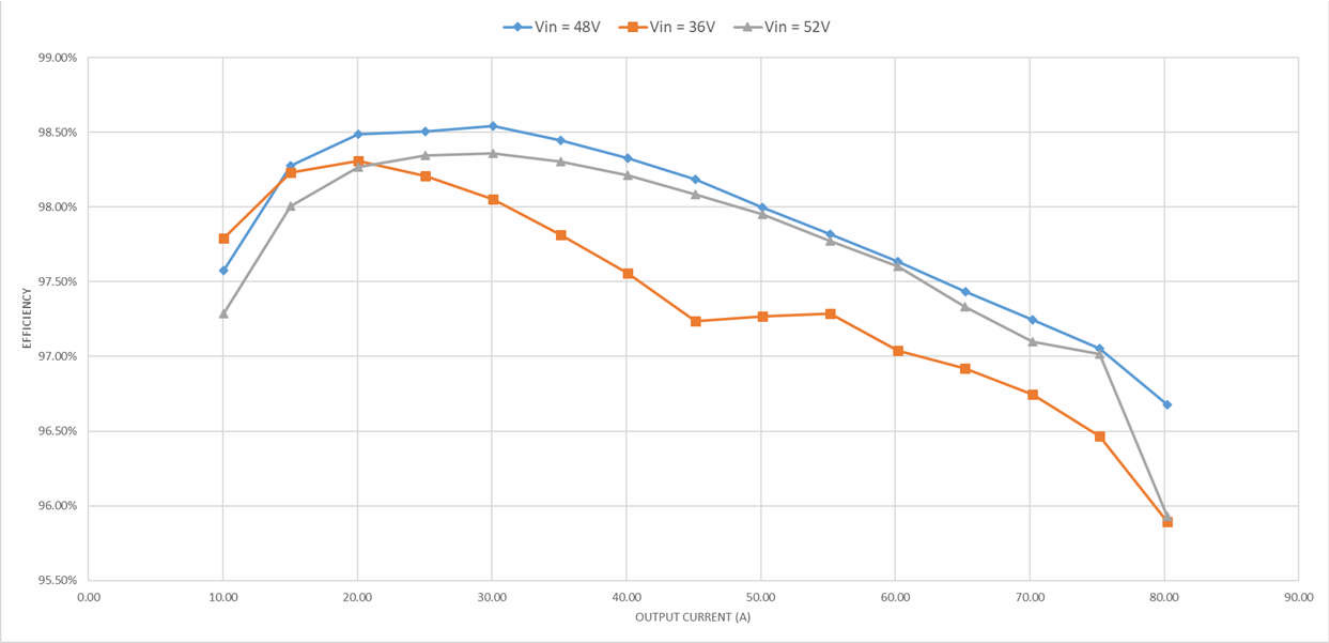


Figure 3-4. 4:1 Conversion Ratio, Power Stage Efficiency vs I_{out}, I_{out} > 10A

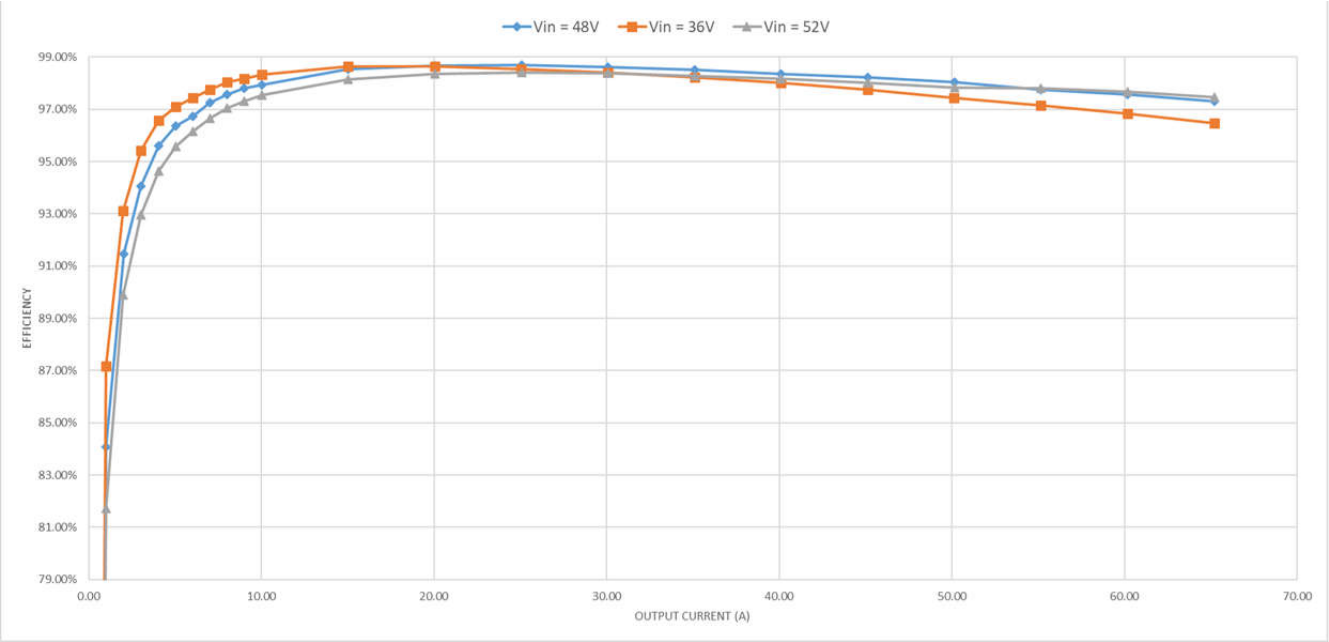


Figure 3-5. 3:1 Conversion Ratio, Power Stage Efficiency vs I_{out}, Full Current Range

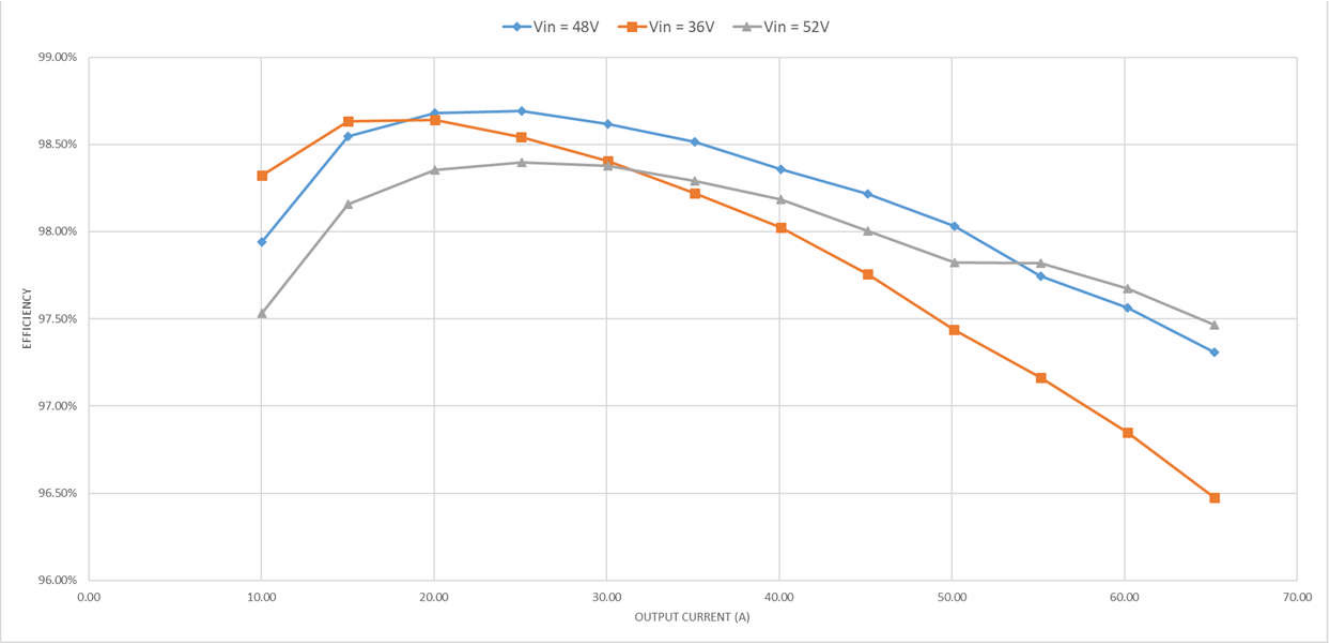


Figure 3-6. 3:1 Conversion Ratio, Power Stage Efficiency vs I_{out}, I_{out} > 10A

3.3.3 Output Voltage Ripple

Output voltage ripple is shown in Figure 3-7 and Figure 3-8.

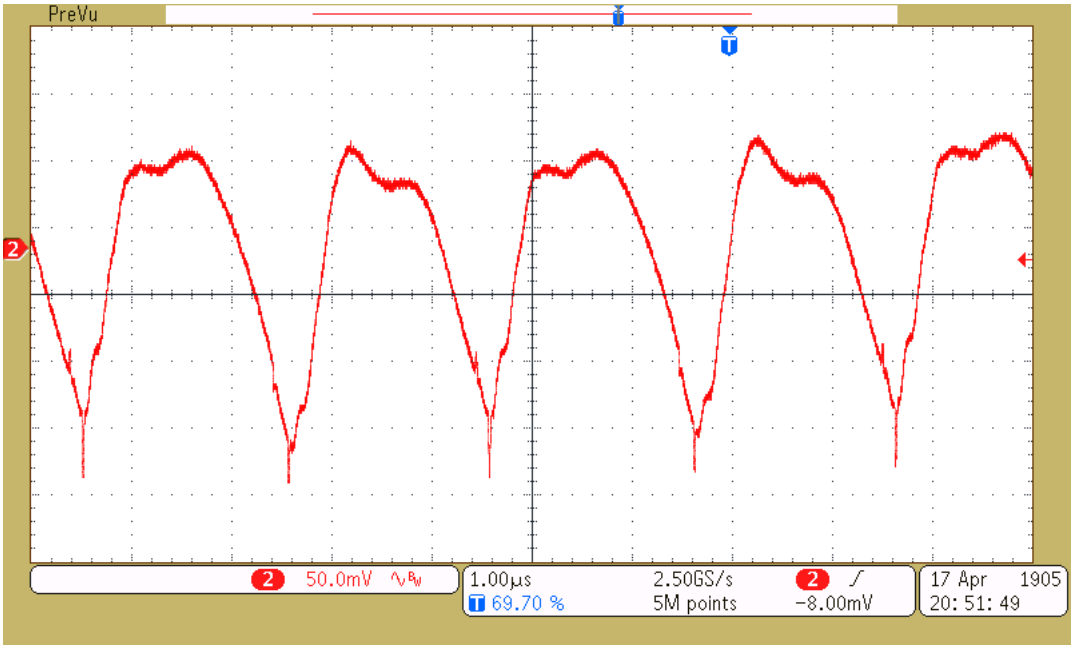


Figure 3-7. Output Voltage Ripple at 48V_{in}, 4:1 Conversion Ratio, I_{out} = 80A

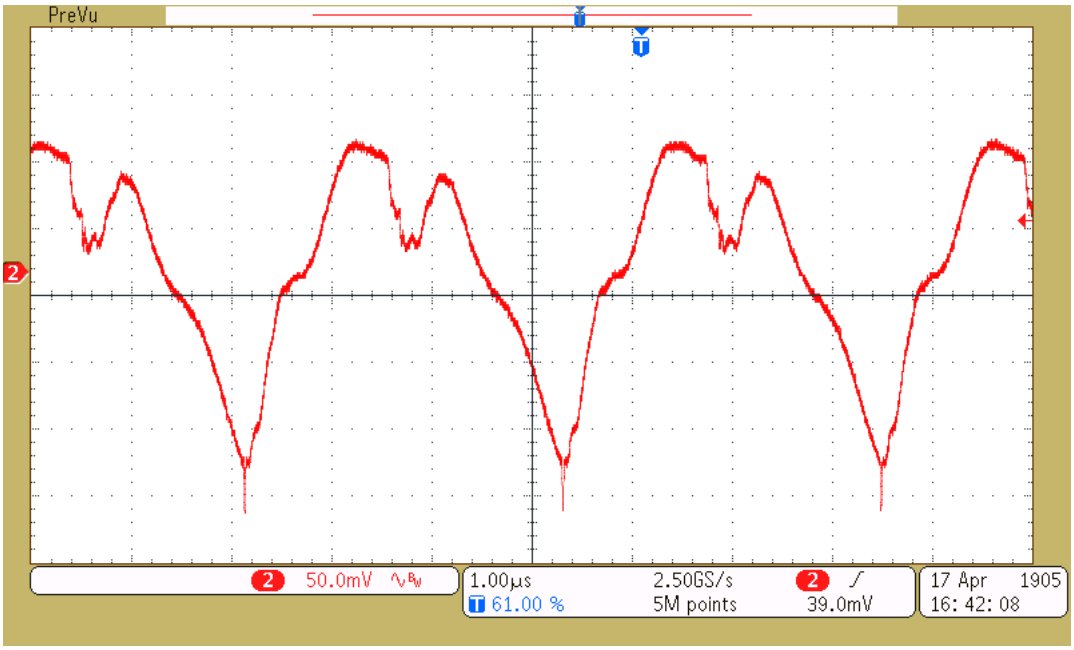


Figure 3-8. Output Voltage Ripple at 48V_{in}, 3:1 Conversion Ratio, I_{out} = 60A

3.3.4 Thermal Images

Thermal images are shown in Figure 3-9 through Figure 3-12. Test condition is room temperature, no air flow.

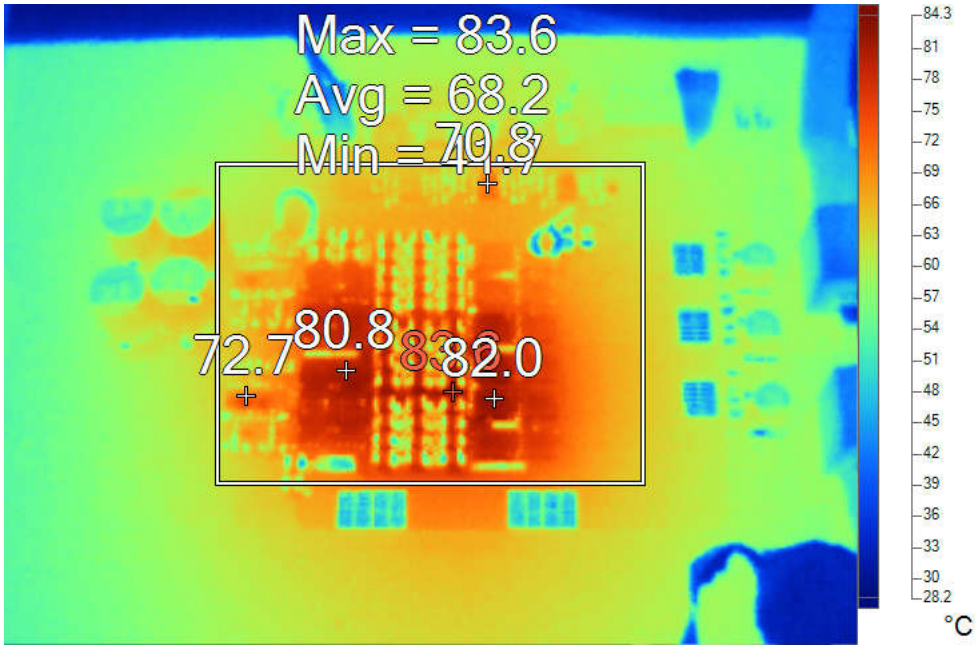


Figure 3-9. Thermal Image at $48V_{in}$, 3:1 Conversion Ratio, 40A Load

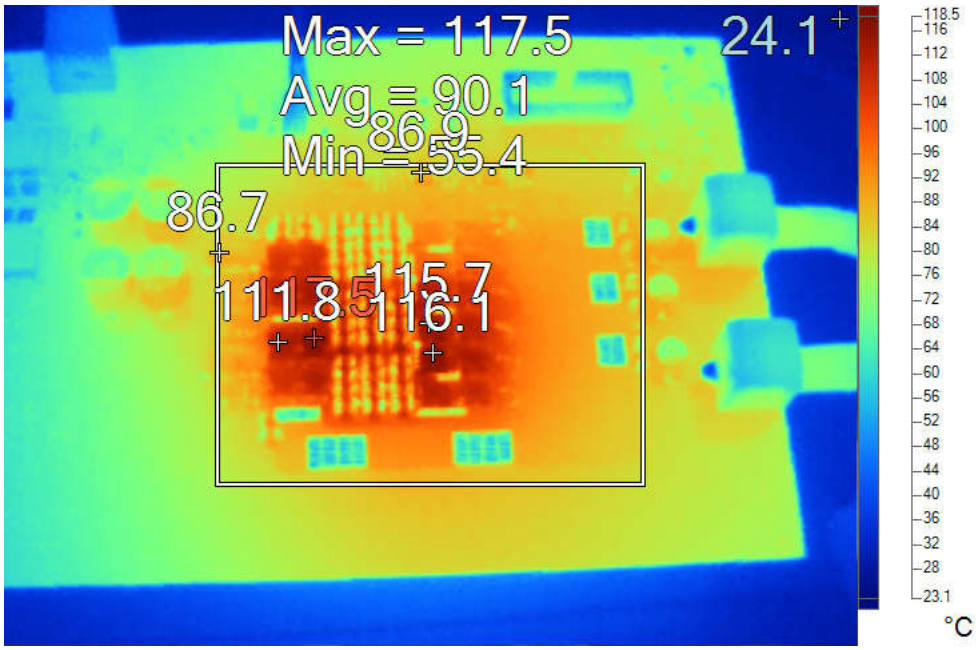


Figure 3-10. Thermal Image at $48V_{in}$, 3:1 Conversion Ratio, 65A Load

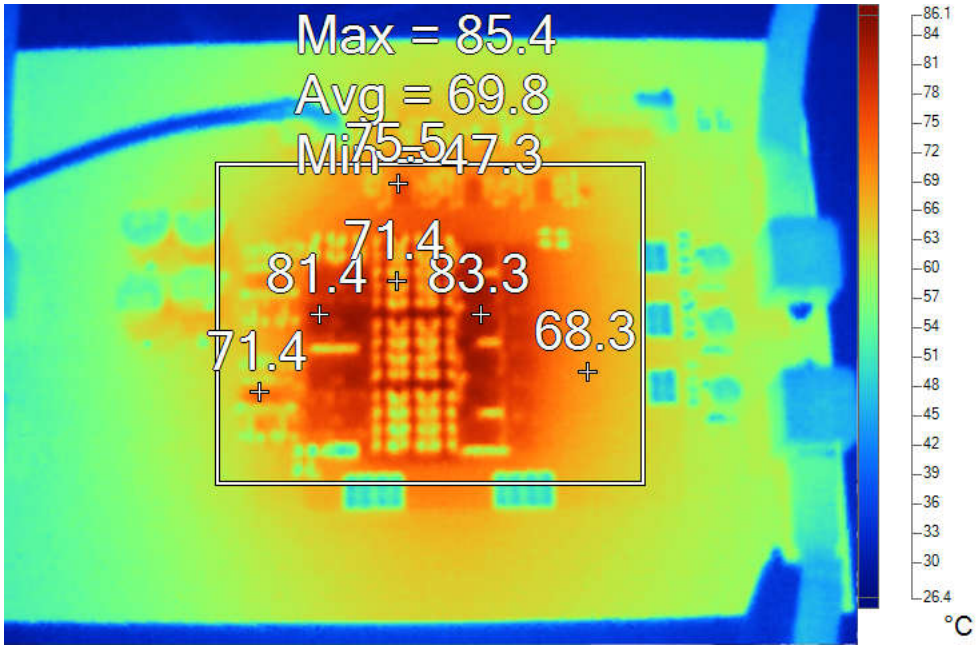


Figure 3-11. Thermal Image at 48V_{in}, 4:1 Conversion Ratio, 60A Load

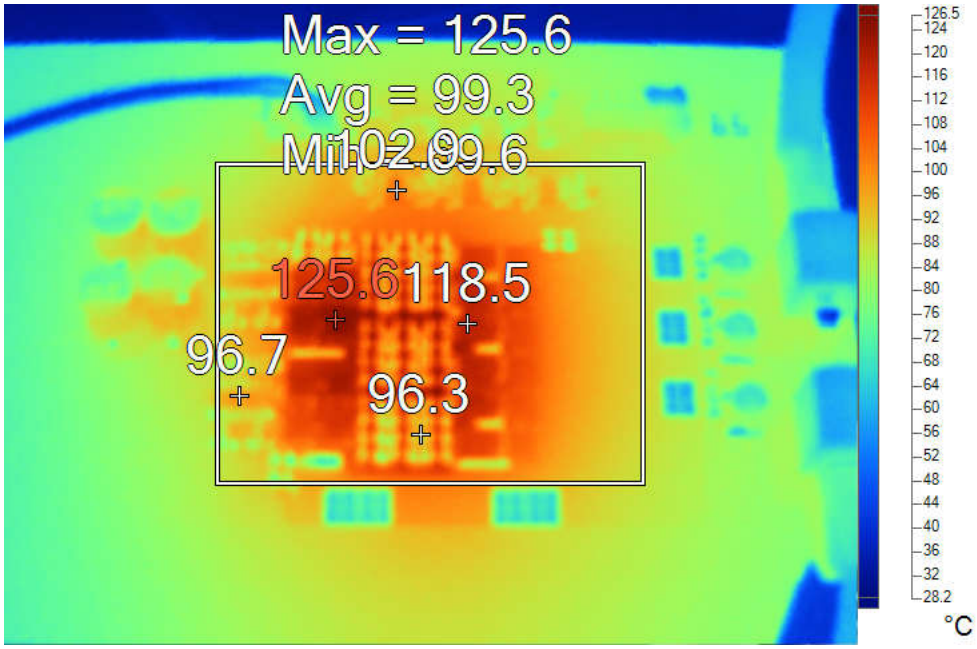


Figure 3-12. Thermal Image at 48V_{in}, 4:1 Conversion Ratio, 80A Load

3.3.5 Switch Voltage Stress of High Side Switches

Voltage stress of high side switches (Q1-Q4 in Figure 2-1) is measured across its drain and source pin (V_{DS}), as shown in Figure 3-13 and Figure 3-14.

Figure 3-13:

CH1: VDS voltage of Q4;

CH2: VDS voltage of Q1;

CH3: VDS voltage of Q2;

CH4: VDS voltage of Q3;

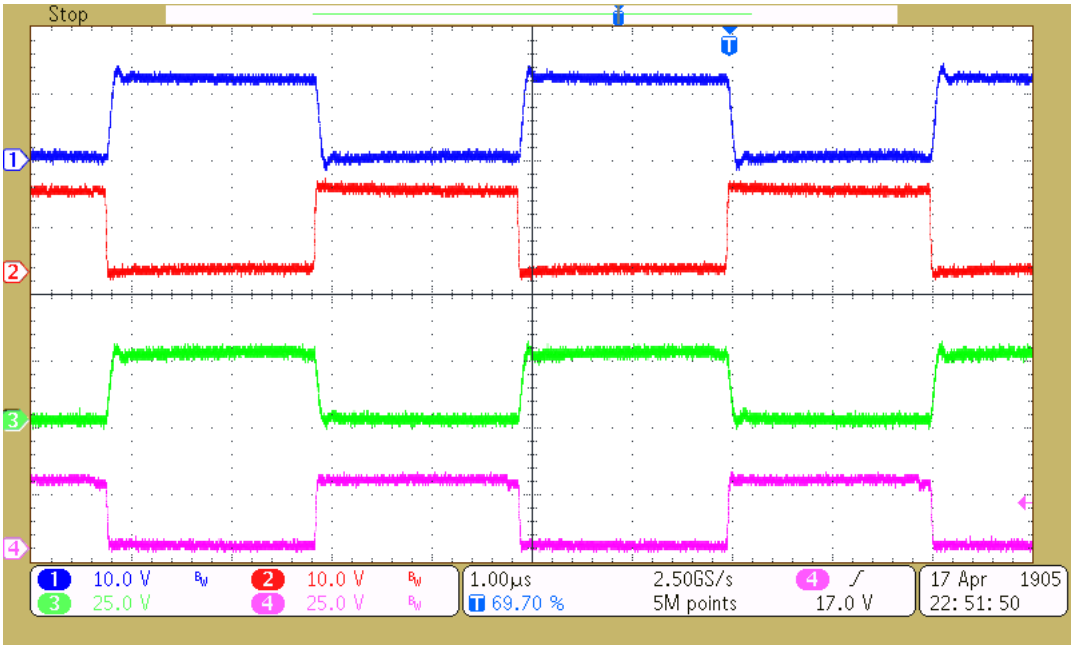


Figure 3-13. VDS Voltages at V_{in} = 48V, 4:1 Conversion Ratio, I_{out} = 80A

Figure 3-14:

CH1: VDS voltage of Q4;

CH2: VDS voltage of Q8; (Q1 is bypassed/forced turn-on; Q8 is measured instead)

CH3: VDS voltage of Q2;

CH4: VDS voltage of Q3;

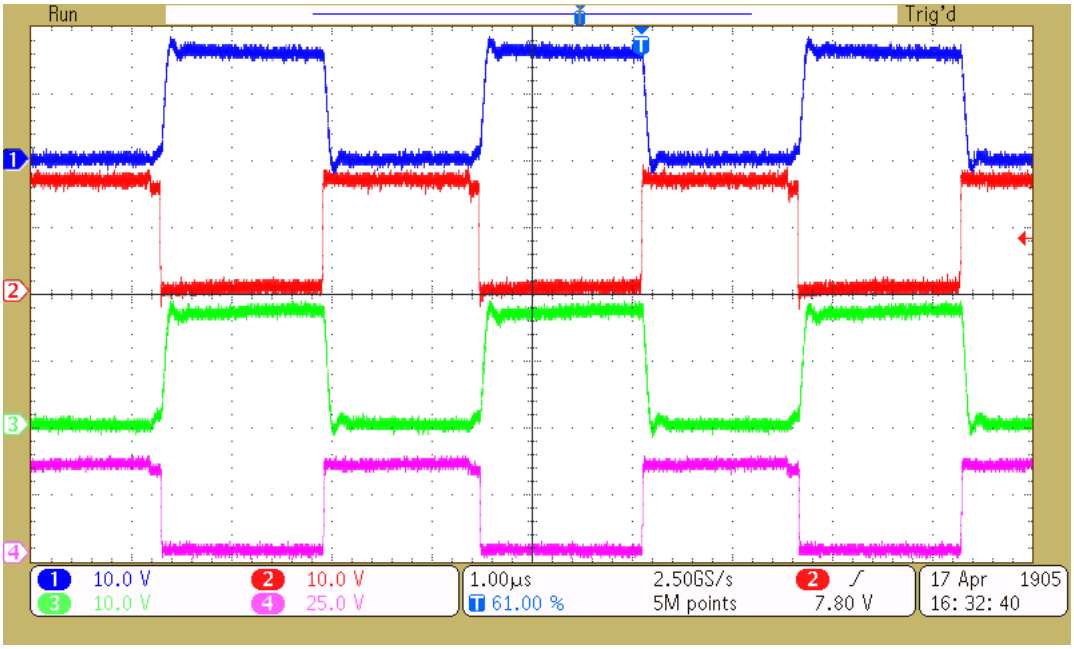


Figure 3-14. VDS Voltages at V_{in} = 48V, 3:1 Conversion Ratio, I_{out} = 60A

3.3.6 Load Transients

Load transient response is shown in Figure 3-15 and Figure 3-16. Current slew rate dI/dt = 0.1A/us.

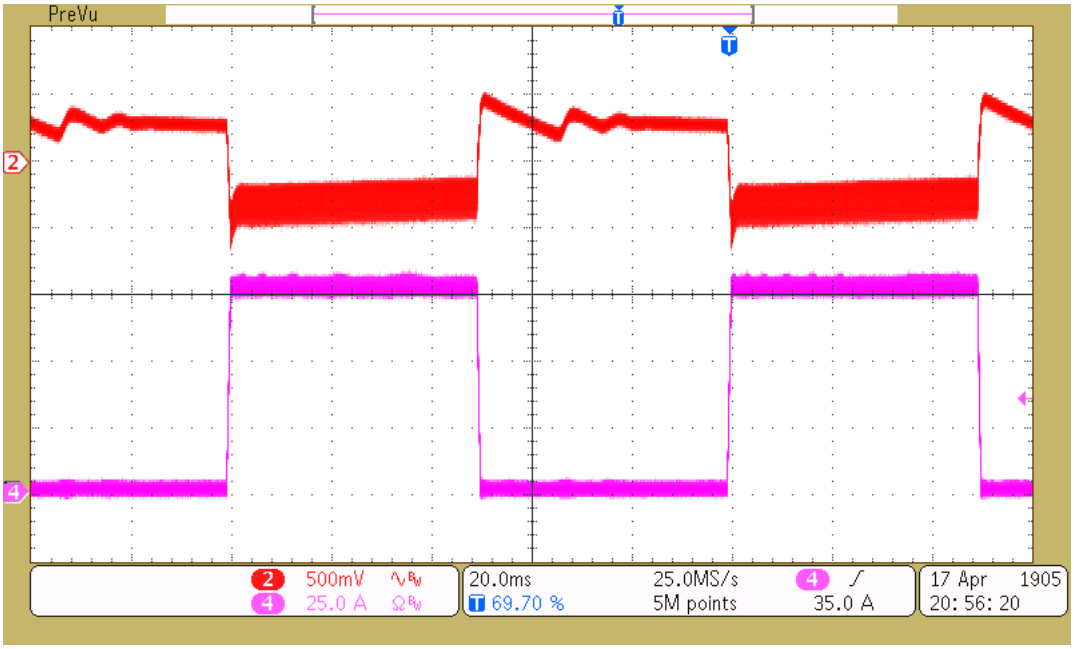


Figure 3-15. Load Transient at V_{in} = 48V, 4:1 Conversion Ratio, I_{out} Step From 0A to 80A

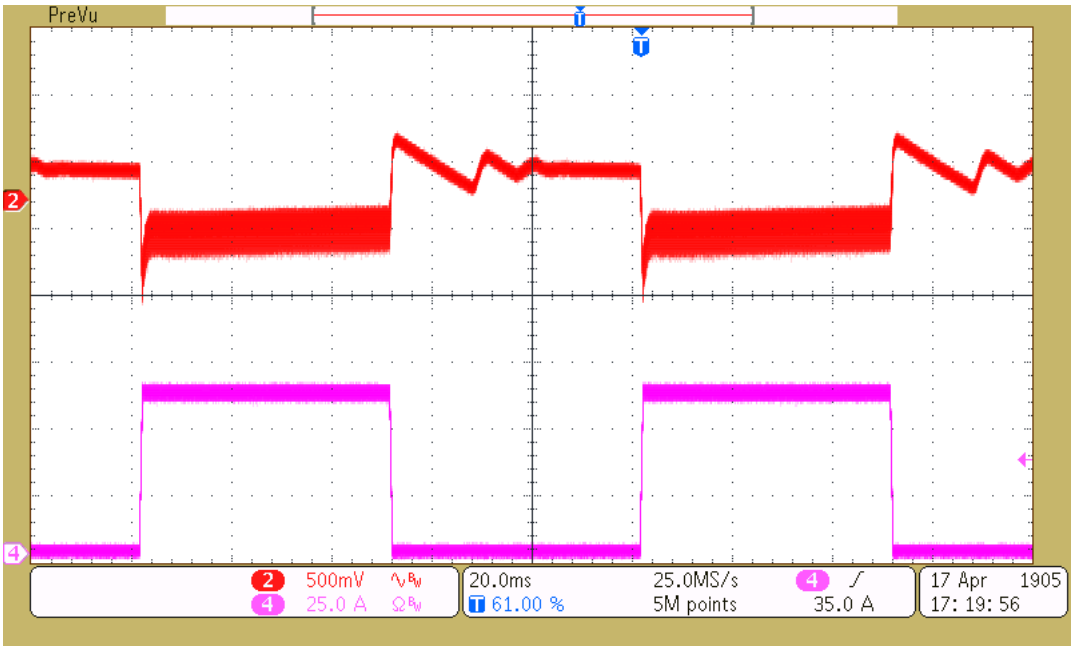


Figure 3-16. Load Transient at V_{in} = 48V_{in}, 3:1 Conversion Ratio, I_{out} Step From 0A to 60A

3.3.7 Reverse Step-up Operation of SCC

Reverse step-up operation is observed (shown in Figure 3-17) via the measurement on the SW node voltage of bias buck converter. V_{SW} here is an indication of whether the 48V on the input (which at the same time is the HV port of the SCC) has been established or not).

Here before the cursor "b" timestamp, the peak of SW node voltage has always been following the 12V input from the LV port (which is the output port for step-down operation).

After the "b" timestamp, the peak of SW node has risen as the reverse step-up operation is charging the HV port capacitors and raising HV voltage. By the time of the cursor "a" timestamp, the reverse operation has been done.

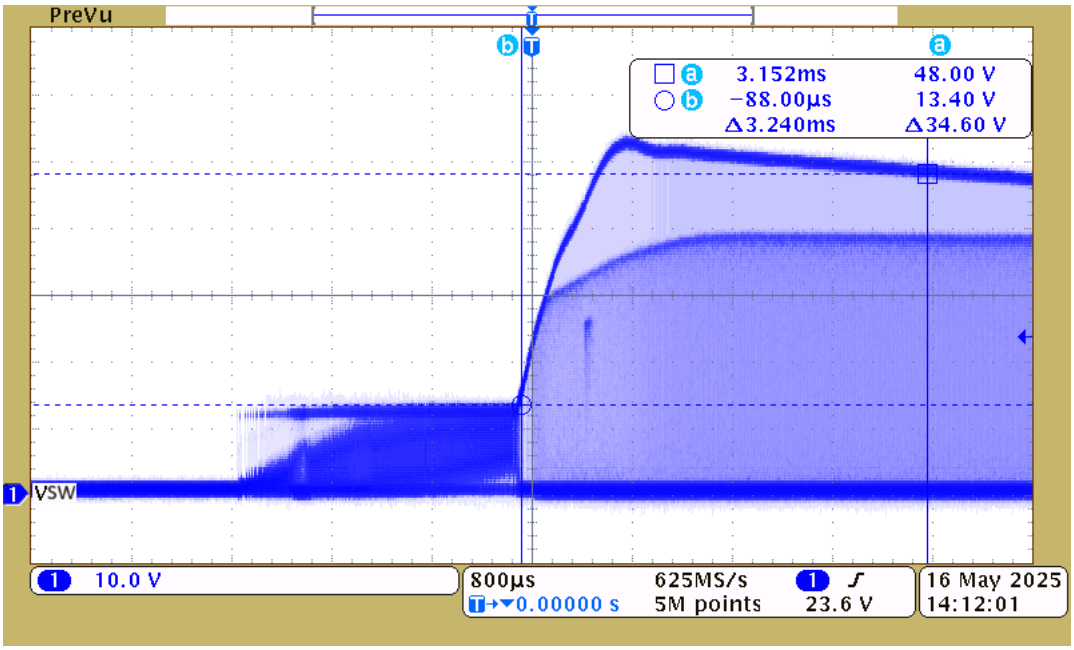


Figure 3-17. Reverse Operation, 1:4 Conversion Ratio, V_{LV} = 12V, SCC Load = 300W.

4 Design and Documentation Support

4.1 Design Files

4.1.1 PCB Layout Recommendations

For this switched capacitor converter design, first follow the PCB layout practice guidelines for general switching converter to improve overall thermal and EMI performance.

- Application reports:
- Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies*
- Texas Instruments, *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Application brief:
- Texas Instruments, *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
- Seminar:
- Texas Instruments, *Constructing Your Power Supply – Layout Considerations*

Aside from these practices, verify the layout is symmetrical as possible across similar structures. For example, for the high-side and low-side FETs (Q1 and Q2 as well as Q3 and Q4) driven by the two UCC21330A-Q1 gate drivers in the design, the layout should be kept in a similar pattern.

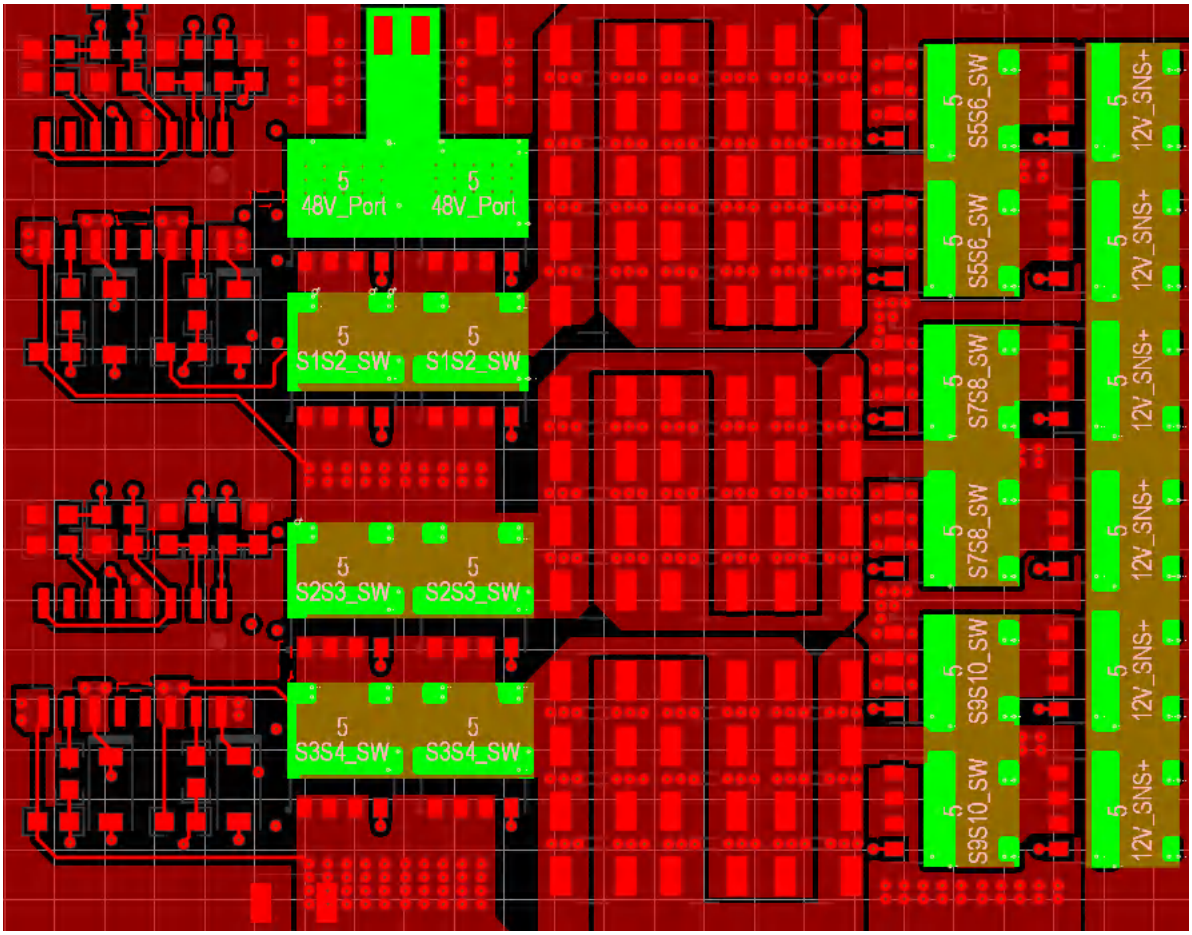


Figure 4-1. SCC Power Stage Layout Example

This helps maintain a similar parasitic inductance in across each flying capacitor leg (C_1, C_2 and C_3 in Figure 2-1) and help reproducing a similar resonant performance.

4.2 Documentation Support

1. Texas Instruments, *UCC21330x-Q1 Automotive 4A, 6A, 3kVRMS Isolated Dual-Channel Gate Driver* Data Sheet
2. Texas Instruments, *UCC27211A-Q1 Automotive 120V, 3.7A/4.5A Half-Bridge Driver with 8V UVLO* Data Sheet
3. Texas Instruments, *TPS1212-Q1 Low IQ Automotive High-Side Switch Controller With Bi-directional IMON, Low Power Mode, Load Wakeup, I2t, and Diagnostics* Data Sheet
4. Texas Instruments, *TLC555-Q1 Automotive LinCMOS™ Technology Timer* Data Sheet
5. Texas Instruments, *TIDA-020094 48V Zone Reference Design*
6. Texas Instruments, *48V Automotive Systems: Why Now?*

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