Using the TPS2410EVM

User's Guide

Literature Number: SLVU181B
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TPS2410 EVM (HPA204)

This user's guide is to facilitate operation of the TPS2410 and TPS2411 evaluation module. It is used by an engineer or technician, and supplements the TPS2410, TPS2411 data sheets, schematics, and circuit board labeling. Two variant of EVM exists for two different package options. TPS2410EVM and TPS2411EVM are used in evaluation of the 14 Pin TSSOP (PW) packaged device and TPS2411EVM-096 can be used to evaluate 14 Pin UQFN (RMS) packaged device. Schematic of both EVM remains the same, however PCB and BOM files differ due to different package option.

1 Introduction

The TPS2410 controls an N-channel MOSFET to operate in circuit as an ideal diode. The MOSFET source and drain voltages are monitored by TPS2410 pins A and C. The TPS2410 drives the MOSFET gate high if VAC exceeds 10 mV, and turns the MOSFET off if VAC falls below a threshold that is both programmable and dependent on the choice of TPS2410 or TPS2411.

The TPS2410 has a turn-off point of 2.5-mv V_{AC}.

TPS2411 is similar to TPS2410 when RSET is open and has a resistor programmable MOSFET turn-off point. The TPS2411 can even be set to a slightly negative shutdown allowing for some voltage back current.

Figure 1 shows the conventional wire-OR of power supplies with diodes. Each diode D1 and D2 is replaced by a TPS2410 and MOSFET eliminating the voltage and power loss in the diode.

The evaluation module is set up to wire-OR two power supplies for redundant power to a load using two TPS2410s and MOSFETs. This document contains setup and user information about this evaluation module to assist with the operation of TPS2410.

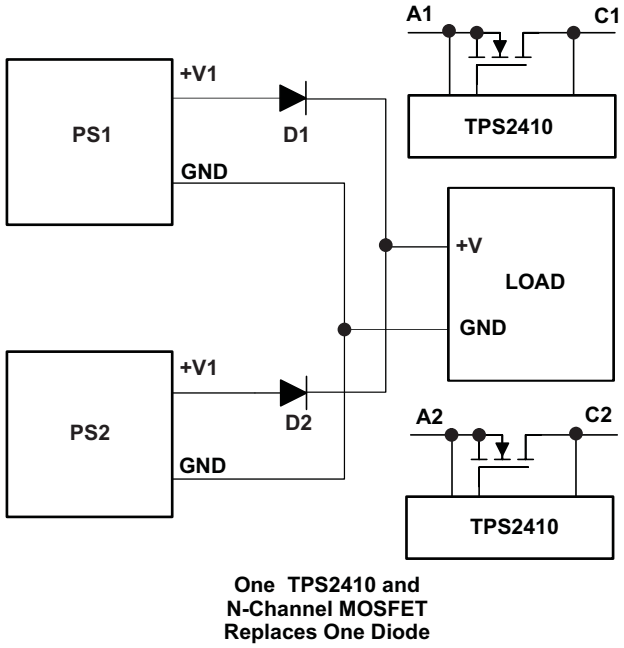


Figure 1. Conventional Wire-OR Power Supplies

Reference Figure 2, a block diagram of the TPS2410EVM and TPS2411EVM.

- The **5-V supply** is used to power status LEDs. It is jumper selected to power VDD on the TPS2410s and the glitch circuit if the control voltage is less than 3.0 V.
- The **status** outputs turn on LEDs to give a visual condition of the system Fault, power good and gate status are displayed.
- The **Glitch** maker, discussed in the Test Methods Section applies a 1-Ω load to the input supply for 100 μs. This disruption allows the user to scope test points and observe system recovery.
- The **RSET** resistor is used to program the turn-off point of the TPS2411.
- The **Filter** compensates for system noise.
- The **UV** and **OV** circuits set permissible limits for input operating voltage.

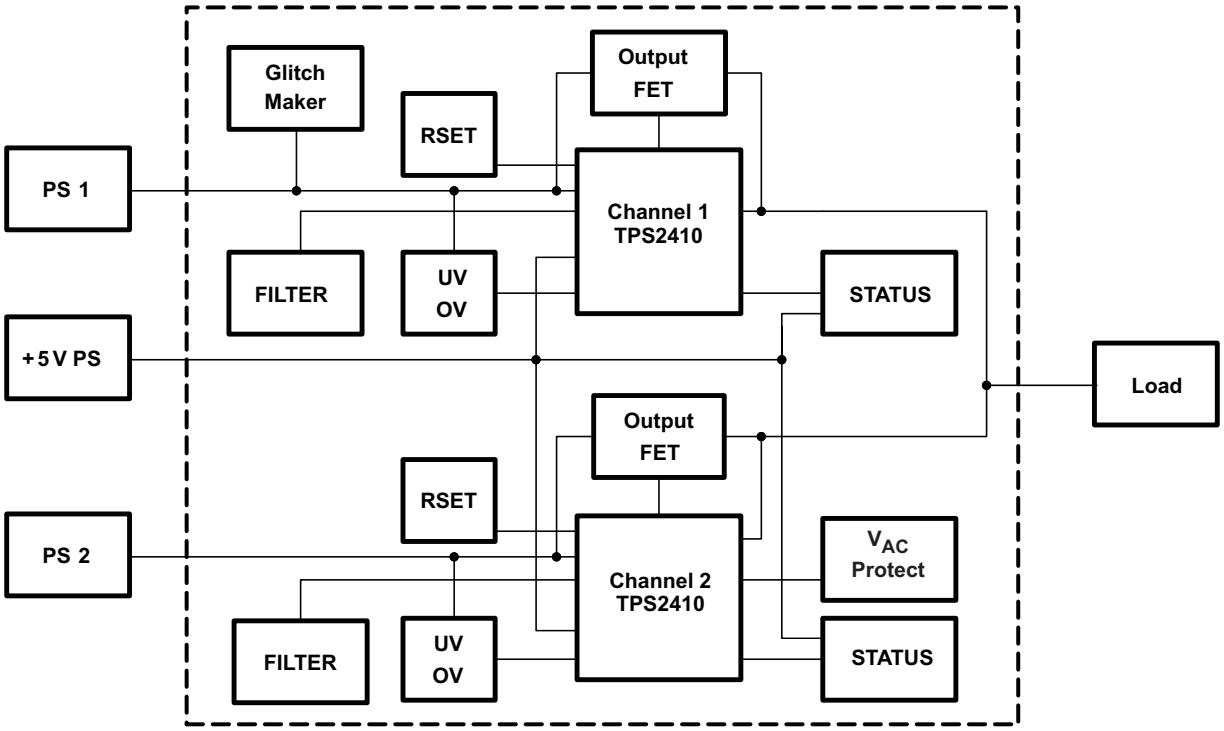


Figure 2. EVM Block Diagram

2 MOSFET Configurations

The TPS2410 EVM is supplied with IRL3713 MOSFETS. These MOSFETs can be replaced with user selected parts if desired as there are alternative MOSFET footprints that accept N-channel parts in D2PACK, DPACK, and SOIC packages. The schematic is shown in Section 4.

The MOSFETs are configured to operate as singles with only Q6 and Q13 populated as supplied. They may be configured to operate in parallel on the PS1 channel by populating Q6 and Q5 and shorting drain to source on Q4. Similarly, for parallel operation on the PS2 channel, populate Q13 and Q12 and short drain to source on Q11. MOSFETs can be configured back-to-back by populating only Q4 and Q5 on channel 1, and Q12 and Q11 on channel 2.

In single or parallel configurations, the body diode of the MOSFET limits V_{AC} to 0.7 V. For back to back MOSFETs, there could be a danger of exceeding the V_{AC} operating maximum 5 V. The V_{AC} protect circuit is a low powered FET that is turned on when V_{AC} approaches the maximum.

3 LED Indicators

Each channel has LED indicators for fault (FLTB), gate status (STAT), and power good (PG). Table 1 summarizes the indicators. Each indicator is labeled on the circuit board for easy reference.

Table 1. LED Indicators

Indicator	Channel 1	Channel 2	LED On
Fault (FLTB)	D3	D8	Fault = on
Gate Status (STAT)	D2	D7	Bad gate = on
Power Good (PG)	D1	D6	Power good = on

3.1 User Circuits

There are two sections of the circuit board with plated through holes for user defined circuits.

3.2 Materials Needed – TI Supplied

- TPS2410 evaluation module
- TPS2410 reference design documentation
- TPS2410 data sheet

3.3 User Supplied

- 2 – power supplies for wire-OR to load, up to 25 A
- 1 – 5-V power supply to supply EVM
- Power supply cables
- Load – active load, power resistors or actual load
- Oscilloscope
- Current probe
- Differential probe

3.4 Jumper Description

Jumpers J1, J2, J13, J14
V_{DD} can be powered by the input power supply pin A, Jump J2-2, 3 and J14-2, 3. When it is powered by the load, pin C, jump J2-1, 2 and J14-1, 2. If A and C are less than 3 V, connect the 5 V to V_{DD}, jumper J1-1 to J2 -2 and J13-1 to J14-2.

J3, J15
Jumpers J3 and J15 connect a pot to the RSET pin when testing the TPS2411. These jumpers are normally left open when testing the TPS2410.

J4, J17
Jumpers J4 and J17 are open to enable the UV and OV inputs to the TPS2410.

J6
Jumper J6 is on to connect the STAT pins together on both TPS2410 channels. When the STAT pin is low, the turn off of the channel powering the load is de-sensitized.

J8
Jumper J8 is the gate voltage for the Glitch FET. Jump J8-2, 3 when the PS1 voltage is greater than 5 V. Jump J8-1, 2 to use the 5-V supply when PS1 is less than 5 V.

J16
Jumper J16-2, 3 connects pin C to the load for single or parallel FETs. Connect J16-1, 2 to protect the pin A and C inputs when output FETs are configured back-to-back.

3.5 Procedure – Jumper Set-Up

An initial jumper setup is recommended in Table 2. The module has flexibility to operate in other modes. Change jumpers to operate in other configurations as required after getting started. After the initial setup, reference the schematic and set jumpers as required for testing. Other J reference designators on the schematic are simple connectors.

Table 2. Initial Jumper Settings

Jumper	Function	Selection	Comment
J1	5 V to V_{DD}, CH1	Open	
J2	A or C to V_{DD}, CH1	Jumper 2 - 3	Connects A
J3	Install to use RSET, CH1	Open	
J4	In to disable OV channel 1	Open	
J6	In to OR STAT lines	Open	
J8	5 V or PS1 to gate of PS1 pulse	Jumper 2 - 3	Connects PS1
J13	5 V to V_{DD}, CH1	Open	
J14	A or C to Vdd, CH2	Jumper 2 - 3	Connects A
J15	Install to use RSET, CH2	Open	
J16	Connects the load to CH2 C or FET	Jumper 2 - 3	Connects C
J17	In to disable OV Channel 2	Open	

3.6 Power Supply Connection

Connect the power supplies and load to the TPS2410 test card as shown in Table 3. Loading less than 30 A is safe for IRl3713S. The load can be a test load or the actual system load.

Table 3. Power Supply Connection

Connection	Supply	Terminal
PS1	+V	PS1, J12
PS1	PS1, J312	IN1, J5
PS1	GND	PS1GND, J10
PS2	+V	PS2, J18
PS2	GND	PS2GND, J19
5 V	5 V	J20-2
5GND	GND	J20-1
Load +	Load, +V	J7
Load –	GND	J11

3.7 OV and UV Setup

Set the OV and UV pots for each input voltage selected and re-adjust these pots when the input voltage range is changed.

For this example, PS1 and PS2 are 12 V ±20 %. Set PS1 to the undervoltage set point, 9.6 V, and adjust R13 until TP7 measures 0.6 V, reference Table 4. Set PS1 to the overvoltage set point, 14.4 V, and adjust R12 until TP10 measures 0.6 V.

Complete this procedure for channel 2. Set the power supply voltages, PS1 and PS2, to the typical input, 12 V.

Table 4. UV and OV Setup

Supply Setting	Potentiometer	Test Point
PS1-UV	R13	TP7
PS1-OV	R12	TP10
PS2-UV	R32	TP24
PS2-OV	R31	TP26

3.8 Test Points

Table 5 lists some common test points for observation. There are more test points shown on the schematic.

Table 5. Common Test Points

Function	TP Channel 1	TP Channel 2
A	TP2	TP18
C	TP9	–
GATE	TP11	TP22
OV INPUT	TP10	TP26
UV INPUT	TP7	TP24
FAULT	TP8	TP25
PG	TP4	TP20

3.9 RSET

RSET is usually used in TPS2411 and sometimes in the TPS2410 to program the MOSFET turn-off point. The RSET calculation from the data sheet is:

$$R_{RSET} = \left(\frac{-470.02}{V_{OFF} - 0.00314} \right) \quad (1)$$

Calculate the RSET resistor. For the PS1 channel, remove jumper J3 and connect an ohm-meter from J3-2 to GND. Adjust pot R8 for the calculated resistance value. Install the jumper J3-1, 2. Repeat for the PS2 channel RSET Pot R26 and jumper J15. The component reference designators for each channel is summarized in Table 6.

Table 6. RESET Resistor Setting

RSET Pot	Jumper	Measure
R8	J3	J3-2
R26	J15	J15-2

3.10 Test Methods

The EVM has many operating configurations to view the system response. The user can make modifications to the EVM jumpers and test other set ups.

3.11 Adjust Input Power Supplies

Vary the input voltages to observe system behavior. Jumpers can be set as in Table 2. Turn the power supplies to the application typical volts; for this paper, we will use 12 V. The load is shared between the supplies. Both gates will be on and the power supply current meters show output. Decrease one supply voltage slightly and note the gate on that channel pass FET turn off and the other channel FET gate increases to keep the FET on to supply the load. Observe the FET gates with a scope. With a voltmeter, verify V_{DS} for the on channel to be tens of millivolts.

3.12 Glitch Maker

Remove the jumper from J5 to J12 and connect the power supply to J12. This reduces the bulk capacitance at the PCB power supply input. Set power supplies up for equal or slight differential voltage so that the PS1 supply is contributing to the load. Press momentary switch S1, labeled PULSE. The switch closure places a 1-Ω load across the input power supply for 100 μs. Observe the effect of an input power supply glitch. Scope on the MOSFET gates, load voltage, TPS2410 fault output, STAT and PG.

3.13 Load Change

A dynamic change to the load can be made by switching additional load on or off with an external switch. Some power load test equipment can be used to dynamically change the load.

4 Scope Traces

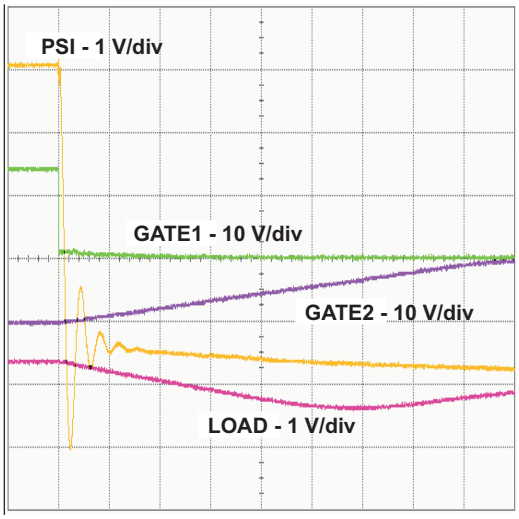


Figure 3. PSI Shorted, Loaded

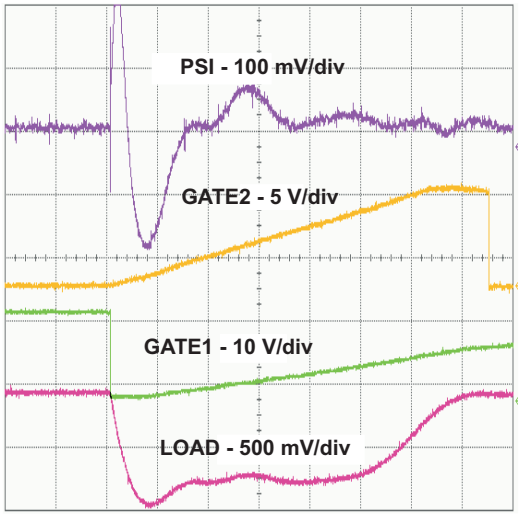


Figure 4. PSI Glitched

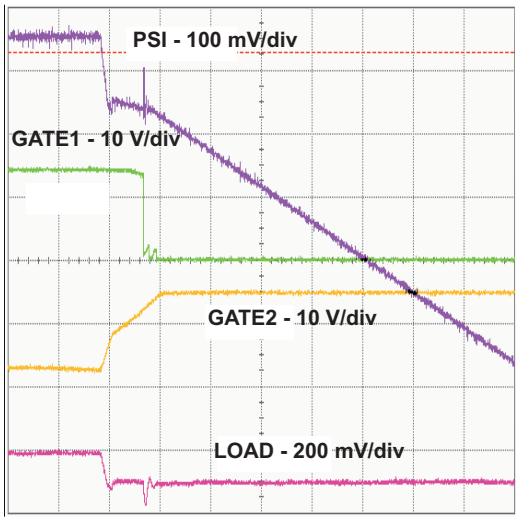


Figure 5. PSI Set to Standby

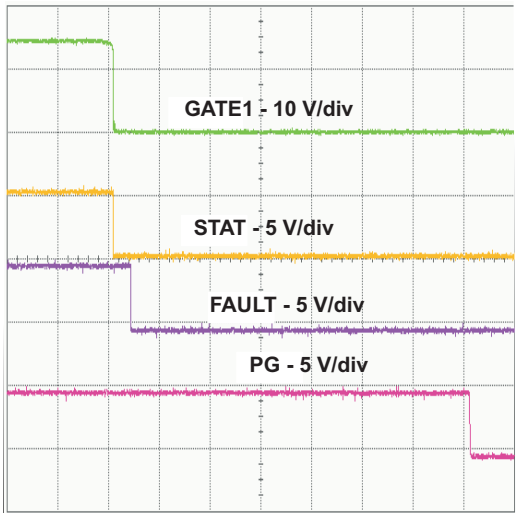


Figure 6. PSI Set to Standby

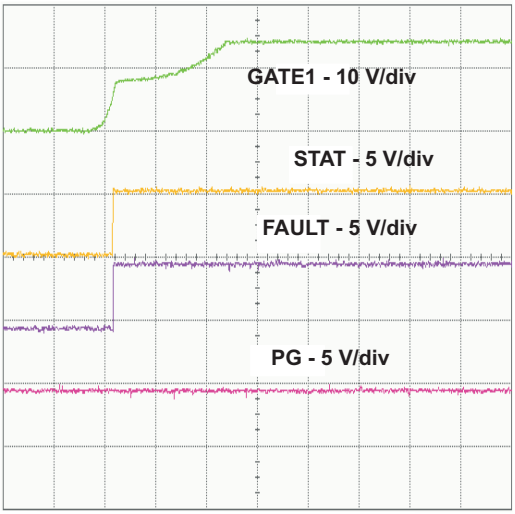


Figure 7. PS2 On - PSI Turned On From Standby

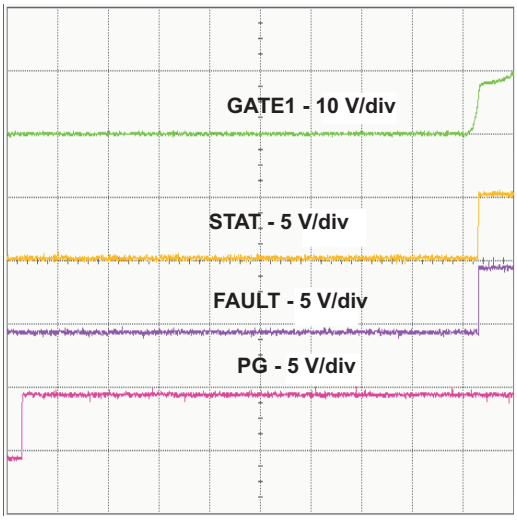


Figure 8. PSI Turned On From Standby

5 Schematics

Schematics of TPS2410EVM and TPS2411EVM is shown in Figure 9, Figure 10 and Figure 11. Schematics of TPS2411EVM-096 is shown in Figure 12, Figure 13 and Figure 14.

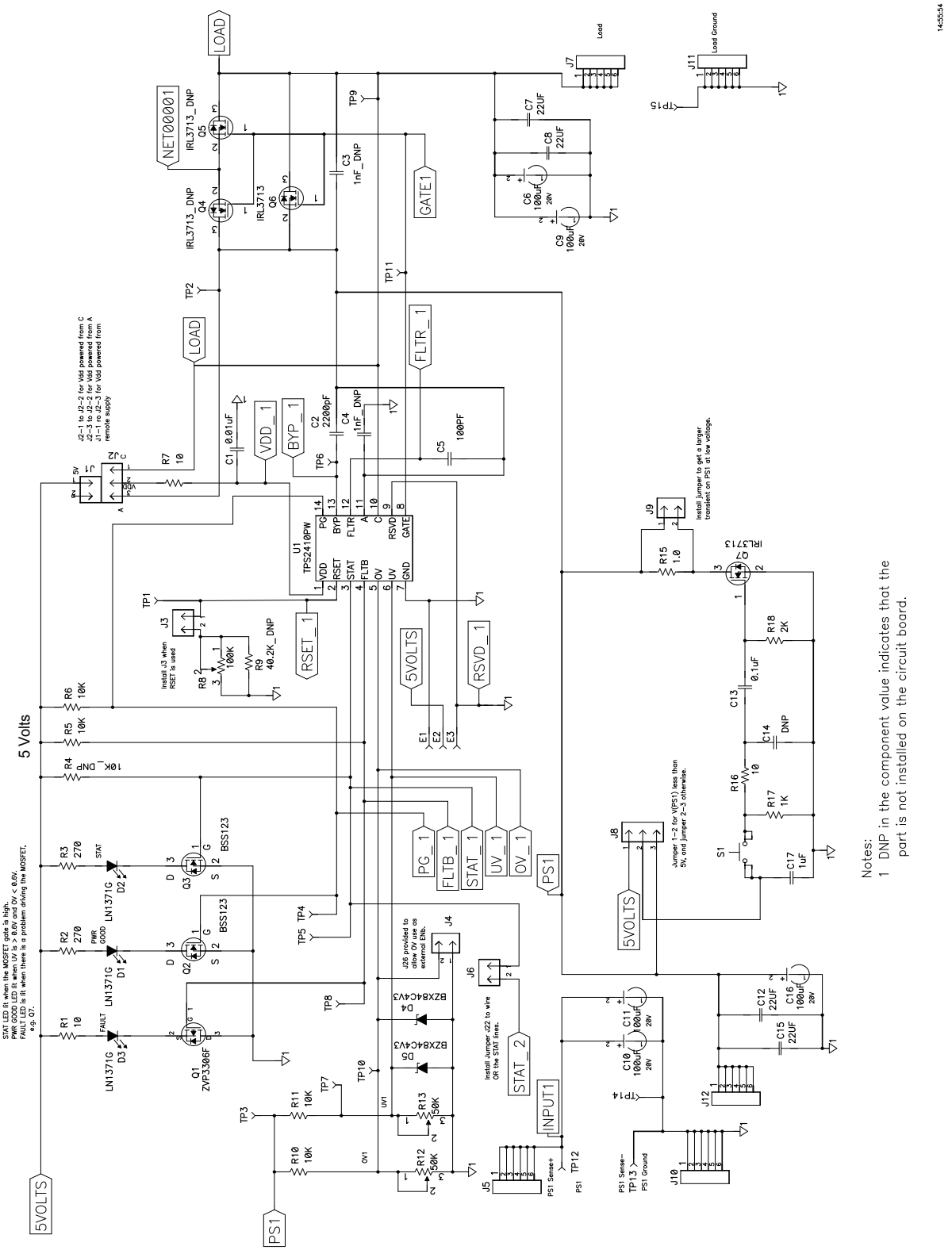


Figure 9.

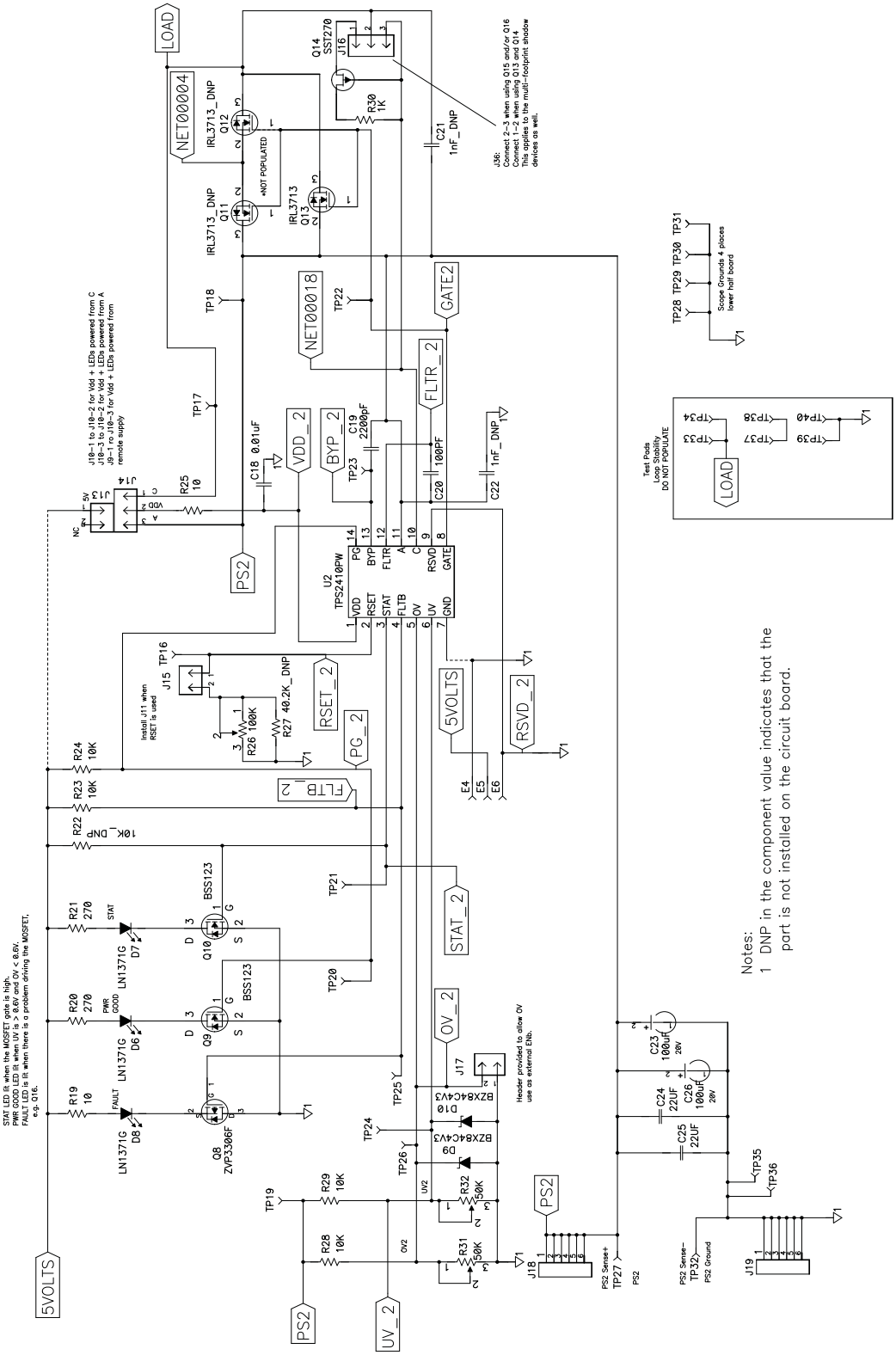
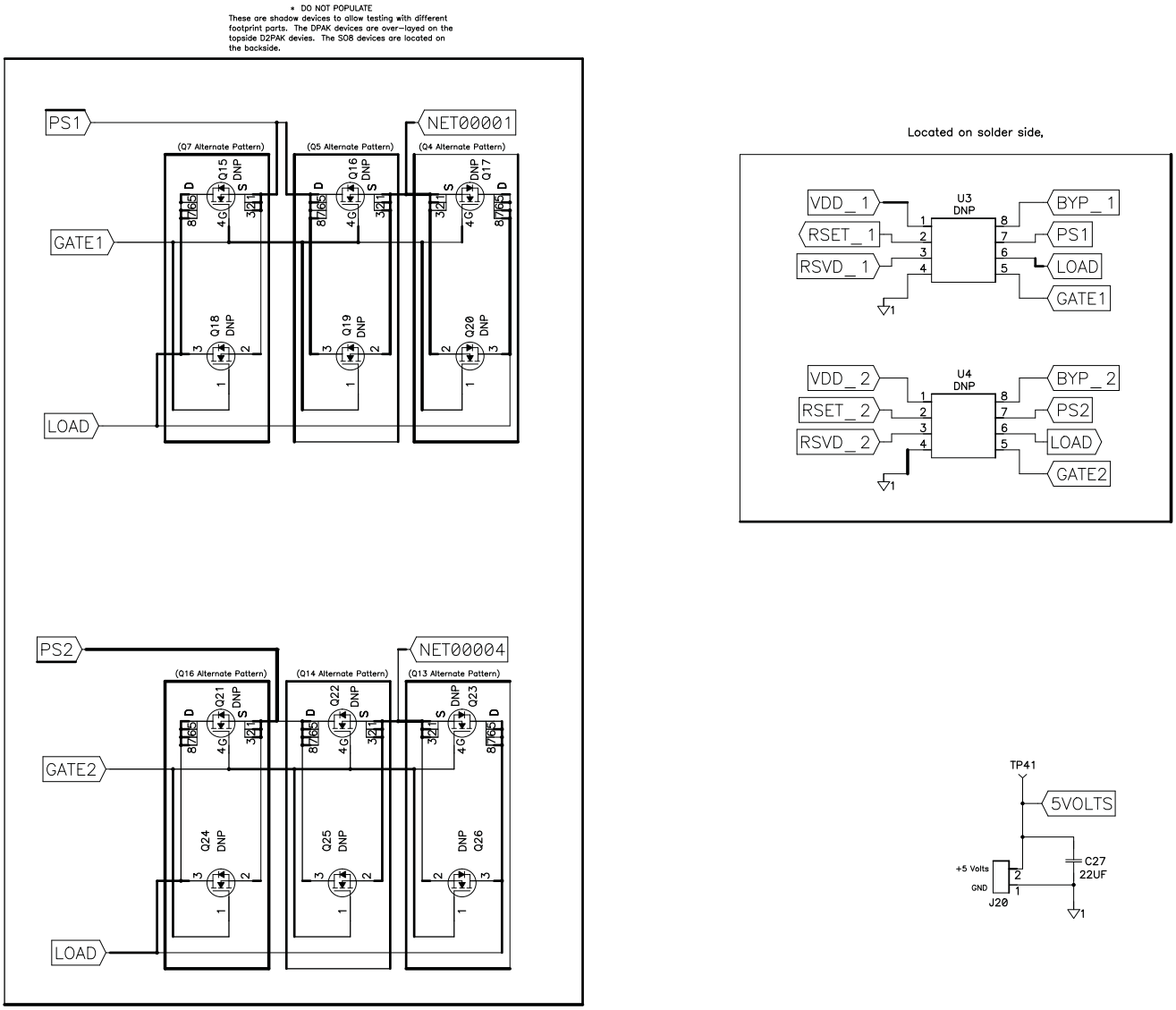


Figure 10.



Notes:
1 DNP in the component value indicates that the part is not installed on the circuit board.

Figure 11.

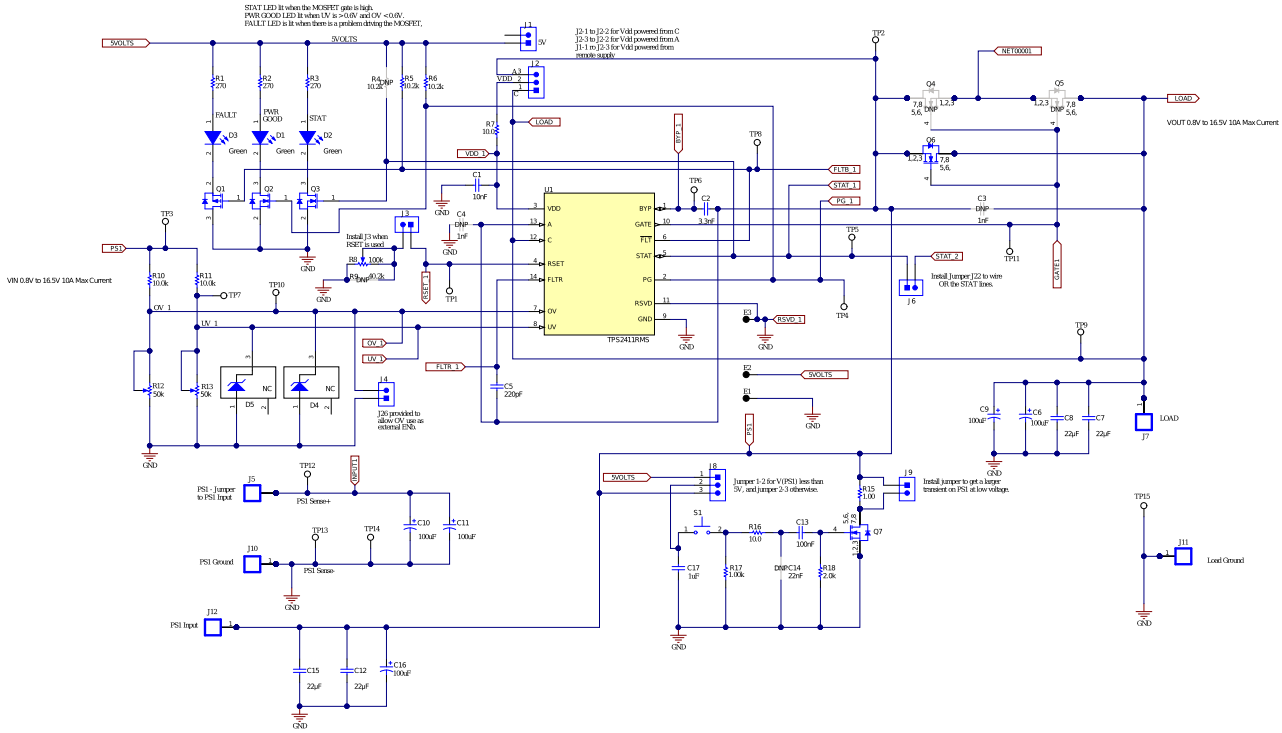


Figure 12. TPS2411EVM-096 Schematic Sheet 1

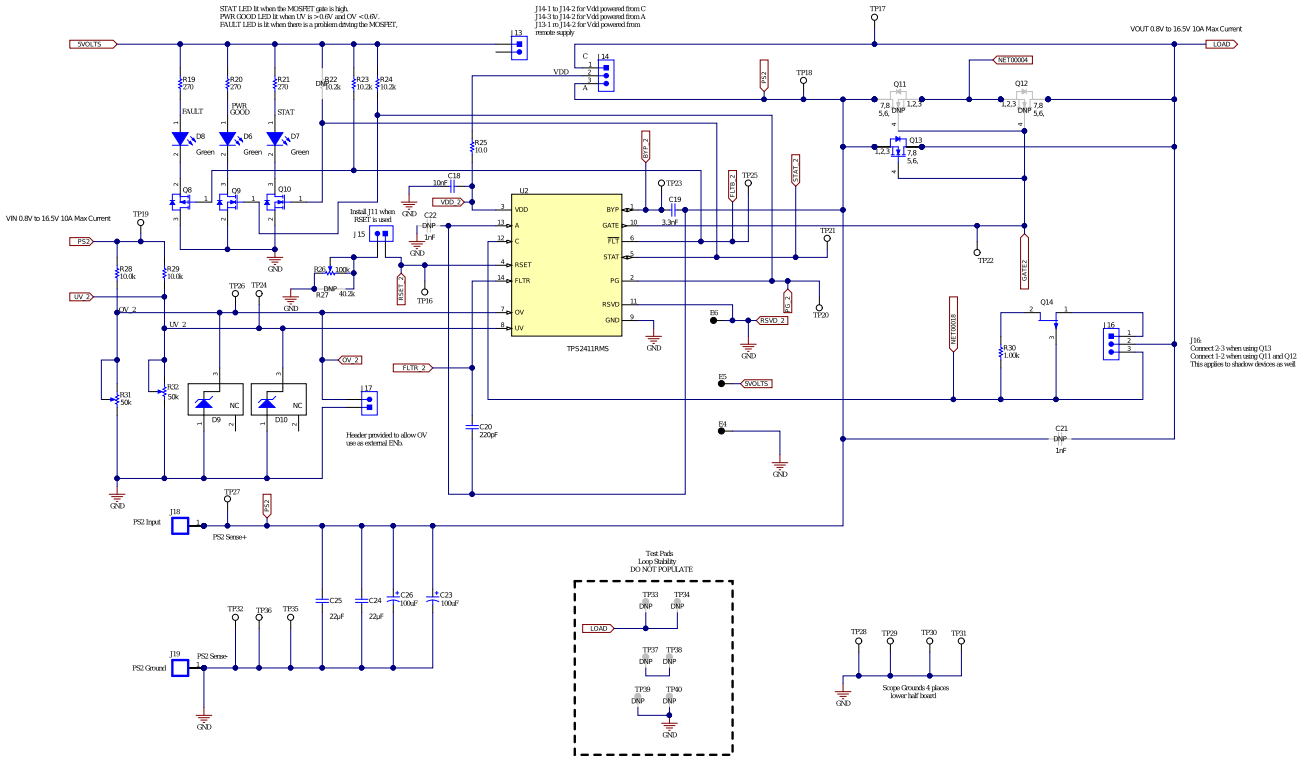


Figure 13. TPS2411EVM-096 Schematic Sheet 2

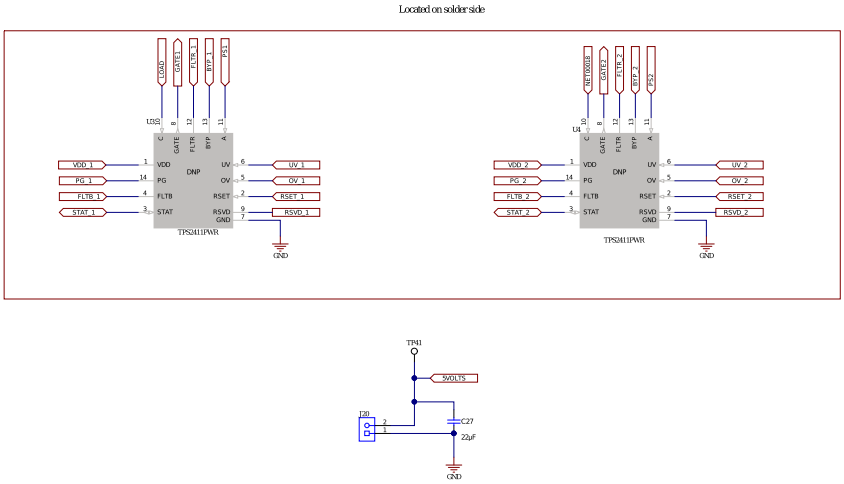


Figure 14. TPS2411EVM-096 Schematic Sheet 3

6 EVM Assembly Drawings and PCB Layout

Assembly Drawings and PCB Layout for TPS2410EVM and TPS2411EVM are shown in Figure 15 through Figure 18. Assembly Drawings and PCB Layout for TPS2411EVM-096 are shown in Figure 19 through Figure 24.

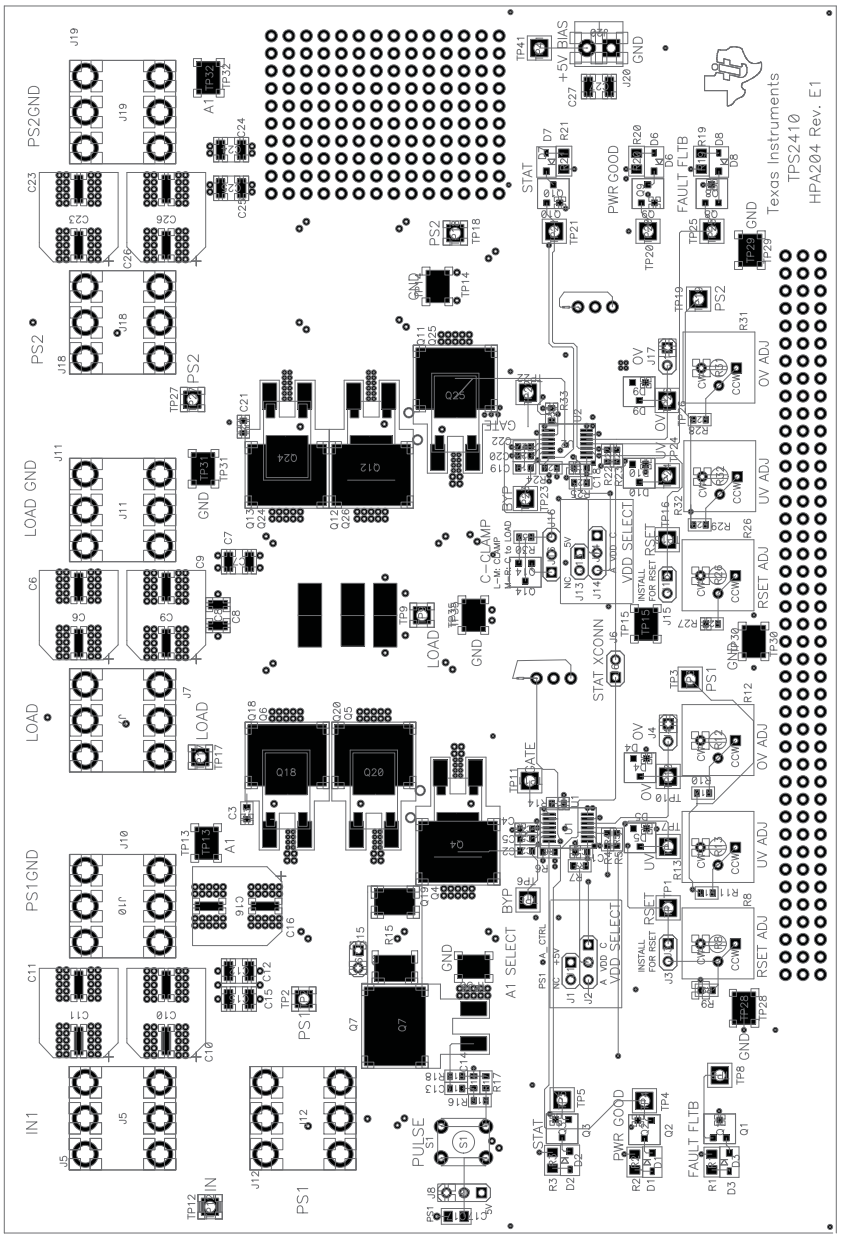


Figure 15. TPS2410EVM Top Overlay

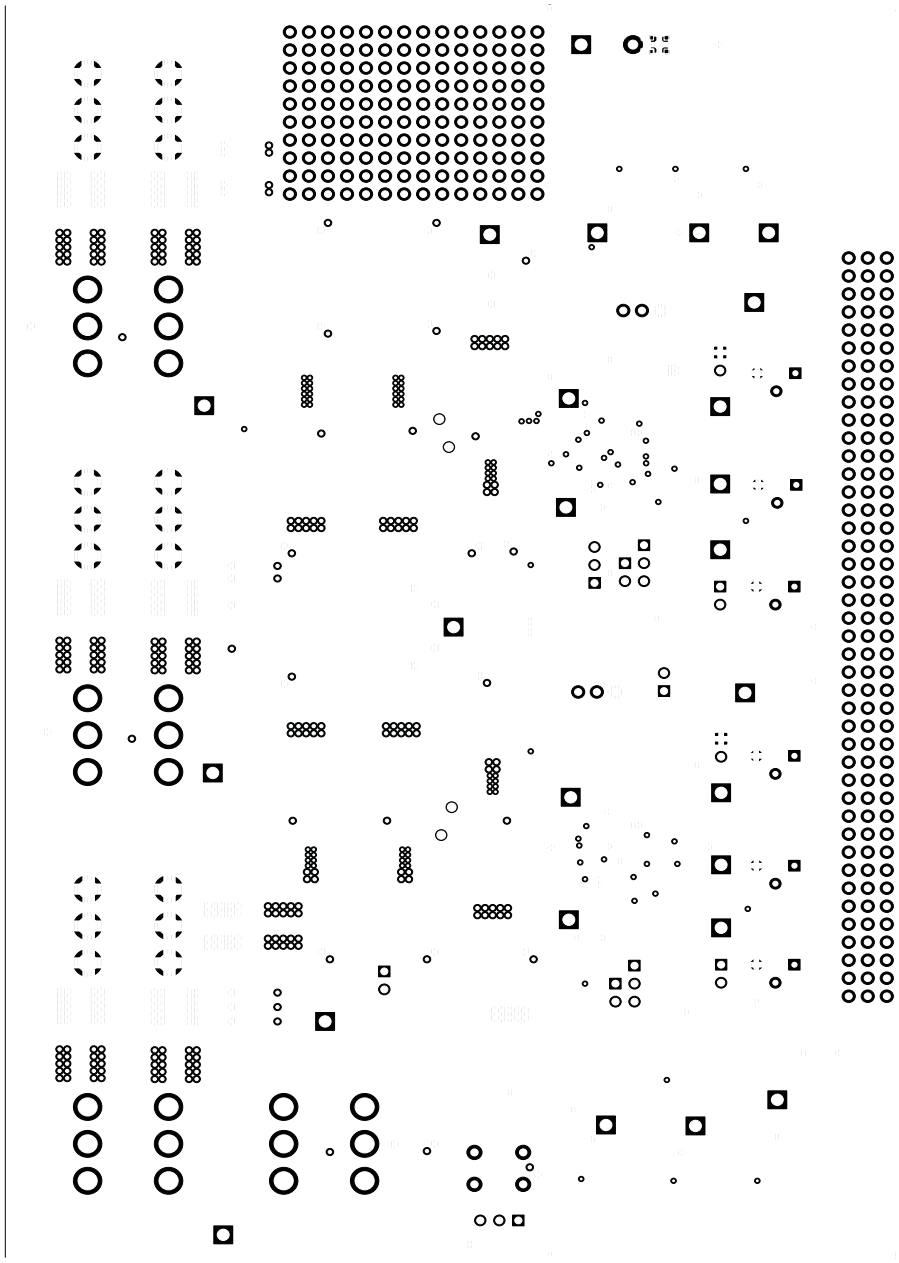


Figure 16. TPS2410EVM Internal Layer 1

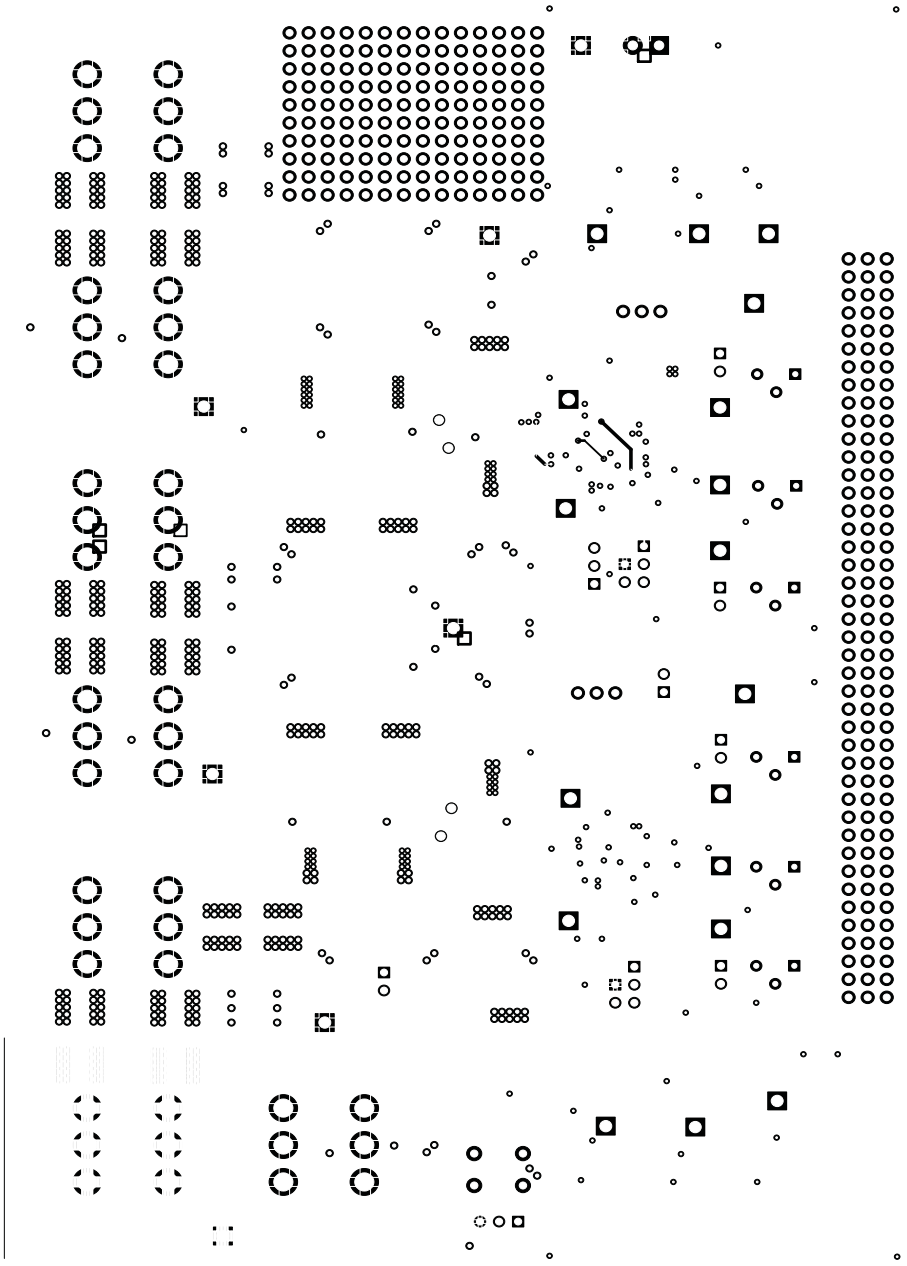


Figure 17. TPS2410EVM Internal Layer 2

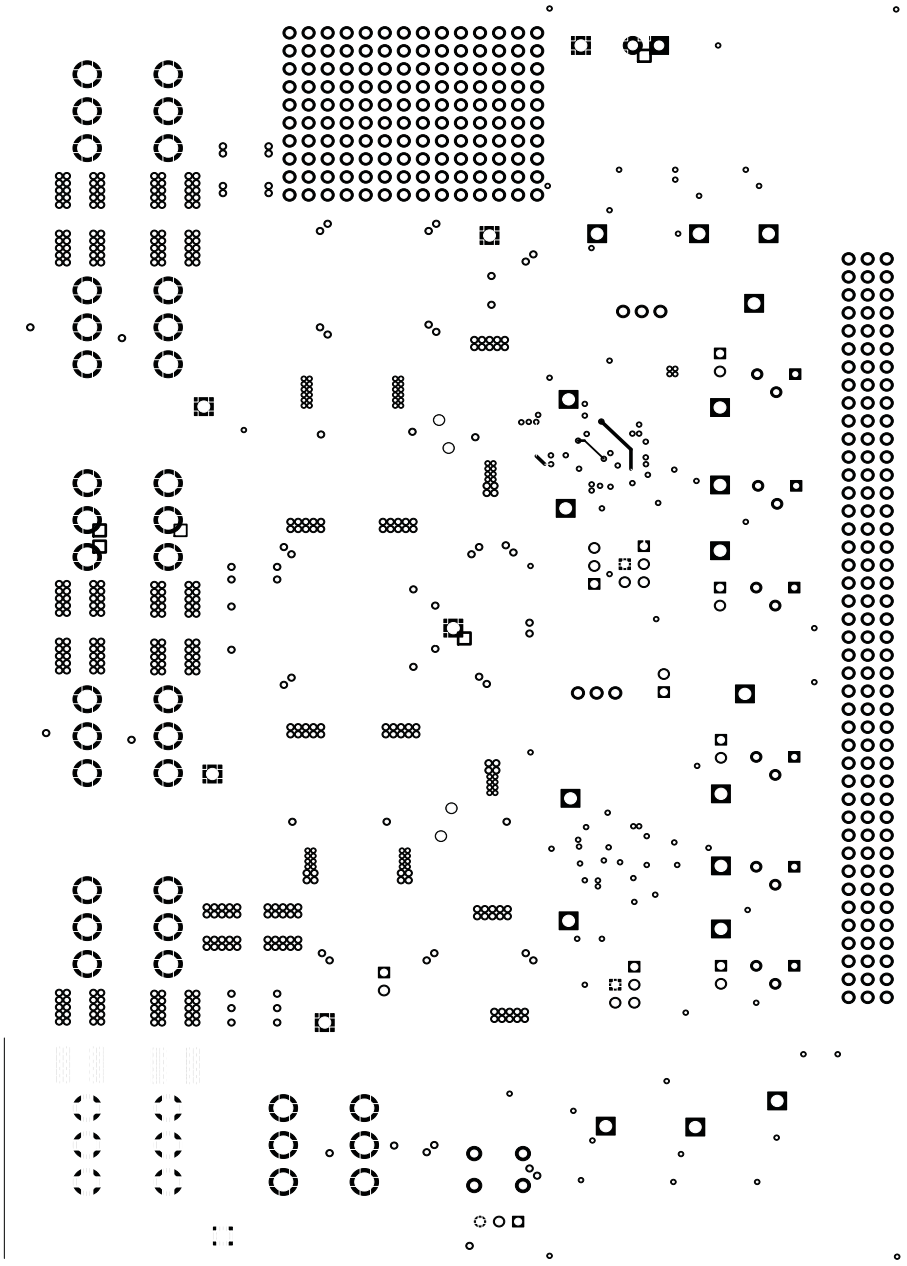


Figure 18. TPS2410EVM Bottom Layer

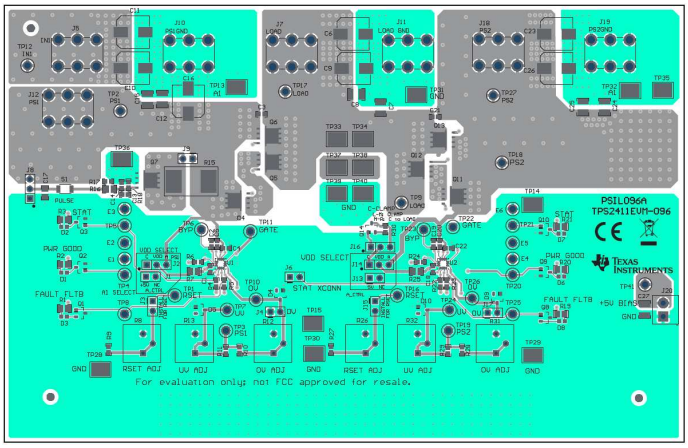


Figure 19. TPS2411EVM-096 Top Overlay

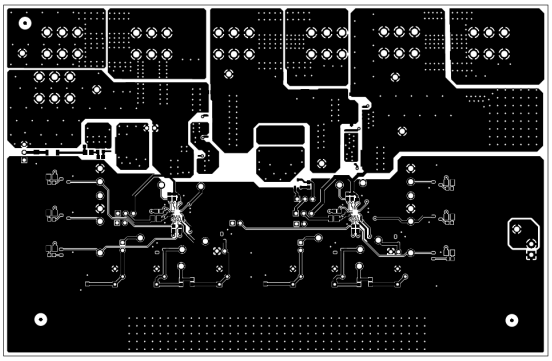


Figure 20. TPS2411EVM-096 Top Layer

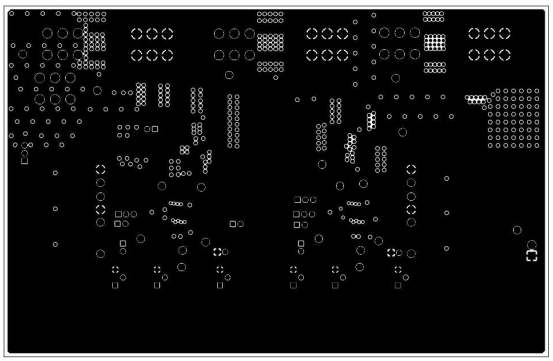


Figure 21. TPS2411EVM-096 Internal Layer 1

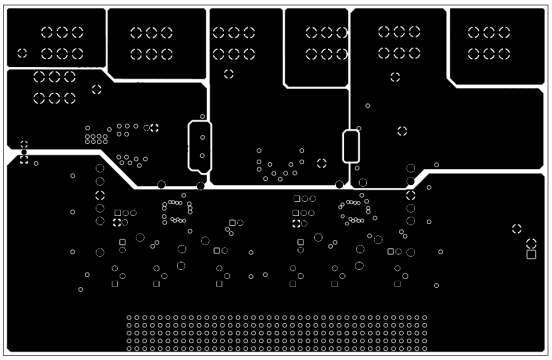


Figure 22. TPS2411EVM-096 Internal Layer 2

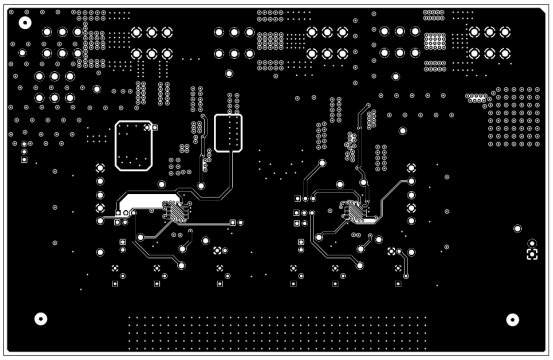


Figure 23. TPS2411EVM-096 Bottom Layer

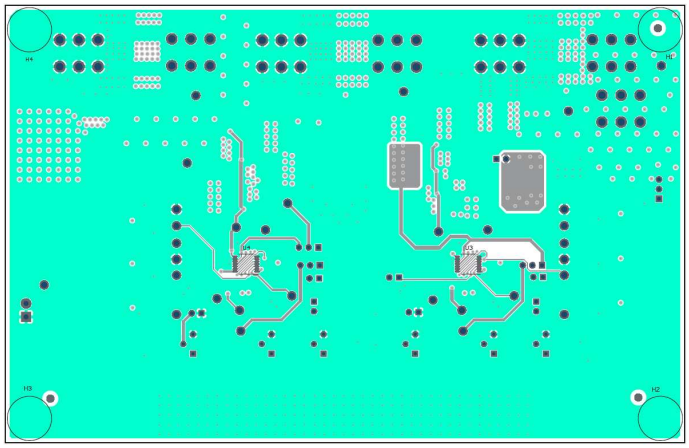


Figure 24. TPS2411EVM-096 Bottom Overlay

7 List of Materials

Table 7. HPA204E1 List of Materials(1) (2) (3) (4)

COUNT	RefDes	Description	Size	Part Number
2	C1, C18	Capacitor, ceramic, 25 V, 0.01 μF, X7R, 20%	0603	STD
1	C13	Capacitor, ceramic, 16 V, 0.1 μF, X5R, 20%	0603	STD
0	C14	Capacitor, ceramic, 25 V, X5R, 10%	0603	Do Not Populate (DNP)
1	C17	Capacitor, ceramic, 25 V, 1 μF, X5R, 20%	0805	ECJ2FB1E105M
2	C2, C19	Capacitor, ceramic, 50 V, 2200 pF, X7R, 10%	0603	STD
0	C3, C4, C21, C22	Capacitor, ceramic, 25 V, 1 nF_DNP, X7R, 10%	0603	STD
2	C5, C20	Capacitor, ceramic, 25 V, 100 μF, 100 pF, X7R, 10%	0603	STD
7	C6, C9–C11, C16, C23, C26	Capacitor, OSCON, SM, 100 μF, 20 V, 20%	G-Case	20SVP100M
7	C7, C8, C12, C15, C24, C25, C27	Capacitor, ceramic, 25 V, 22 μF, X5R, 20%	1210	ECJ4YB1E226M100M
6	D1–D3, D6–D8	Diode, LED, green	0.114 × 0.049 inch	LN1371G
4	D4, D5, D9, D10	Diode, zener, 4.3 V, 350 mW	SOT-23	BZX84C4V3T
0	E1–E6	Pad, TH, DNP	0.038 inch	
8	J1, J3, J4, J6, J9, J13, J15, J17	Header, 2 pin, 100-mil spacing, (36-pin strip)	0.100 inch × 2	PTC36SAAN
4	J2, J8, J14, J16	Header, 3 pin, 100-mil spacing, (36-pin strip)	0.100 inch × 3	PTC36SAANl
1	J20	Terminal block, 2 pin, 6 A, 3 mm to 5 mm	0.27 × 0.25 inch	ED1514
7	J5, J7, J10–J12, J18, J19	Screw terminal, 30 A	0.470 × 0.470 inch	8196-x
2	Q1, Q8	MOSFET, P-channel, 60 V, 90 mA, 14 Ω	SOT23	ZVP3306F0
1	Q14	Trans, P-channel, JFET, -30 V	SOT-23	SST270
0	Q15–Q17, Q21–Q23	MOSFET, N-channel, paceholde	SO8	DNP
0	Q18–Q20, Q24–Q26	MOSFET, N-channel, placeholder	DPAK	DNP
4	Q2, Q3, Q9, Q10	MOSFET, N-channel, 100 V, 0.17 A, 6 Ω	SOT23	BSS123c
0	Q4, Q5, Q11, Q12	MOSFET, N-channel, 30 V, 260 A, 3 mΩ	SMD-220	IRL3713SPBF
3	Q6, Q7, Q13	MOSFET, N-channel, 30 V, 260 A, 3 mΩ	SMD-220	IRL3713SPBFV
2	R1, R19	Resistor, chip, 10 Ω, 1/10 W, 5%	0805	STD
4	R12, R13, R31, R32	Potentiometer, 3/8 cermet, single turn, flat, 50 kΩ	0.375 sq inch	3386P-50K
1	R15	Resistor, Power Metal Strip, 1Ω, 5 W, 1%	4527	WSR5 1R0 1% R86
1	R16	Resistor, chip, 10 Ω, 1/16 W, 1%	0603	STD
2	R17, R30	Resistor, chip, 1 kΩ, 1/16 W, 1%	0603	STD
1	R18	Resistor, chip, 2 kΩ, 1/10 W, 5%	0603	STD
4	R2, R3, R20, R21	Resistor, chip, 270 Ω, 1/16 W, 1%	0603	STD
0	R4, R22	Resistor, chip, 10 kΩ_DNP, 1/16 W, 1%	0603	STD
8	R5, R6, R10, R11, R23, R24, R28, R29	Resistor, chip, 10 kΩ, 1/16 W, 1%	0603	STD

(1) These assemblies are ESD sensitive, ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

Table 7. HPA204E1 List of Materials[1] [2] [3] [4] (continued)

COUNT	RefDes	Description	Size	Part Number
2	R7, R25	Resistor, chip, 10 Ω, 1/16 W, 1%	0603	STD
2	R8, R26	Potentiometer, 100 kΩ, 3/8 cermet, single turn, flat	0.375 sq inch	3386P-50K
0	R9, R27	Resistor, chip, 40.2 kΩ_DNP, 1/16 W, 1%	0603	STD
1	S1	Switch, 1P1T, 20 mA, 15 V	0.240 × 0.256	EVQPAD04M
2	SH1, SH2	Short jumper		
25	TP1–TP12, TP16–TP27, TP41	Test point, white, thru hole	0.125 × 0.125 inch	5012
10	TP13–TP15, TP28–TP32, TP35, TP36	Test point, SM, 0.150 × 0.090	0.185 × 0.135 inch	5016
0	TP33, TP34, TP37–TP40	Test point, SM, 0.150 × 0.090	0.185 × 0.135 inch	5016_DNP
2	U1, U2	IC, N+1 Supply and Voltage OR Controller	PW14	TPS241xPW
0	U3, U4		PW8	DNP
1	—	PCB, 7 In × 4.25 In x 0.3 In		HPA204

Table 8. PSIL096 List of Materials

COUNT	RefDes	Description	Package Reference	Part Number
2	C1, C18	Capacitor, ceramic, 50 V, 0.01 μF, X7R, 10%	0603	CL10B103KB8NCNC
1	C13	Capacitor, ceramic, 25 V, 0.1 μF, X5R, 10%	0603	885012206071
0	C14	Capacitor, ceramic, 50 V, 0.022 μF, X7R, 10%	0603	C0603X223K5RACTU
1	C17	Capacitor, ceramic, 25 V, 1 μF, X5R, 10%	0805	08053D105KAT2A
2	C2, C19	Capacitor, ceramic, 50 V, 3300 pF, X7R, 10%	0603	885012206086
0	C3, C4, C21, C22	Capacitor, ceramic, 50 V, 1 nF, X7R, 10%	0603	885012206083
2	C5, C20	Capacitor, ceramic, 50 V, 220 pF, X7R, 10%	0603	C0603C221K5RACTU
7	C6, C9–C11, C16, C23, C26	Capacitor, Aluminium Polymer, SM, 100 μF, 20 V, 20%	G-Case	20SVP100M
7	C7, C8, C12, C15, C24, C25, C27	Capacitor, ceramic, 25 V, 22 μF, X7R, 10%	1210	CL32B226KAJNFNE
6	D1–D3, D6–D8	Diode, LED, green	1.6x0.8mm	LTST-C193KGKT-5A
4	D4, D5, D9, D10	Diode, zener, 4.3 V, 300 mW	SOT-23	BZX84C4V3-7-F
0	E1–E6	Pad, TH, DNP	Black Multipurpose Testpoint	5011
8	J1, J3, J4, J6, J9, J13, J15, J17	Header, 2 pin, 100-mil spacing, (36-pin strip)	Header, 2 PIN, 100mil, Tin	PEC02SAAN
4	J2, J8, J14, J16	Header, 3 pin, 100-mil spacing, (36-pin strip)	Header, 3 PIN, 100mil, Tin	PEC03SAAN
1	J20	Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS
7	J5, J7, J10–J12, J18, J19	Screw terminal, 30 A, TH	12.9x6.3x7.9 mm	8199
2	Q1, Q8	MOSFET, P-channel, -50 V, -130 mA	SOT23	BSS84-7-F
1	Q14	Trans, P-channel, JFET, -30 V, -15 mA	SOT-23	MMBFJ270
4	Q2, Q3, Q9, Q10	MOSFET, N-channel, 100 V, 0.17 A	SOT23	BSS123
0	Q4, Q5, Q11, Q12	MOSFET, N-channel, 30 V, 100 A	DNK0008A	CSD17573Q5B
3	Q6, Q7, Q13	MOSFET, N-channel, 30 V, 100 A	DNK0008A	CSD17573Q5B
4	R5, R6, R23, R24	Resistor, chip, 10.2 kΩ, 1/10 W, 1%	0603	CRCW060310K2FKEA

Table 8. PSIL096 List of Materials (continued)

COUNT	RefDes	Description	Package Reference	Part Number
2	R8, R26	Potentiometer, 0.5 W, single turn, flat,100 kΩ	375x190x375mil	3386P-1-104LF
2	R1, R19	Resistor, chip, 270 Ω, 1/8 W, 5%	0805	CRCW0805270RJNEA
4	R12, R13, R31, R32	Potentiometer, 0.5 W, single turn, flat, 50 kΩ	375x190x375mil	3386P-1-503LF
1	R15	Resistor, Power Metal Strip, 1Ω, 2 W, 1%	4527	WSR21R000FEA
3	R7, R16, R25	Resistor, chip, 10 Ω, 1/10 W, 0.1%	0805	CRT0805-BY-10R0ELF
2	R17, R30	Resistor, chip, 1 kΩ, 1/16 W, 1%	0603	RC0603FR-071KL
1	R18	Resistor, chip, 2 kΩ, 1/10 W, 5%	0603	RC0603JR-072KL
4	R2, R3, R20, R21	Resistor, chip, 270 Ω, 1/8 W, 5%	0805	CRCW0805270RJNEA
0	R4, R22	Resistor, chip, 10.2 kΩ, 1/10 W, 1%	0603	CRCW060310K2FKEA
4	R10, R11, R28, R29	Resistor, chip, 10 kΩ, 1/10 W, 1%	0603	ERJ-3EKF1002V
0	R9, R27	Resistor, chip, 40.2 kΩ, 1/10 W, 1%	0603	ERJ-3EKF4022V
1	S1	Switch, 1P1T, 50 mA, 12 V	3x1.6x2.5mm	B3U-1000P
2	SH1, SH2	Short jumper		
25	TP1–TP12, TP16–TP27, TP41	Test point, white, thru hole	0.125 × 0.125 inch	5012
10	TP13–TP15, TP28–TP32, TP35, TP36	Test point, SM, 0.150 × 0.090	0.185 × 0.135 inch	5016
0	TP33, TP34, TP37–TP40	Test point, SM, 0.150 × 0.090	0.185 × 0.135 inch	5016
2	U1, U2	IC, N+1 Supply and Voltage OR Controller	RMS14	TPS2411RMS
0	U3, U4	IC, N+1 Supply and Voltage OR Controller	PW14	TPS2410PW
1	—	Printed Circuit Board		PSIL096

Revision History

Changes from A Revision (February 2012) to B Revision	Page
• Updated the *Schematics* section	11
• Updated the *EVM Assembly Drawings and PCB Layout* section	16
• Updated the *List of Materials* section	24

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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