TPS65086100 User's Guide for NXP LS1043A

This user's guide describes an example of how to program the one-time programmable (OTP) memory banks of the PMIC *TPS65086100* to power the NXP QorIQ® Layerscape family of LS10XXA processors. This document is intended to be paired with the *TPS65086100 OTP Generator for LS1043A* for programming the part.

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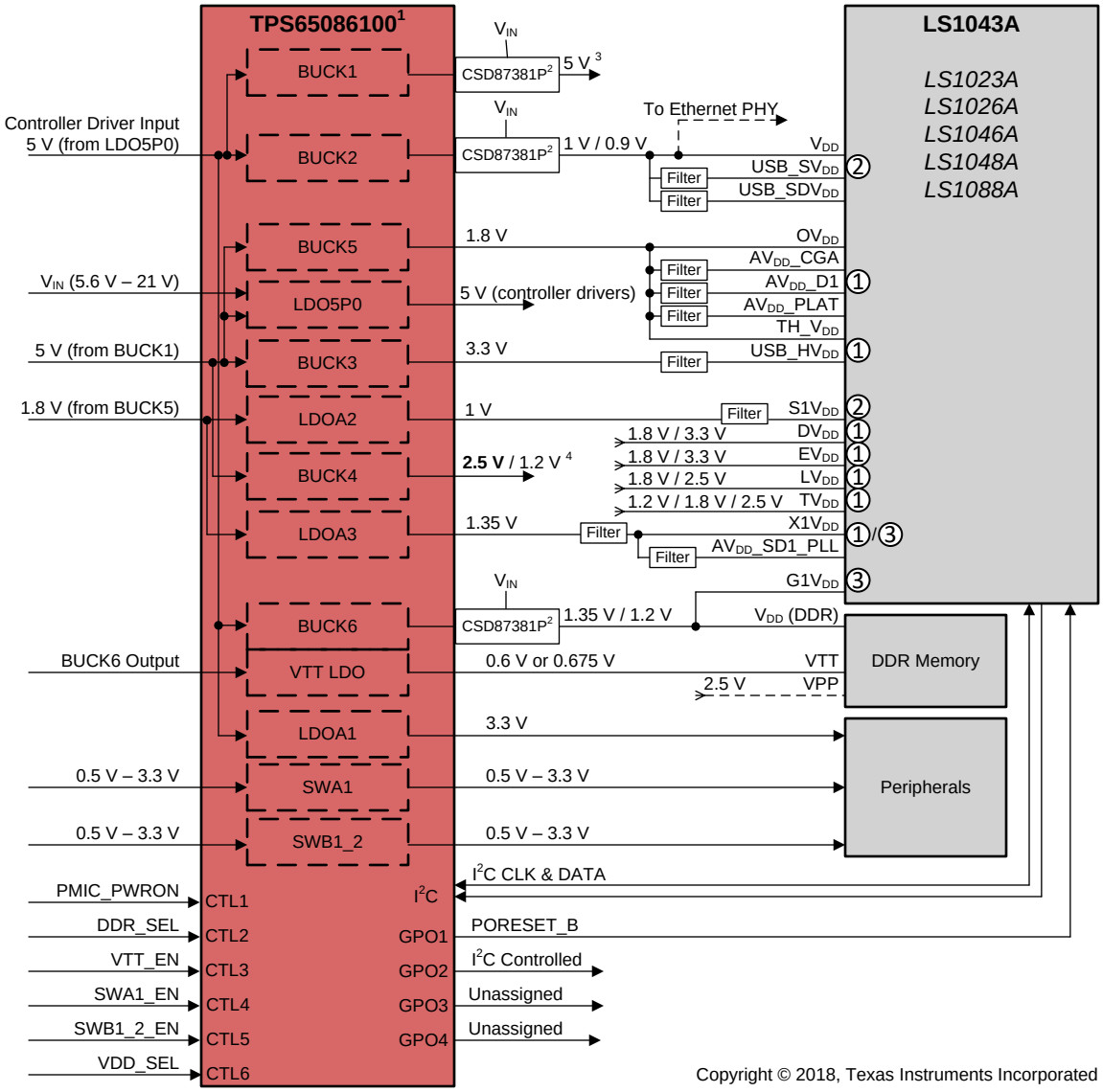
1 Introduction

This document provides typical settings to program the OTP of PMIC TPS65086100 to work with the NXP QorIQ® Layerscape family of processors. While the examples here highlight the *LS1043A*, these settings and configurations can be applied to the *LS1023A*, *LS1026A*, *LS1046A*, *LS1048A*, and *LS1088A* with minor adjustments. This document includes an example of a power map, default voltage settings, power-up sequence, and power-down sequence. Some guidance on connection with the system are also provided. This user's guide does not provide details about the power resources, external components, or functionality of the device. For such information, see the full specification in the device datasheet.

2 Power Map

The TPS65086100 device can be paired with the LS1043A processor and other processors in its family. Figure 1 shows a typical power map for the TPS65086100 device in conjunction with the LS1043A.



(1) The TPS65086100 part will need to be programmed with the *OTP Generator*.

(2) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.

(3) Select "external feedback" on the *OTP Generator* for BUCK1 when programming the TPS65086100 to use 5 V as a voltage option.

(4) The 2.5 V here is the default option for BUCK4, but 1.2 V can be chosen if using DDR3L and TV_{DD} = 1.2 V.

Figure 1. TPS65086100 with NXP LS1043A Example Power Map

The voltages DV_{DD}, EV_{DD}, LV_{DD}, and TV_{DD} can be connected if necessary to any of the bucks dependent on their voltage requirements and can be adjusted in the *OTP Generator* file to match to the correct voltages.

Table 1. CTL Pin Functionality

CTL Pin	Functionality	Description
CTL1	PMIC_PWRON	While the CTL1 pin is high, the PMIC performs the basic power-up sequence. Setting the CTL1 pin low turns those rails off.
CTL2	DDR_SEL	The CTL2 pin sets the BUCK6 ($G1V_{DD}$) voltage. For 1.35 V (DDR3L), tie this pin high (BUCK2). For 1.2 V (DDR4), tie this pin to ground.
CTL3	VTT_EN	The CTL3 pin is the pin-controlled enable for the VTT LDO regulator. If the VTT LDO regulator is not needed, connect the CTL3 pin to ground. If the VTT LDO regulator is used, tie the CTL3 pin to a regulator output to enable it during the sequence.
CTL4	SWA1_EN	The CTL4 pin is the pin-controlled enable for the SWA1 load switch. The CTL4 pin can be connected to ground if the SWA1 load switch is not used or if using I^2C to enable or disable the rail.
CTL5	SWB1_2_EN	The CTL5 pin is the pin-controlled enable for SWB1_2 load switch. Can be connected to GND if SWB1_2 is not used or if using I^2C to enable or disable the rail.
CTL6	VDD_SEL	The CTL2 pin sets the BUCK2 (VDD) voltage. For 1.0 V, tie this pin high. For 0.9 V, tie this pin to ground.

NOTE: These CTL pin settings are for programming the part from the *OTP Generator*. They are used to implement the power map shown in Figure 1.

3 Block Diagram

Section 3 shows the labeled block diagram for the TPS65086100 device.

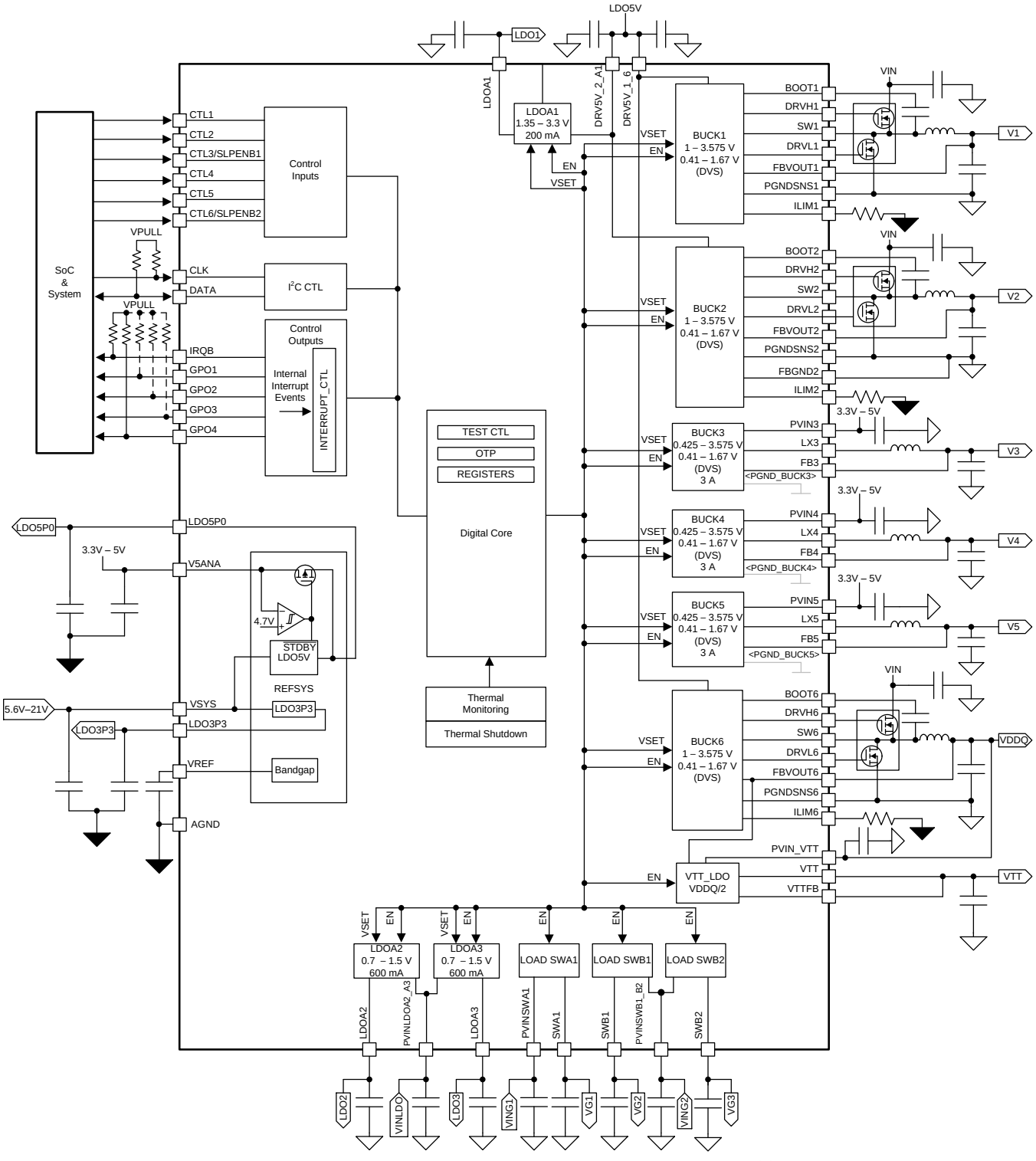


Figure 2. TPS65086100 Example Block Diagram

4 Power-Up Sequence

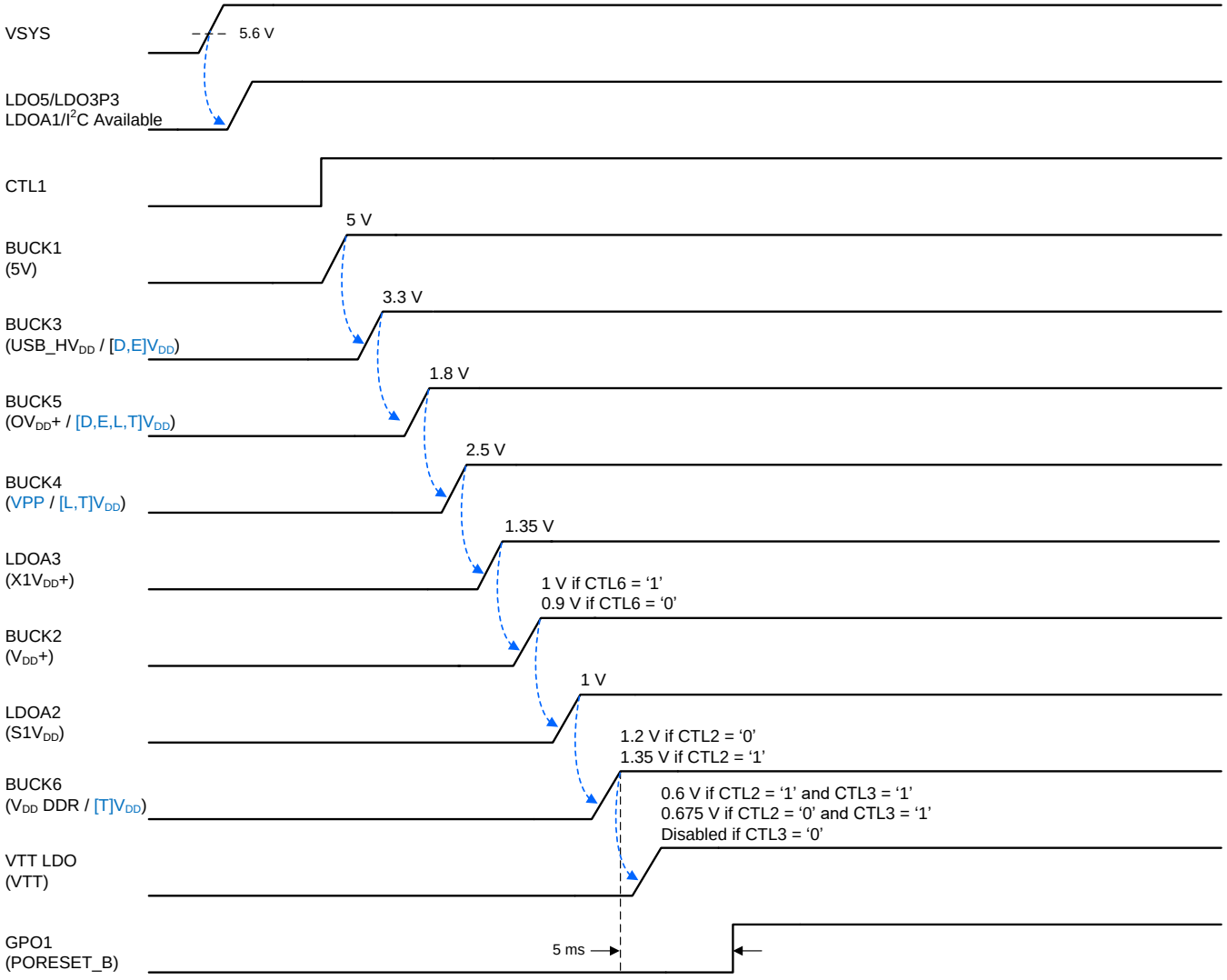


Figure 3. TPS65086100 Power-Up Sequence for LS1043A

SWA1 is enabled by CTL4, and SWB1_2 is enabled by CTL5. They are all independent of CTL1. Many of these rails can be powered up at the same time as per power requirements, but are intentionally staggered to minimize effects on the supply. Items in blue are optional connections dependent on configuration of rails.

5 Power-Down Sequence

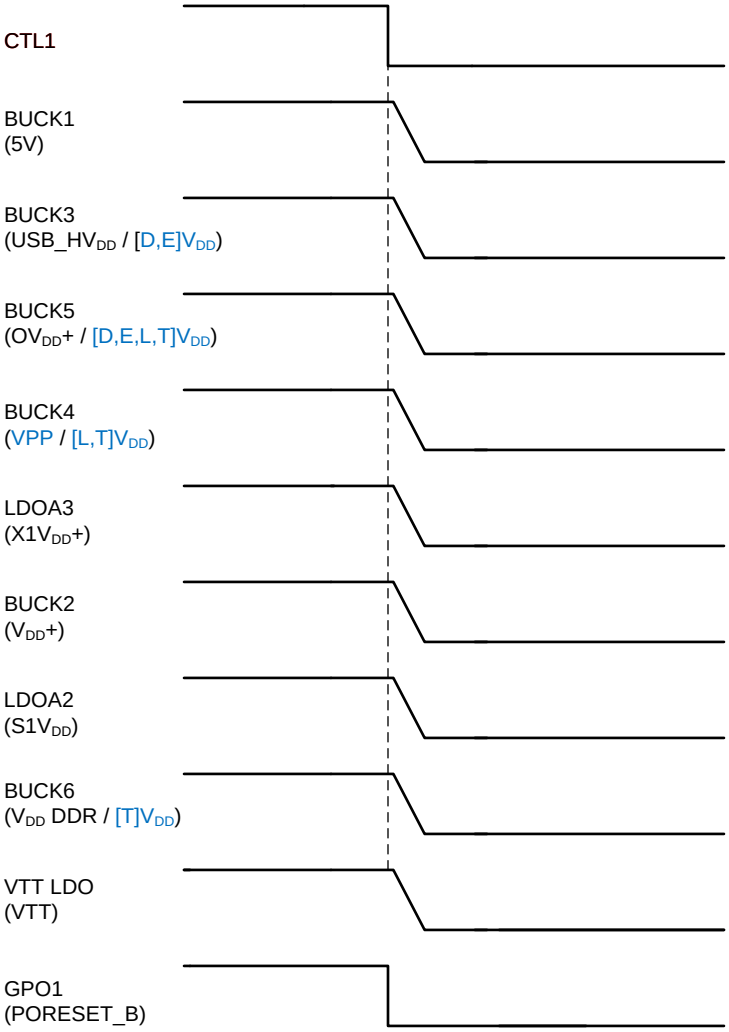


Figure 4. TPS65086100 Power-Down Sequence for LS1043A

All rails assigned to CTL1 power down simultaneously when the CTL1 pin is set low.

6 DDR3L vs DDR4 Considerations

The LS1043A and family of processors can be chosen to be configured with either DDR3L or DDR4. The PMIC can consequently be adjusted to function for either DDR3L or DDR4. While choosing DDR3L, the user should ensure that 1.35 V is selected on BUCK6 (CTL2 = '1') and VTT should be enabled by CTL3. For DDR4, BUCK6 should be selected for 1.2 V (CTL2 = '0') and VPP should be connected to BUCK4. NXP outlines more power considerations on designing in the LS1043A, LS1046A, and LS1088A processors which can be downloaded from the *QorIQ® Layerscape 1088A and 1048A Communications Processor* page.

7 TPS86086100 Ripple and Transient Performance

The *LS1043A Design Checklist* provides recommendations for supply filtering to ensure that PMICs will be within the recommended operating conditions. The datasheet for the LS1043A highlights +5%/-3% for the 1.0 V rails and ±5% for all other rails. The DC ripple tests were performed on BUCK1 (5 V), BUCK2 (1.0 V), and BUCK6 (1.35 V), while load transient tests were performed on BUCK2 and BUCK6. The V_{SYS} rail was powered by 12 V as recommended in the block diagram. As per NXP recommendations a 5 A DC load was used for ripple testing on BUCK2 and BUCK6, a 3 A DC load was used for BUCK1, and a load transient of 5 A to 10 A with a rise of 7 A/µs was applied for transient testing.

These tests were performed on a TPS650860EVM with modifications made to ensure proper supply filtering. A TPS65086100 was programmed with the *OTP Generator* and installed on U1. In addition, four 22 µF ceramic capacitors were installed at C40 - C43. Five 22 µF ceramic capacitors were installed at positions C68 - C70 (stacked to fit). The 220 nH inductor at L2 was replaced with a 470 nH inductor. To configure BUCK1 for 5V from external feedback for the EVM, R24 was replaced with a 294 kΩ resistor and R25 with a 25.5 kΩ resistor. On this board, C37 was also removed and placed onto C71. A 2.2 µH inductor was also placed on L1.

7.1 BUCK1 Ripple Performance

For BUCK1, a 2.2 µH inductor and a total of 194.2 µF of capacitance (1x 150 µF polymer, 2x 22 µF ceramic, 2x 0.1 µF ceramic) was used and is at least recommended for proper supply filtering.

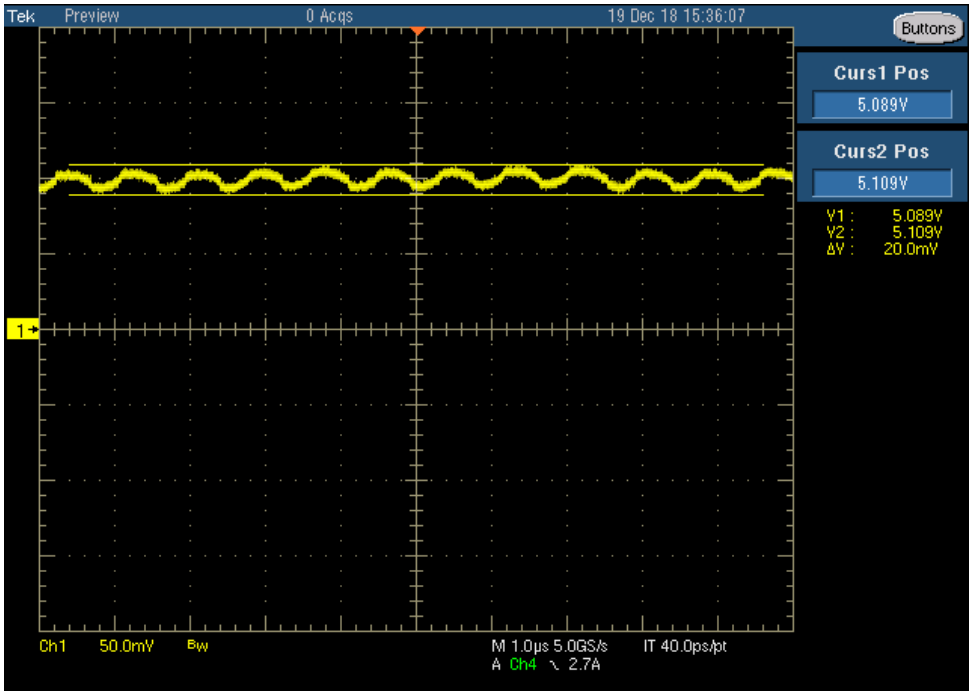


Figure 5. BUCK1 DC Ripple

Table 2. Summary of Results

	Performance Requirement	TPS65086100 Performance
DC Ripple (Pk-Pk)	500 mV	20.0 mV

7.2 BUCK2 Ripple and Load Transient Performance

For BUCK2, a 470 nH inductor and a total of 354.2 µF of capacitance (1x 150 µF polymer, 2x 47 µF ceramic, 5x 22 µF ceramic, 2x 0.1 µF ceramic) was used and is at least recommended for proper supply filtering. According to the LS1043A datasheet, this rail should be within +5%/-3% of 1.0 V (+50 mV/-30 mV). Transient tests were performed with persistent captures of 100 samples.

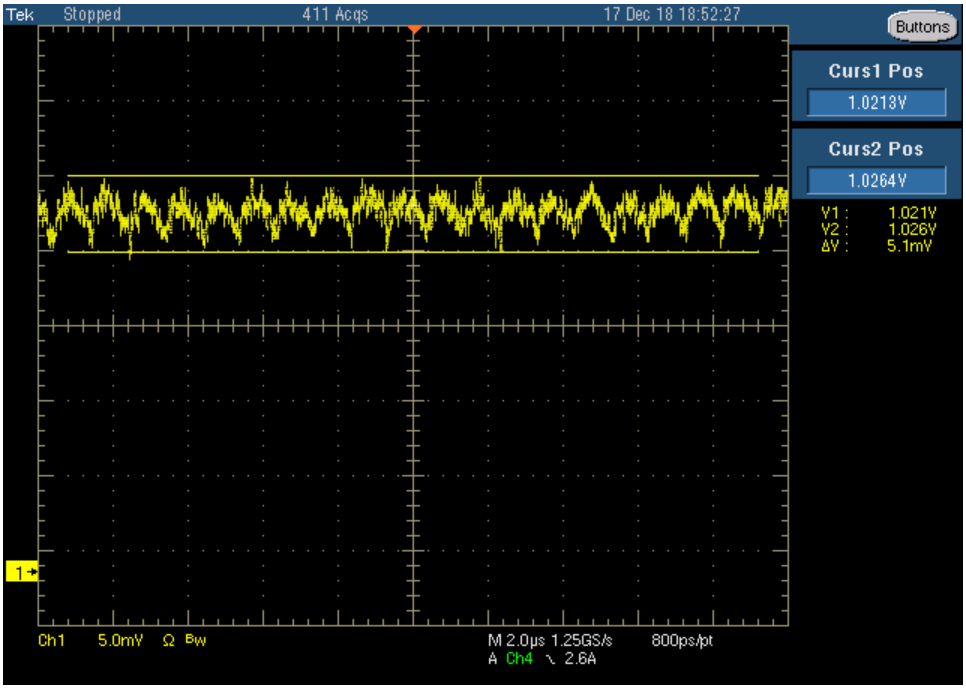


Figure 6. BUCK2 DC Ripple

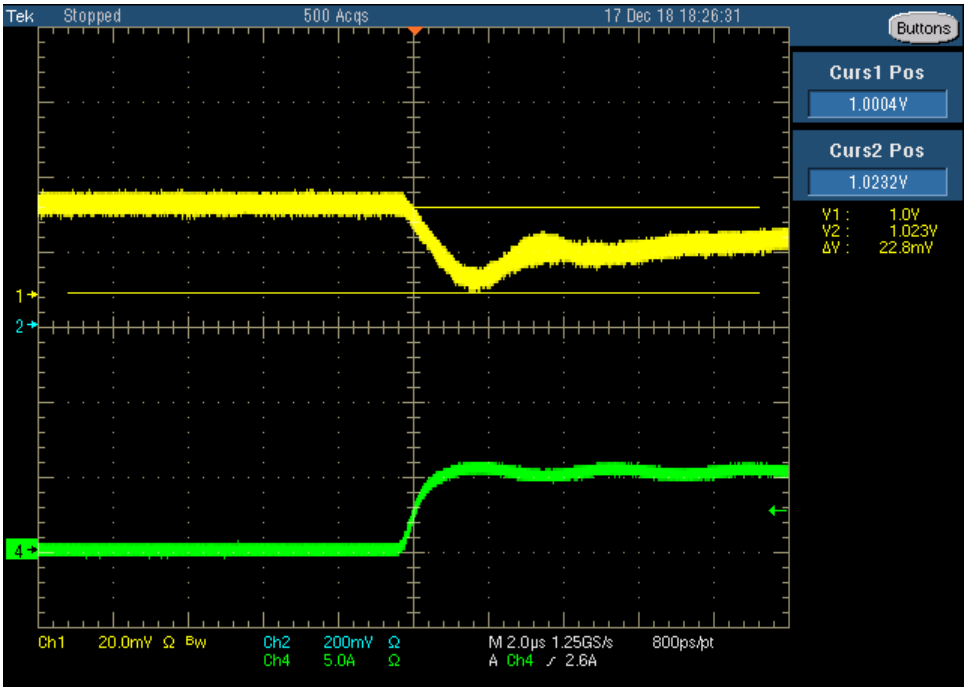


Figure 7. BUCK2 Load Transient Rising Edge

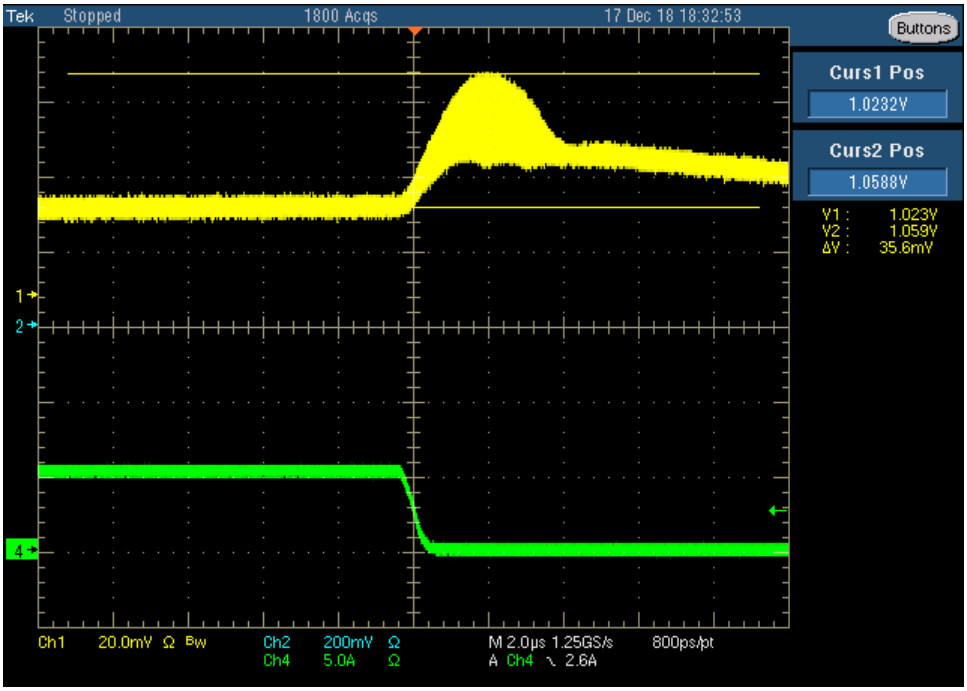


Figure 8. BUCK2 Load Transient Falling Edge

Table 3. Summary of Results

	Performance Requirement	TPS65086100 Performance
DC Ripple (Pk-Pk)	80 mV	5.1 mV
Rising Edge (Pk-Pk)	30 mV	22.8 mV
Falling Edge (Pk-Pk)	50 mV	35.6 mV

7.3 BUCK6 Ripple and Load Transient Performance

For BUCK6, a 470 nH inductor and a total of 330.2 µF of capacitance (1x 220 µF ceramic, 5x 22 µF ceramic, 2x 0.1 µF ceramic) was used and is at least recommended for proper supply filtering. According to the LS1043A datasheet, this rail should be within ±5% of 1.35 V (±67 mV). Transient tests were performed with persistent captures of 100 samples.

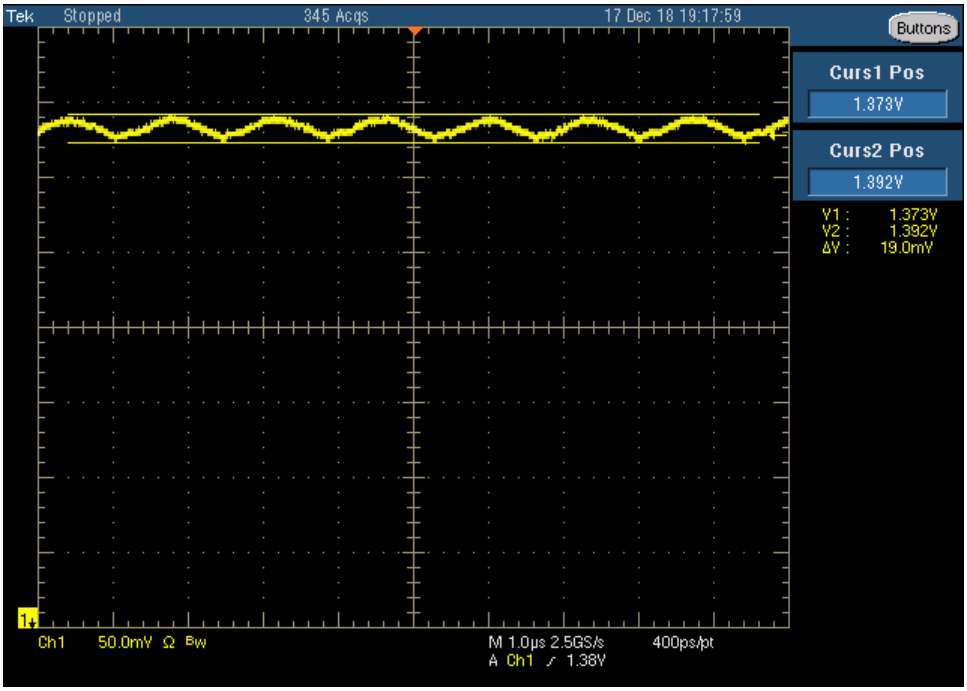


Figure 9. BUCK6 DC Ripple

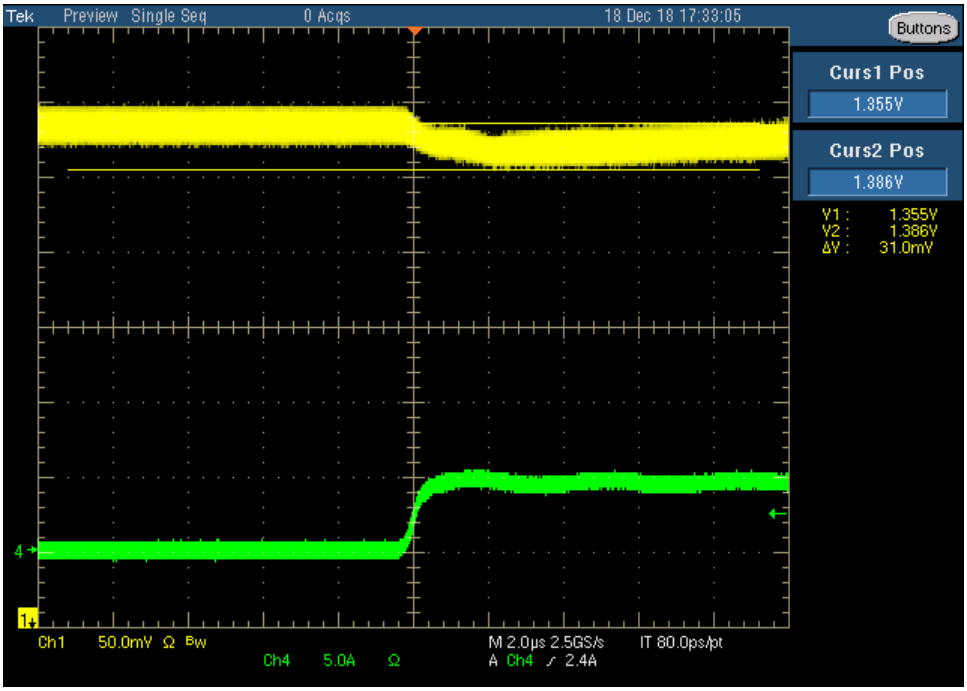


Figure 10. BUCK6 Load Transient Rising Edge

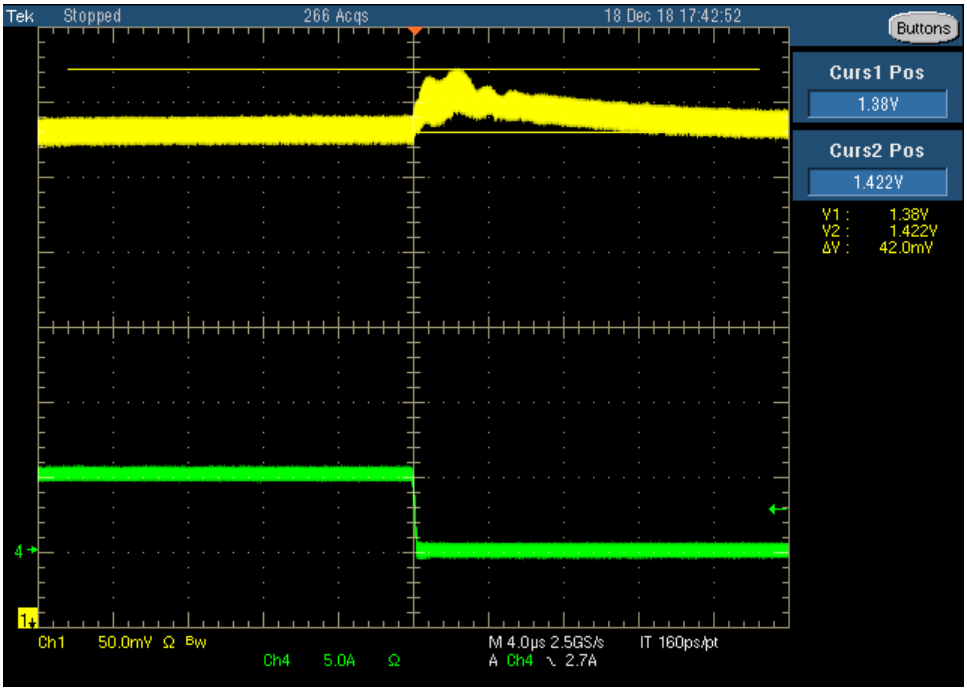


Figure 11. BUCK6 Load Transient Falling Edge

Table 4. Summary of Results

	Performance Requirement	TPS65086100 Performance
DC Ripple (Pk-Pk)	135 mV	19.0 mV
Rising Edge (Pk-Pk)	67 mV	31.0 mV
Falling Edge (Pk-Pk)	67 mV	42.0 mV

8 OTP Summary

All values that can be modified by I^2C after power on are marked by an asterisk (*). For additional details such as GPO power-good inputs, refer to the device register map.

Table 5. TPS65086100 Settings Summary—Buck Regulators

Regulator	Default Voltage	Sleep Voltage	Step Size	SLP Pin	SLP_EN	Power fault Masked	Force PWM
BUCK1	5 V (Ext FB)	N/A	N/A	CTL6	No *	No *	Force PWM
BUCK2	1 V *	0.9 V *	10 mV	CTL6	Yes *	No *	Force PWM
BUCK3	3.3 V *	3.3 V *	25 mV	CTL6	No *	No *	Force PWM
BUCK4	2.5 V *	2.5 V *	25 mV	CTL6	No *	No *	Force PWM
BUCK5	1.8 V *	1.8 V *	25 mV	CTL6	No *	No *	Force PWM
BUCK6	1.35 V * / 1.2 V	1.35 V *	10 mV	CTL6	No *	No *	Force PWM

Table 6. TPS65086100 Settings Summary—General Purpose LDOs

Regulator	Default Voltage	Sleep Voltage	Always-On	SLP Pin	SLP_EN	Power Fault Masked
LDOA1	3.3 *	—	Yes	—	—	No *
LDOA2	1 *	1 *	—	CTL6	No *	No *
LDOA3	1.35 *	1.35 *	—	CTL6	No *	No *

Table 7. TPS65086100 Settings Summary—VTT LDO

Regulator	ILIM Setting	ENABLE Pin	Power Fault Masked
VTT LDO	1.8 A	CTL3	No *

Table 8. TPS65086100 Settings Summary—Load Switches

Regulator	Power-Good Voltage	SWB1_2 Merged	Power Fault Masked
SWA1	1.5 V	—	Yes *
SWB1	1.5 V	Yes	Yes *
SWB2	1.5 V	Yes	Yes *

Table 9. TPS65086100 Settings Summary—GPOs

GPO	Power Good (PG) or I^2C	State	Output Type
GPO1	PG	—	Open Drain
GPO2	I^2C	Low *	Open Drain
GPO3	PG	—	Open Drain
GPO4	PG	—	Open drain

9 I²C Address: Default (0x5E) Register Values

This section describes the values using default I²C address 0x5E. See the *TPS65086100 OTP Memory Programming Guide* for more information on choosing between this address and 0x38 in Section 10.

Table 10. TPS65086100 Default Register Values

Address	Name	Default Value [7:0]
00h	DEVICEID1	8b01000011
01h	DEVICEID2	8b00000001
20h	BUCK1CTRL	8b00000010
21h	BUCK2CTRL	8b01111000
22h	BUCK3DECAY	8b11101000
23h	BUCK3VID	8b11101000
24h	BUCK3SLPCTRL	8b11101000
25h	BUCK4CTRL	8b00001111
26h	BUCK5CTRL	8b00001111
27h	BUCK6CTRL	8b00001111
28h	LDOA2CTRL	8b00001101
29h	LDOA3CTRL	8b00001101
40h	DISCHCTRL1	8b01010101
41h	DISCHCTRL2	8b01010101
42h	DISCHCTRL3	8b00010101
43h	PG_DELAY1	8b00000000
92h	BUCK1SLPCTRL	8b00000010
93h	BUCK2SLPCTRL	8b01100101
94h	BUCK4VID	8b10101000
95h	BUCK4SLPVID	8b10101000
96h	BUCK5VID	8b01110000
97h	BUCK5SLPVID	8b01110000
98h	BUCK6VID	8b10111110
99h	BUCK6SLPVID	8b10111110
9Ah	LDOA2VID	8b01100110
9Bh	LDOA3VID	8b11011101
9Ch	BUCK123CTRL	8b00111111
9Dh	PG_DELAY2	8b00000000
9Fh	SWVTT_DIS	8b01110000
A0h	I2C_RAIL_EN1	8b00000000
A1h	I2C_RAIL_EN2/GPOCTRL	8b00000100
A2h	PWR_FAULT_MASK1	8b01000000
A3h	PWR_FAULT_MASK2	8b00100110
A4h	GPO1PG_CTRL1	8b11111111
A5h	GPO1PG_CTRL2	8b11111111
A6h	GPO4PG_CTRL1	8b11111111
A7h	GPO4PG_CTRL2	8b11111111
A8h	GPO2PG_CTRL1	8b11011111
A9h	GPO2PG_CTRL2	8b11111111
AAh	GPO3PG_CTRL1	8b11111111
ABh	GPO3PG_CTRL2	8b11111111
ACh	MISCSYSPG	8b11111111
ADh	VTT_DISCH_CTRL	8b01011111
AEh	LDOA1_SWB2_CTRL	8b01111101

10 I²C Address: 0x38 Register Values

This section describes the registers that can be accessed using I²C address 0x38. These registers can only be accessed by putting the device into programming mode. See the *TPS65086100 OTP Memory Programming Guide* for more information on putting the device into programming mode. It is recommended to use the *OTP Generator* tool to make changes to these OTP settings. Do not attempt to write a RESERVED R/W bit to the opposite value.

NOTE: There are additional registers not shown that are set by the *OTP Generator* tool.

Table 11. TPS65086100 0x38 Register Values

Address	Name	Default Value [7:0]
02h	OTP_CTRL1	8b00100000
03h	OTP_CTRL2	8b00000000
07h	BUCK1_CTRL_EN1	8b11111111
08h	BUCK1_CTRL_EN2	8b11100011
09h	BUCK1_CTRL_EN3	8b00000000
0Ah	BUCK2_CTRL_EN1	8b01111111
0Bh	BUCK2_CTRL_EN2	8b11000011
0Ch	BUCK2_CTRL_EN3	8b00000000
0Dh	BUCK3_CTRL_EN1	8b11111110
0Eh	BUCK3_CTRL_EN2	8b01100011
0Fh	BUCK3_CTRL_EN3	8b00000000
10h	BUCK4_CTRL_EN1	8b11110111
11h	BUCK4_CTRL_EN2	8b11100011
12h	BUCK4_CTRL_EN3	8b00000000
13h	BUCK5_CTRL_EN1	8b11111011
14h	BUCK5_CTRL_EN2	8b01100011
15h	BUCK5_CTRL_EN3	8b00000000
16h	BUCK6_CTRL_EN1	8b10111111
17h	BUCK6_CTRL_EN2	8b11000111
18h	BUCK6_CTRL_EN3	8b00000000
19h	SWA1_CTRL_EN1	8b11111111
1Ah	SWA1_CTRL_EN2	8b00001111
1Bh	SWA1_CTRL_EN3	8b00000000
1Ch	LDOA2_CTRL_EN1	8b11111101
1Dh	LDOA2_CTRL_EN2	8b01000111
1Eh	LDOA2_CTRL_EN3	8b00000000
1Fh	LDOA3_CTRL_EN1	8b11110111
20h	LDOA3_CTRL_EN2	8b10000011
21h	LDOA3_CTRL_EN3	8b10000000
22h	SWB1_CTRL_EN1	8b11111111
23h	SWB1_CTRL_EN2	8b10001011
24h	SWB1_CTRL_EN3	8b00000000
25h	SWB2_LDOA1_CTRL_EN1	8b11111111
26h	SWB2_LDOA1_CTRL_EN2	8b00000011
27h	SWB2_LDOA1_CTRL_EN3	8b00000000
29h	SLP_PIN	8b11111111
2Ah	OUTPUT_MODE	8b00100111
5Fh	I2C_SLAVE_ADDR	8b00000000

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