



ABSTRACT

The LP876242-Q1 Evaluation Module (EVM) highlights the performance and flexibility of the LP876242-Q1 power management integrated circuit (PMIC) for xWR radar applications. Use this document in conjunction with the Scalable PMIC's GUI User's Guide [SLVUBT8](#) and the LP876242-Q1 Four 8.8-MHz Buck Converters for AWR and IWR MMICs [SNVSC07](#).

	<p>Caution</p>	<p>Caution Hot surface. Contact may cause burns. Do not touch!</p>
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1 Introduction

The LP876242-Q1 power management integrated circuit (PMIC) family is extremely flexible and scalable, providing configurability at the device and system level. At the device level, a single PMIC provides four separate step down converters (BUCK regulators). These BUCK regulators have been tested to conform with the radar specification and are switched at 8.8 MHz switching frequency. The LP876242-Q1 evaluation module (EVM) is both an evaluation and development tool. With the EVM both device level and system level configurability are available through an easy to use graphical user interface (GUI) tool.

2 Getting Started

Only a power supply and the EVM are required to evaluate and test the LP876242-Q1 default configuration under load conditions. To start evaluating the LP876242-Q1 follow the following steps.

1. Connect power to the EVM.
2. Connect the EVM to the host PC through the USB. In the event that the power is provided by the USB cable, apply the appropriate jumper connection to connect +VBUS and VCCA see [Table 3-5](#).
3. Launch the GUI and evaluate.

Terminal J7, labeled VCCA in [Figure 2-1](#), can accept wire gauges up to 14 AWG. The voltage supplied must be within the input range of the device, 2.8 V to 5.5 V. The power supply providing the input to VCCA is required to supply 135 % of the output power. Once power has been supplied to VCCA, the GPIO4 / ENABLE jumper can be used to power on the output rails. The default ON Request for the device is the ENABLE pin which is a level sensitive input. Please refer to [LP876242-Q1 data sheet](#) for more details.

[Figure 2-1](#) shows the top side of the LP876242Q1EVM.

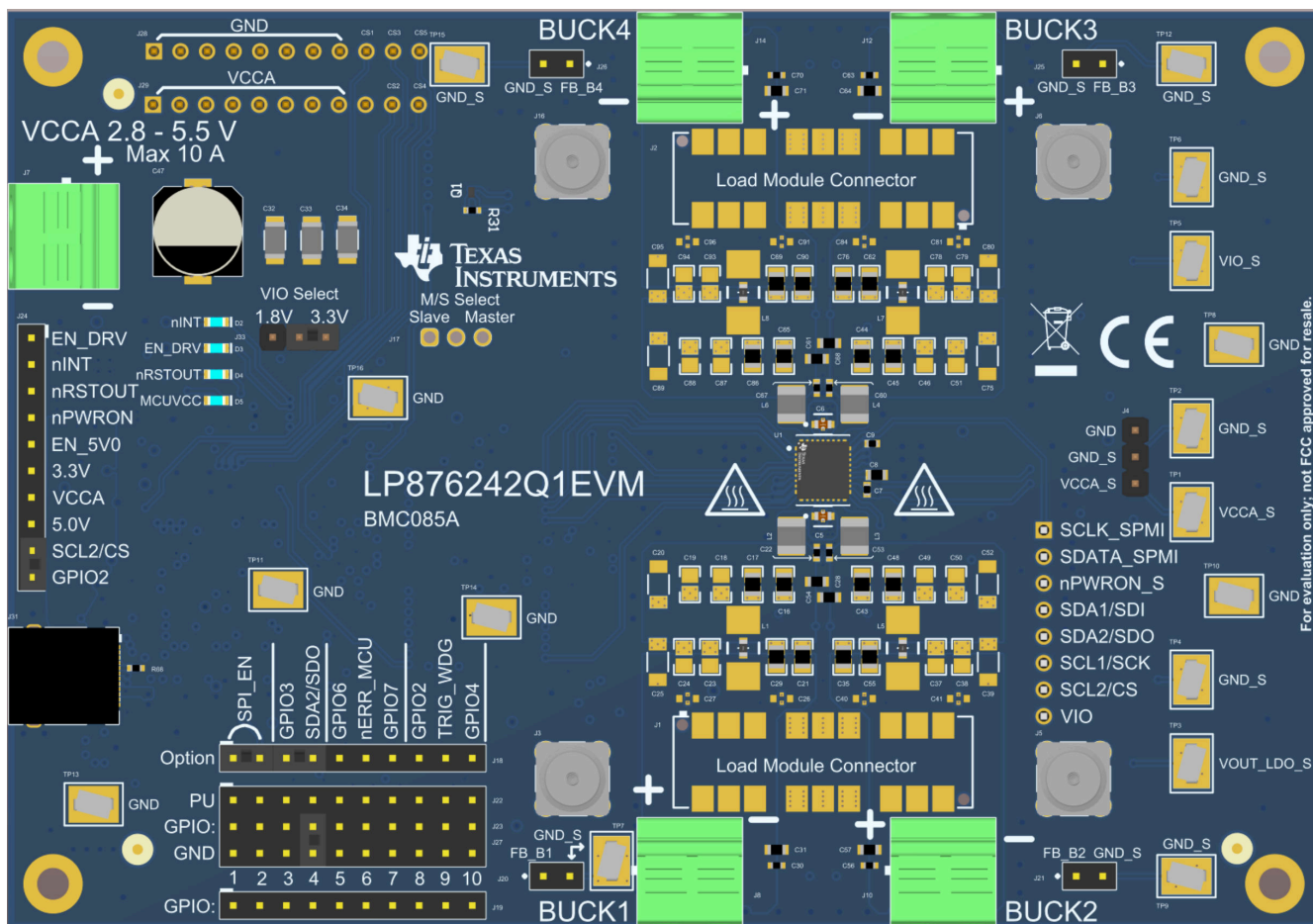


Figure 2-1. EVM Top View

2.1 The GUI Tool

Texas Instruments provides a GUI tool to enable, configure, and evaluate the various features of the LP876242-Q1 with the EVM. Please refer to the GUI User's Guide [SLVUBT8](#) for a more detailed description of this tool.

The GUI runs on most PC platforms and requires an available USB port. The EVM USB connector is type-C and a type-A to type-C cable is provided with the EVM to connect to the host computer. The EVM enumerates as two COM ports and one additional port for the device firmware updates. The GUI uses ACtrl COM port which can be found from the device manager of the operating system. The COM port can be changed from the GUI from Options—Device Settings menu.

A tool for estimating the efficiency of LP876242-Q1 device is also available called PMIC Efficiency Estimator Tool. The tool can be accessed [here](#).

3 EVM Details

The following sections describe the various interfaces for measuring and controlling the configuration. Note: the configurations are in coordination with the settings of the PMIC. It is important to understand that both the EVM configuration and the settings of the PMIC must match. The communication interface can be easily changed using the jumpers on J18 and J24. Please refer to the GUI User's Guide [SLVUBT8](#) on how to update the PMIC communication protocol.

3.1 Terminal Blocks

The terminal blocks are simple push and release terminals which can accommodate wire sizes up to 14 AWG. [Table 3-1](#) lists the terminal blocks found around the perimeter of the EVM. J7, VCCA, is the input voltage for the regulators. The rest of the terminal blocks are for the BUCK outputs.

Table 3-1. Terminal Blocks

Terminal	Designator	Description
VCCA	J7	All Regulator Input, 2.8 V to 5.5 V Range
BUCK1	J8	Buck 1 Output, 2 A Capable
BUCK2	J10	Buck 2 Output, 4 A Capable
BUCK3	J12	Buck 3 Output, 3 A Capable
BUCK4	J14	Buck 4 Output, 3 A Capable

3.2 Test Point Descriptions

Numerous test points are provided to access voltages and signals. Test points marked with _S are designed for sensing voltages only and are not designed to carry large DC currents.

Table 3-2. Test Point Descriptions

Test Point	Device Pin	Description
TP1	VCCA_S	VCCA voltage sense point. Routed from close to the VCCA pin of the LP876242-Q1.
TP2, TP4, TP6, TP7, TP9, TP12, TP15	GND_S	Ground sense points routed from various locations.
TP3	VOUT_LDO_S	Voltage sense point for the internal LDO output voltage.
TP5	VIO_S	VIO voltage sense routed from the VIO pin of the LP876242-Q1.
TP8, TP10, TP11, TP13, TP14, TP16	GND	Solid ground points. Are able to carry larger DC currents.
J20,J21,J25,J26	FB_B1,FB_B2,FB_B3,FB_B4	Buck output voltage sense points.

3.3 Configuration Headers

There are four headers available to configure the EVM function. Header J18, as shown in the silk screen picture in [Figure 3-1](#), is used to configure the EVM to match the settings written to the LP876242-Q1 configuration

registers. J33 is used to select the PMIC IO voltage, either 1.8 V or 3.3 V. The fifth header is J24 which allows VCCA to be powered from the USB connection and the configuration of GPIO2, I2C2 or SPI.



Figure 3-1. EVM Header J18

Table 3-3. Header J18 Description

Option Pins	Configuration	Description	
SPI_EN	Open	I ² C Mode. The signal path for I ² C communication between the MCU and the PMIC is enabled.	
	Closed (Default)	SPI mode. The signal path for SPI communication between the MCU and the PMIC is enabled.	
GPIO3, SDA2/SDO	Open	GPIO mode. GPIO2 from PMIC is connected to PM7 of the MCU through a level translator.	
	GPIO3,SDA2/SDO: Closed (Default)	I ² C Mode (J18 VIO, I2C/SPI: Open)	Q&A Watchdog mode. GPIO3 supports the Q&A Watchdog when PMIC is in the Alternative function and the I ² C mode is selected. This setting is also done on connector J24 by closing GPIO2 to SCL2/CS if I2C2 is wanted to be used.
		SPI mode (J18 VIO, I2C/SPI: Closed)	SPI mode, Chip Select. GPIO2 and GPIO3 supports SPI communication when the PMIC is in the Alternative function. This setting is also done on connector J24 by closing GPIO2 to SCL2/CS if I2C2 is wanted to be used.
GPIO6, nERR_MCU, GPIO7	Open (Default)	GPIO mode. GPIO6 of the PMIC is connected to PP5 of the through a level translator.	
	GPIO6, nERR_MCU Closed	System error count down input signal from the MCU. VIO Select must be 3.3 V. GPIO6 or GPIO7 supports the system error count down from the MCU when the PMIC is in the Alternative function.	
	nERR_MCU, GPIO7 Closed		

Table 3-3. Header J18 Description (continued)

Option Pins	Configuration	Description
GPIO2, TRIG_WDG, GPIO4	Open (Default)	GPIO mode. GPIO7 of the PMIC is connected to PH0 of the through a level translator.
	GPIO2, TRIG_WDG Closed	Trigger signal for trigger mode watchdog. VIO Select must be 3.3 V.
	TRIG_WDG, GPIO4 Closed	GPIO7 or GPIO6 supports the trigger mode watchdog signal when the PMIC is in the Alternative function.

Table 3-4. Header J33 VIO Voltage Select

Configuration	Description
Open	Not Allowed
VIO Select, 3.3 V: Closed (Default)	VIO is 3.3 V.
VIO Select, 1.8 V: Closed	VIO is 1.8 V.

Table 3-5. Header J24, 3.3V/5V, GPIO2/I2C/SPI

Configuration	Description	
3.3V, VCCA: Closed	3.3 V from TLV733P-Q1 (U12) is connected to VCCA. The input for U12 is the 5 V from the USB connection (VBUS). VBUS is not intended to support heavy load conditions. 2 W is the maximum power which can be drawn from the USB. This header configuration is the normal state of EVM.	
EN_5V0, 3.3V, VCCA,5.0V: Open	VBUS, and USB_3V3 are isolated. VCCA is powered from J7.	
EN_5V0,3.3V: Closed	5V from USB port is enabled. 5V regulated supply can be used to power up VCCA.	
VCCA, 5.0V: Closed	5 V from USB Port is connected to VCCA. This supply is not intended to support heavy load conditions Do not draw more than 2 W from the USB.	
SCL2/CS, GPIO2: Open	GPIO mode. GPIO2 of the PMIC is connected to IO2 of the MCU.	
SCL2/CS, GPIO2: Closed (Default)	I ² C mode (J18 SPI_EN: Open)	Q&A Watchdog mode. GPIO2 and GPIO3 supports the Q&A Watchdog when the PMIC is in Alternative function and the I ² C mode selected. This setting is also done on connector J18 by closing GPIO3 to SDA2/SDO if I2C2 is wanted to be used.
	SPI mode (J18 SPI_EN: Closed)	SPI mode, Chip Select. GPIO2 and GPIO3 supports SPI communication when the PMIC is in the Alternative function. This setting is also done on connector J18 by closing GPIO3 to SDA2/SDO.

Note

The PMIC device can be configured for a power good level of 3.3 V or 5.0 V for the VCCA pin. If VCCA_VMON feature is enabled please check that the input voltage is correct and use sense connection to compensate IR voltage drop with heavy load currents. Align the 3.3V/5.0V jumper with the PMIC configuration. The default PMIC configuration supports the whole recommended VCCA voltage range.

3.4 Connectors

Four SMA (J3, J5, J6, J16) connectors are included in the EVM, one for each buck. These connectors can be used for noise and ripple measurements and are DC filtered with 10 μ F capacitors and terminated with 50 Ω resistors. The location of the DC filtering capacitor can be changed to alter the measurement point to be either after or before the second LC filtering stage. The default configuration is that each of the connectors take the measurement after the filter. The corresponding DC capacitor footprints are marked on the bottom side of the PCB as shown in [Figure 3-2](#) and summarized in [Table 3-6](#)

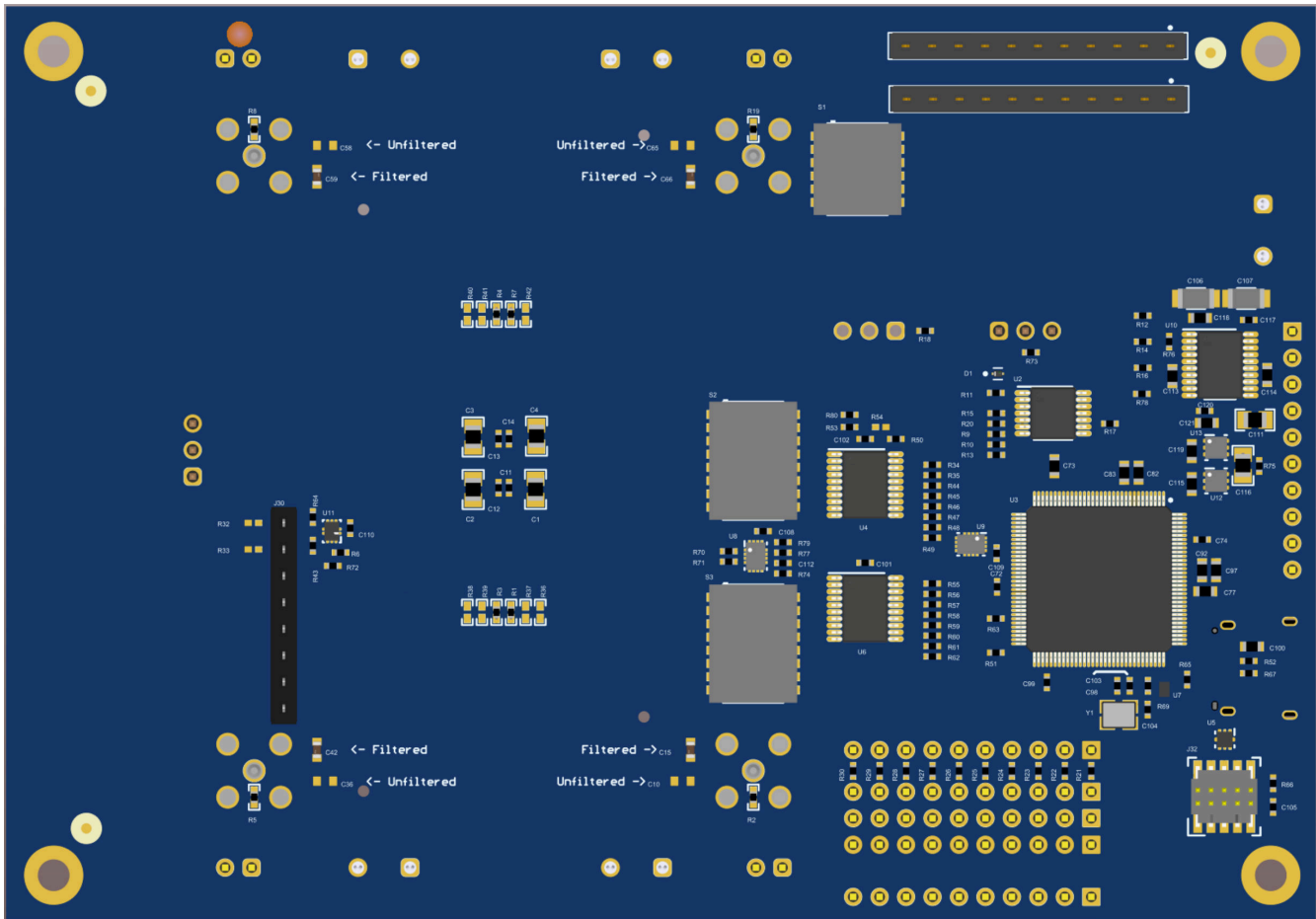


Figure 3-2. EVM Bottom Side

Table 3-6. DC Block

Measurement point	BUCK1	BUCK2	BUCK3	BUCK4
After second LC stage (Filtered) (default)	C15	C42	C59	C66
Before second LC stage (Unfiltered)	C10	C36	C58	C65

Two load module connector footprints are provided, J1 and J2. These connectors are intended to be used with PMICLOADBOARD EVM which is sold separately. The connector components are not populated and the required connectors are shipped with PMICLOADBOARD EVM.

3.5 DIP Switches

There are three DIP switches S1, S2 and S3 on the back side of the PCB. S1 switch can be used for configuring chip select for target device in multi PMIC/stacked use case. S2 and S3 switches allow the user to disconnect the level shifter from the PMIC GPIOs or serial interfaces. The level shifter has pull-ups on the MCU side that can cause unwanted high state on the GPIO signals if configured in high impedance state. See the [Table 3-7](#) for the descriptions of the switches.

Table 3-7. DIP Switches

Switch	Pin	Signal line
S1	1-12	CS5
	2-11	CS4
	3-10	CS3
	4-9	CS2
	5-8	CS1
	6-7	GPIO2
S2	1-16	SDA_I2C1/SDI_SPI
	2-15	SCL_I2C1/SCK_SPI
	3-14	SDA_I2C2/SDO_SPI
	4-13	SCL_I2C2/CS_SPI
	5-12	GPIO1
	6-11	GPIO2
	7-10	GPIO3
	8-9	GPIO4
S3	1-16	GPIO5
	2-15	GPIO6
	3-14	GPIO7
	4-13	GPIO8
	5-12	GPIO9
	6-11	GPIO10
	7-10	Not connected
	8-9	nINT

3.6 EVM Control and GPIO

The EVM has a built-in USB interface based on the MSP432E401Y (U3) to allow the GUI, from the host computer, to communicate with the PMIC. The supply voltage required by the MSP432E401Y is generated automatically by the TLV73333PQDRVRQ1 (U12) and TLV73318PQDRVRQ1 (U13) devices which provides 3.3 V and 1.8 V from USB power, +VBUS. These voltages are available for supplying VIO for the PMIC (selectable from J33). Two SN74GTL2003 level shifters (U4, U6) are used in order to support the use case of the PMIC VIO of 1.8 V (the MCU IO is 3.3 V). In addition to the level shifters, the TS3A5018RSVR (U8) switch is used to apply the pullup voltages to the I²C lines only when the EVM is configured as controller (J17). Additional TS3A5018RSVR (U9) switch is used for SPI enable/disable. The EVM has 4 LEDs to indicate board power, on or off, and some pre-defined PMIC GPOs status. The signals are listed in [Table 3-8](#).

Table 3-8. EVM LED Indicators

LED Designator	Indication
D2	LED is on when nINT is low.
D3	LED is on when EN_DRV is high.
D4	LED is on when nRSTOUT is low.
D5	EVM USB power indicator.

4 Customization

The EVM, in conjunction with GUI tool, provides various degrees of customization. A couple of examples are provided here which can be generalized to a number of functions.

4.1 Changing the Communication Interface

The default settings for communication with the PMIC is SPI. Changing to I²C requires a removal of jumpers from J18, J24 as highlighted in red in Figure 4-1. At J18, the jumper on SPI_EN connects the microcontroller to the SPI bus to which the PMIC is connected. The SPI does not have a device ID and therefore the chip select is used to determine which PMIC receives and responds to commands on the SPI bus.

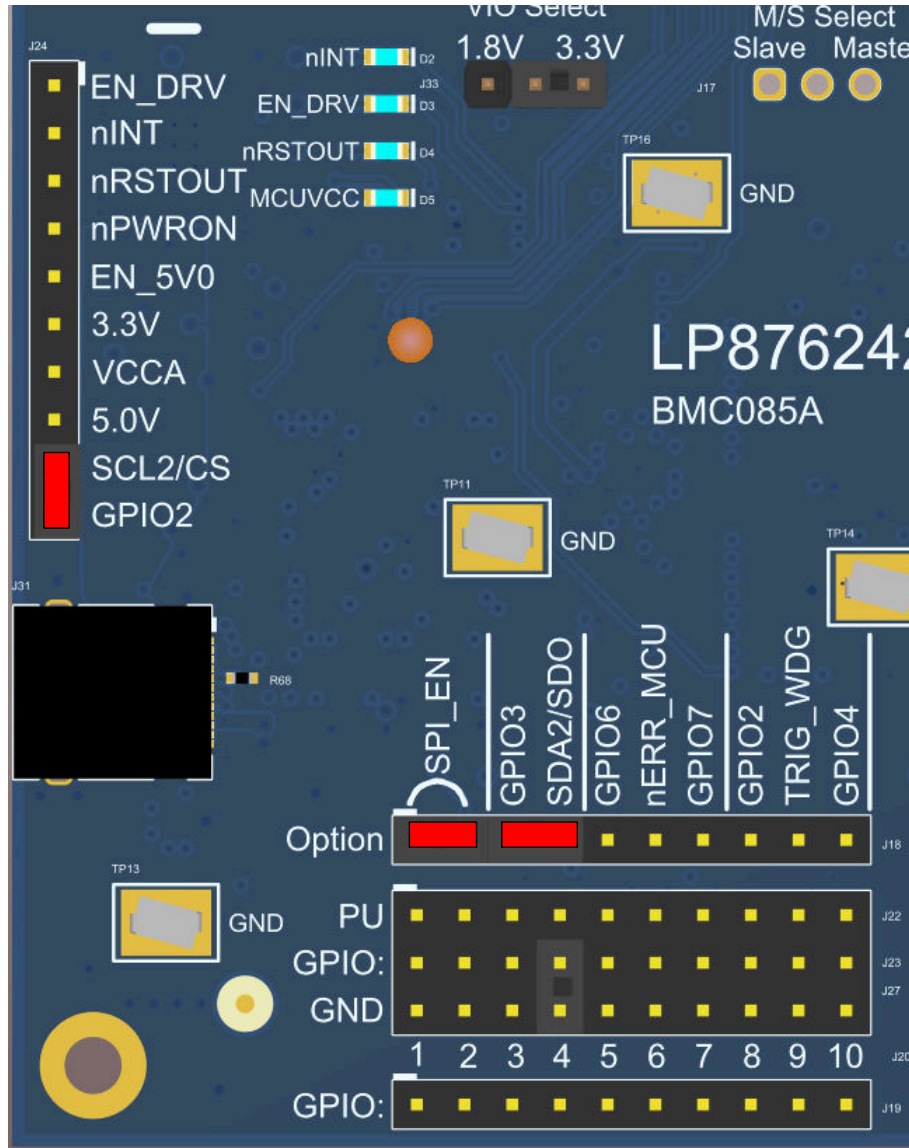


Figure 4-1. Interface Settings for I²C Communication

5 Schematic, Layout, and Bill of Materials

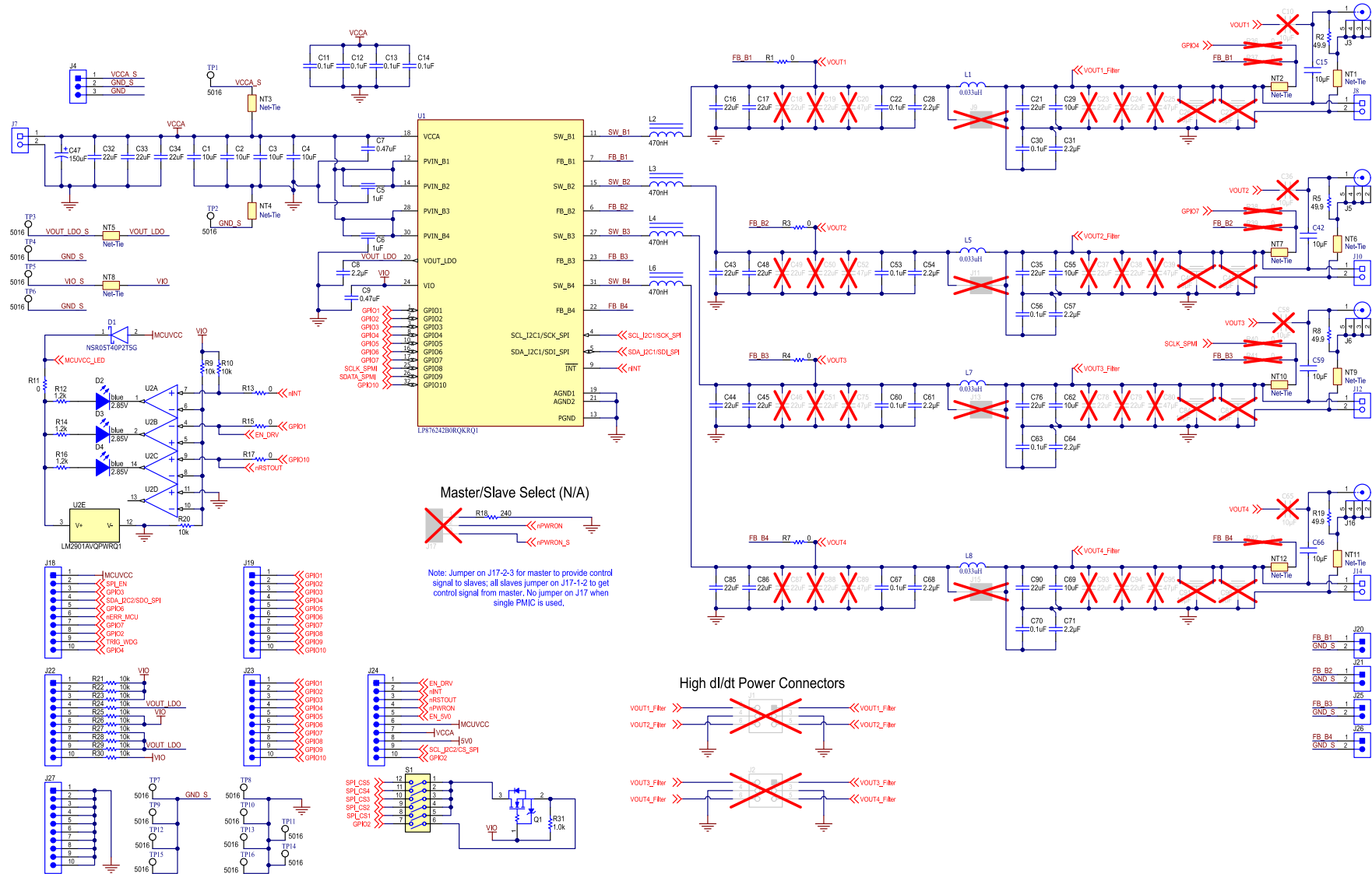


Figure 5-1. Main Schematic Page

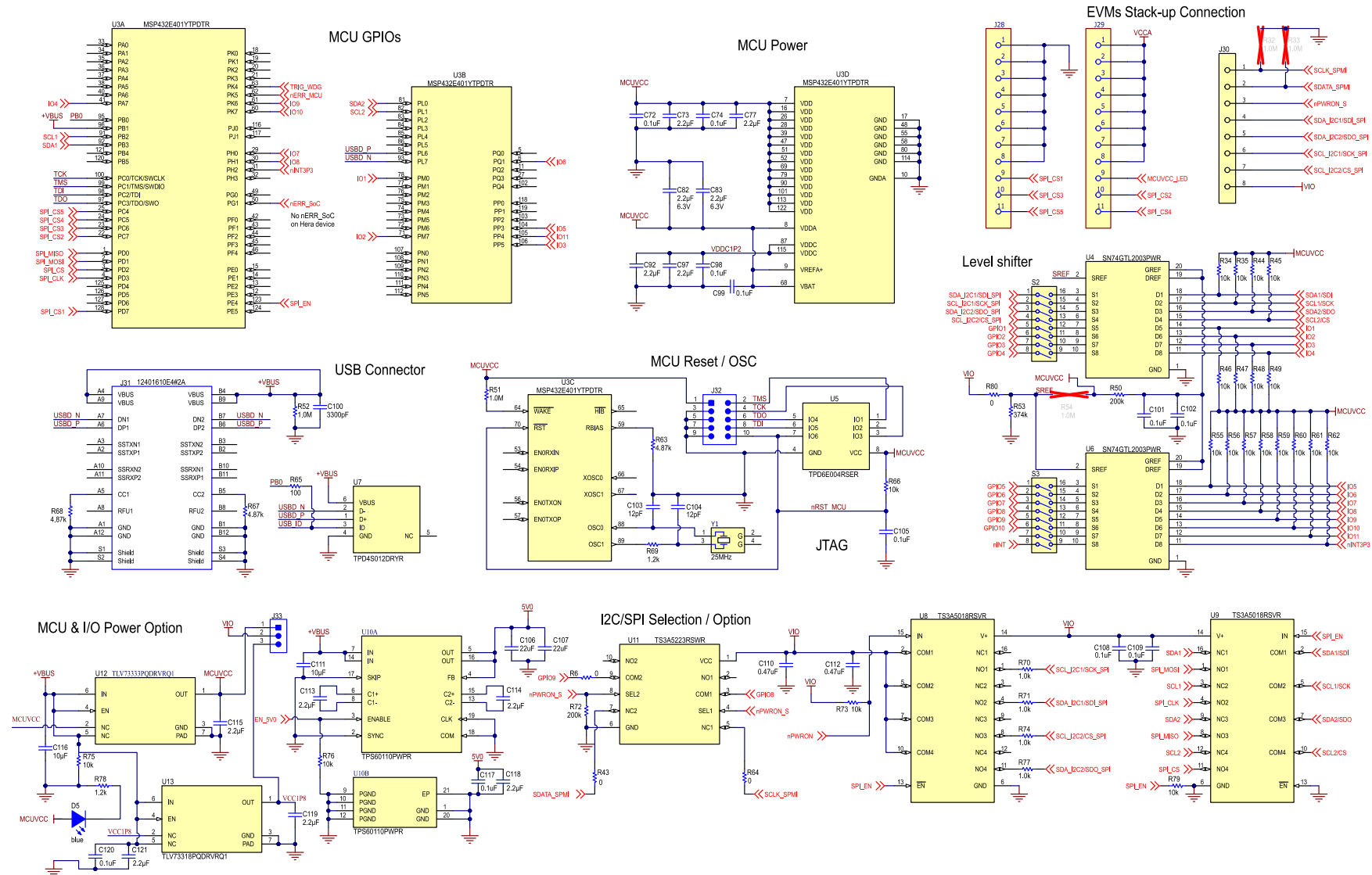


Figure 5-2. MCU Schematic Page

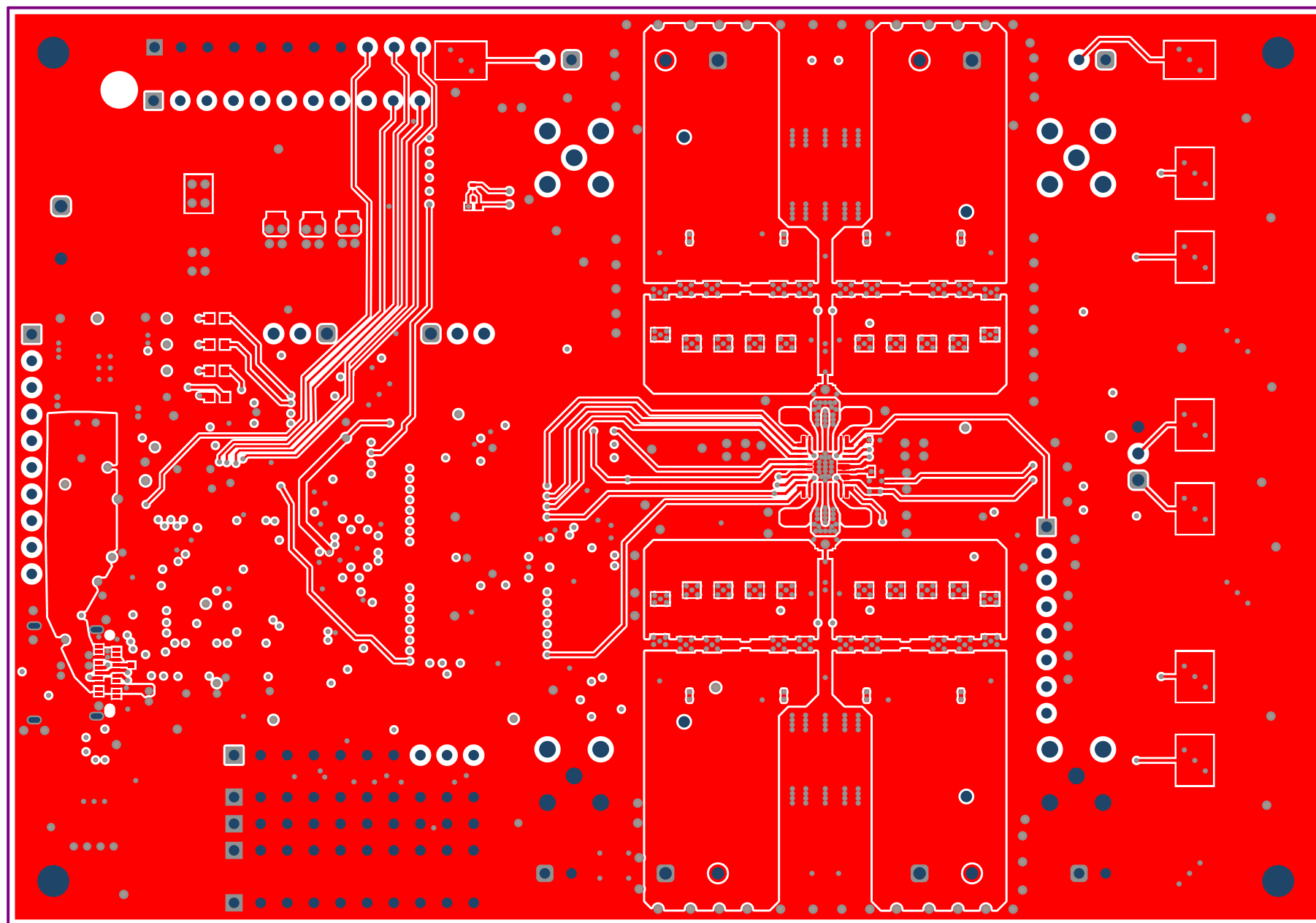


Figure 5-3. Layout Top, Layer 1

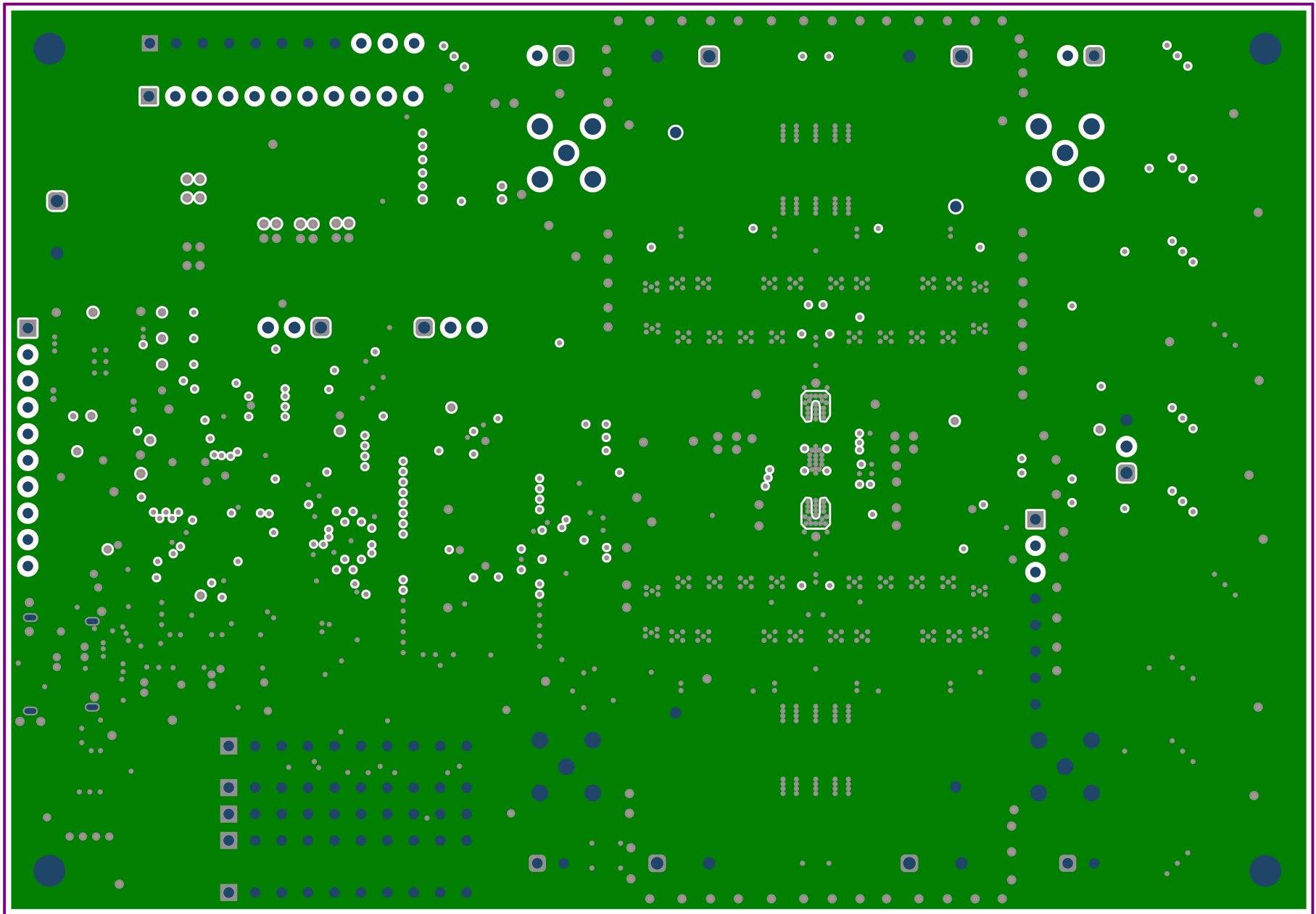


Figure 5-4. Layout Ground, Layer 2

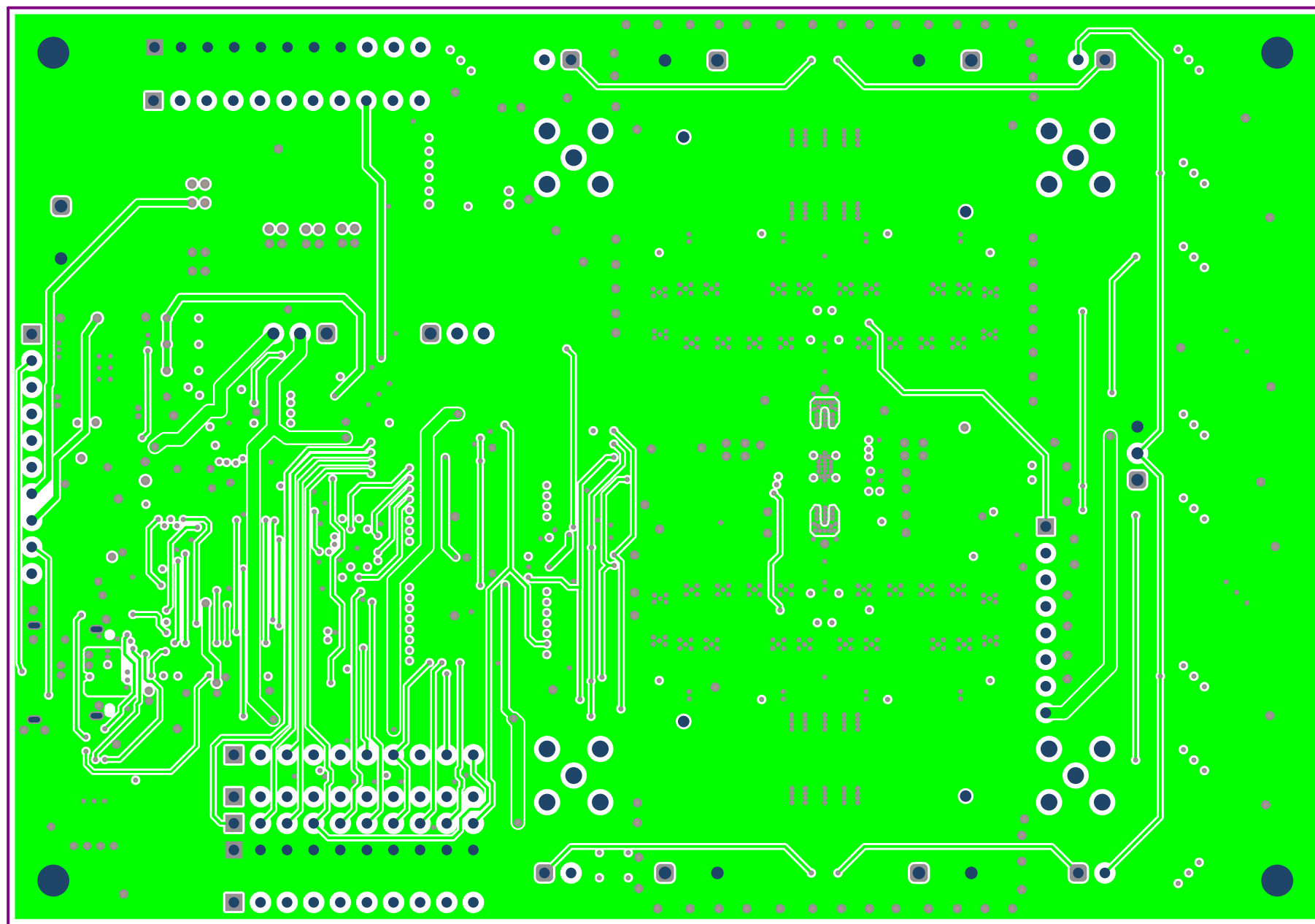


Figure 5-5. Layout Signal, Layer 3

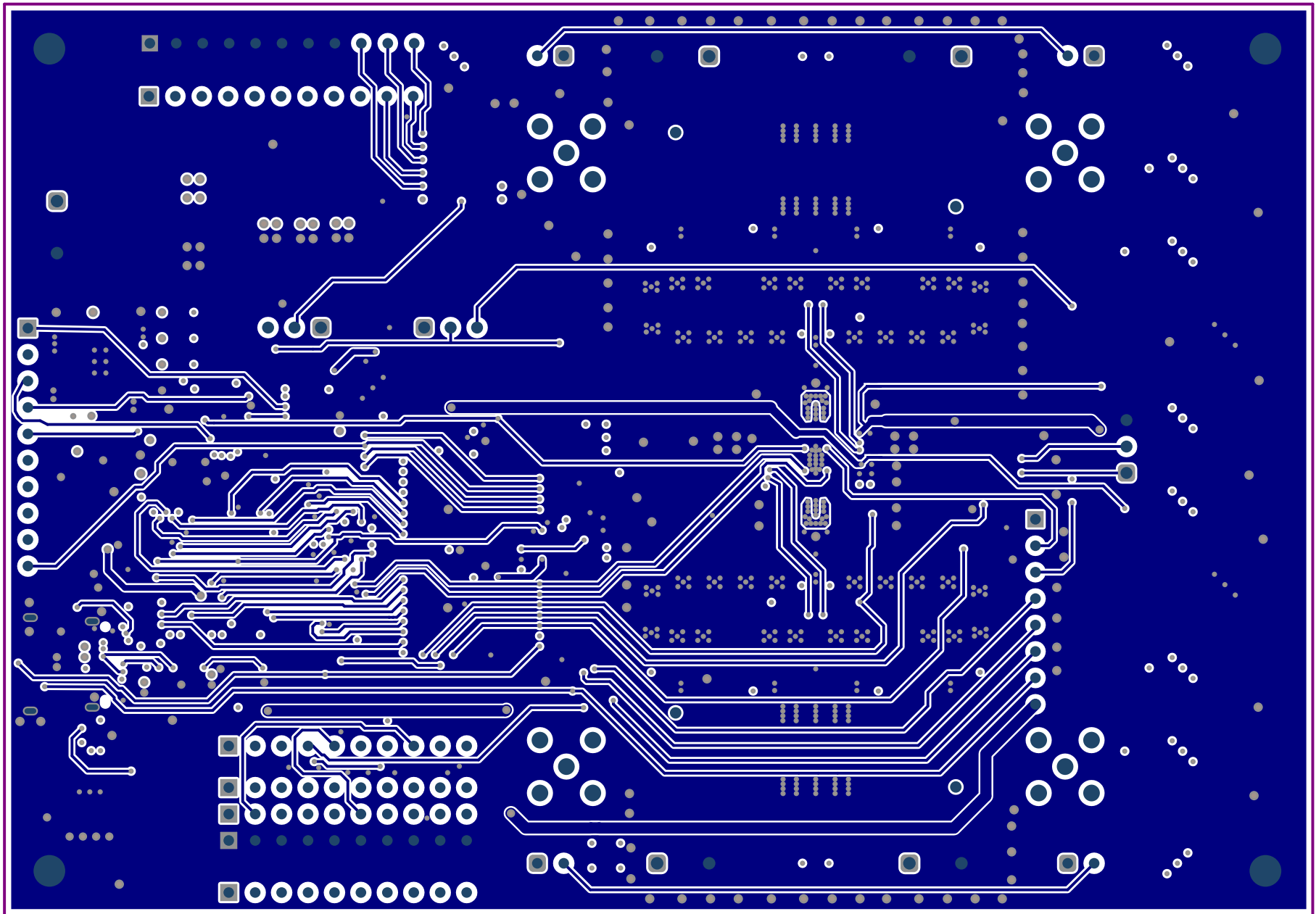


Figure 5-6. Layout Signal, Layer 4

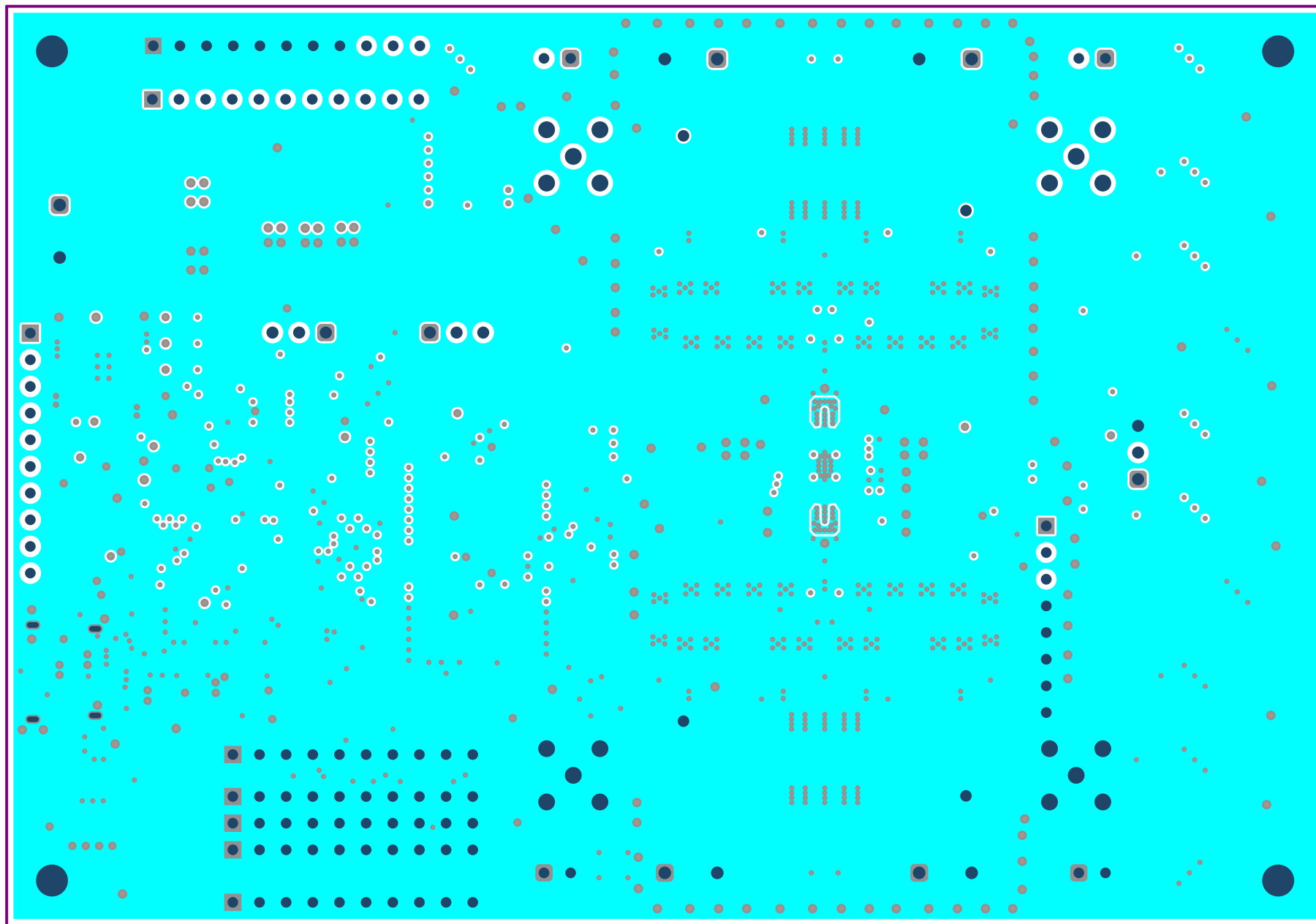


Figure 5-7. Layout Ground, Layer 5

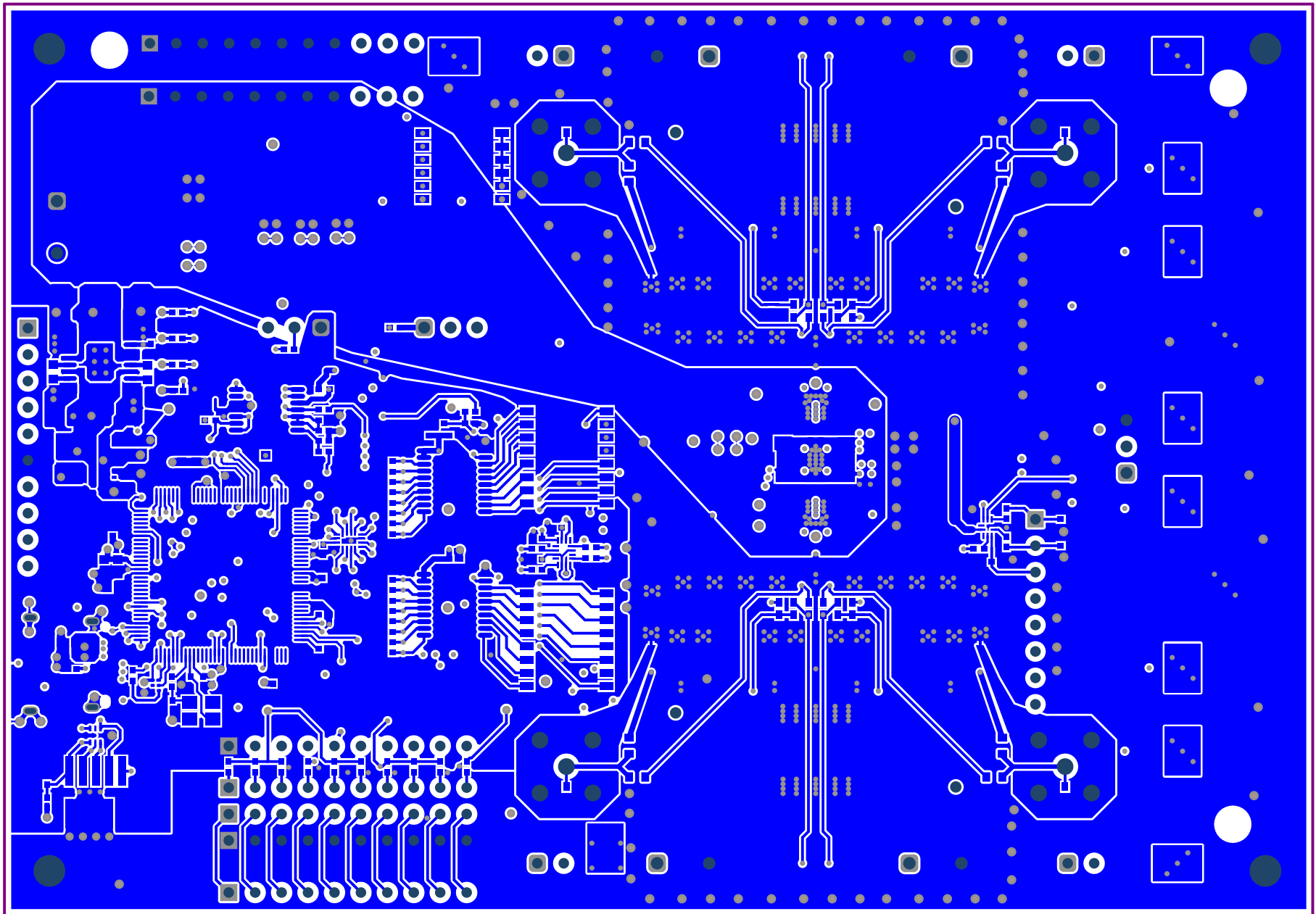


Figure 5-8. Layout Bottom, Layer 6

Table 5-1. Bill of Materials

Item#	Designator	Part Number	Quantity	Value	Manufacturer	Description	Package Reference
1	PCB	BMC085A	1		Any	Printed Circuit Board	
2	C1, C2, C3, C4, C111, C116	GCM21BR71A106KE22L	6	10uF	MuRata	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805	0805
3	C5, C6	NFM18HC105C1C3D	2		Murata	3 Terminals Low ESL Chip Multilayer Ceramic Capacitors for Automotive	0603
4	C7, C9, C110, C112	GCM155C71A474KE36D	4	0.47uF	MuRata	CAP, CERM, 0.47 uF, 10 V, +/- 10%, X7S, 0402	0402
5	C8, C28, C31, C54, C57, C61, C64, C68, C71, C73, C77, C82, C83, C92, C97, C113, C114, C115, C118, C119, C121	GCM188R70J225KE22D	21	2.2uF	MuRata	CAP, CERM, 2.2 uF, 6.3 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603
6	C11, C12, C13, C14, C22, C30, C53, C56, C60, C63, C67, C70, C72, C74, C98, C99, C101, C102, C105, C108, C109, C117, C120	GCM155R71C104KA55D	23	0.1uF	MuRata	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	0402
7	C15, C42, C59, C66	GCM188D70J106ME36D	4		Murata	Chip Multilayer Ceramic Capacitors for Automotive	0603
8	C16, C17, C21, C35, C43, C44, C45, C48, C76, C85, C86, C90	GCM21BD70J226ME36L	12	22uF	MuRata	CAP, CERM, 22 uF, 6.3 V, +/- 20%, X7T, AEC-Q200 Grade 1, 0805	0805
9	C29, C55, C62, C69	GCM21BR70J106KE22L	4	10uF	MuRata	CAP, CERM, 10 uF, 6.3 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	0805
10	C32, C33, C34, C106, C107	GCM31CR71A226KE02L	5	22uF	MuRata	CAP, CERM, 22 uF, 10 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	1206
11	C47	UUD1V151MNL1GS	1	150uF	Nichicon	CAP, AL, 150 uF, 35 V, +/- 20%, 0.17 ohm, SMD	8x10

Table 5-1. Bill of Materials (continued)

Item#	Designator	Part Number	Quantity	Value	Manufacturer	Description	Package Reference
12	C100	C0603C332K5RACTU	1	3300pF	Kemet	CAP, CERM, 3300 pF, 50 V, +/- 10%, X7R, 0603	0603
13	C103, C104	GCM1555C1H120JA16J	2	12pF	MuRata	CAP, CERM, 12 pF, 50 V, +/- 5%, COG/NP0, AEC-Q200 Grade 1, 0402	0402
14	D1	NSR05T40P2T5G	1		onsemi	Diode Schottky 40 V 500mA (DC) Surface Mount SOD-923	SOD-923
15	D2, D3, D4, D5	LB Q39G-L2N2-35-1	4	Blue	OSRAM	LED, Blue, SMD	BLUE 0603 LED
16	H1, H2, H3, H4	FC2058-440-A	4		Fascomp		SPACER
17	H5, H6, H7, H8	9900	4		Keystone	MACHINE SCREW PAN PHILLIPS 4-40	
18	J3, J5, J6, J16	SMA-J-P-H-ST-TH1	4		Samtec	SMA Jack, Straight, 50 Ohm, Gold, TH	TH, 5-Leads, Body 7x7mm
19	J4, J33	61300311121	2		Würth Elektronik	Header, 2.54 mm, 3x1, Gold, TH	Header, 2.54mm, 3x1, TH
20	J7, J8, J10, J12, J14	1792863	5		Phoenix Contact	Terminal Block, 5mm, 2x1, R/A, TH	Terminal Block, 5mm, 2x1, R/A, TH
21	J18, J19, J22, J23, J24, J27	TSW-110-07-G-S	6		Samtec	Header, 100mil, 10x1, Gold, TH	10x1 Header
22	J20, J21, J25, J26	TSW-102-07-G-S	4		Samtec	Header, 100mil, 2x1, Gold, TH	2x1 Header
23	J28, J29	ESQ-111-14-T-S	2		Samtec	Conn Elevated Socket SKT 11 POS 2.54mm Solder ST Thru-Hole Tube	HDR11
24	J30	ESQ-108-14-T-S	1		Samtec	Board-To-Board Connector, Vertical, ESQ Series, 8 Contacts, Receptacle, 2.54 mm, Through Hole	HDR8
25	J31	12401610E4#2A	1		Amphenol Canada	Receptacle, 0.5mm, USB TYPE C, R/A, SMT	Receptacle, 0.5mm, USB TYPE C, R/A, SMT
26	J32	FTSH-105-01-F-DV-K	1		Samtec	Header (Shrouded), 1.27mm, 5x2, Gold, SMT	Header(Shrouded), 1.27mm, 5x2, SMT

Table 5-1. Bill of Materials (continued)

Item#	Designator	Part Number	Quantity	Value	Manufacturer	Description	Package Reference
27	L1, L5, L7, L8	TFM160810ALTA33N NTAA	4	0.033uH	TDK	Fixed Inductor 0.033uH 30% 4.7A 9mOhm 0603	0603
28	L2, L3, L4, L6	TFM322512ALMAR47 MTAA	4	470nH	TDK	Inductor, Thin Film, 470 nH, 5.3 A, 0.021 ohm, AEC- Q200 Grade 0, SMD	TDK Inductor
29	Q1	CSD13381F4	1	12V	Texas Instruments	MOSFET, N-CH, 12 V, 2.1 A, YJC0003A (PICOSTAR-3)	YJC0003A
30	R1, R3, R4, R6, R7, R11, R13, R15, R17, R43, R64, R80	CRCW04020000Z0E D	12	0	Vishay-Dale	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
31	R2, R5, R8, R19	RMCF0402FT49R9	4	49.9	Stackpole Electronics Inc	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
32	R9, R10, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R34, R35, R44, R45, R46, R47, R48, R49, R55, R56, R57, R58, R59, R60, R61, R62, R66, R73, R75, R76, R79	CRCW040210K0JNE D	34	10k	Vishay-Dale	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
33	R12, R14, R16, R69, R78	CRCW04021K20JNE D	5	1.2k	Vishay-Dale	RES, 1.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
34	R18	CRCW0402240RJNE D	1	240	Vishay-Dale	RES, 240, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
35	R31, R70, R71, R74, R77	CRCW04021K00JNE D	5	1.0k	Vishay-Dale	RES, 1.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
36	R50, R72	CRCW0402200KJNE D	2	200k	Vishay-Dale	RES, 200 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
37	R51, R52	CRCW04021M00JNE D	2	1.0Meg	Vishay-Dale	RES, 1.0 M, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
38	R53	CRCW0402374KFKE D	1	374k	Vishay-Dale	RES, 374 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402

Table 5-1. Bill of Materials (continued)

Item#	Designator	Part Number	Quantity	Value	Manufacturer	Description	Package Reference
39	R63, R67, R68	CRCW04024K87FKE D	3	4.87k	Vishay-Dale	RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
40	R65	CRCW0402100RJNE D	1	100	Vishay-Dale	RES, 100, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
41	S1	218-6LPST	1		CTS Electrocomponents	Switch, SPST, Slide, Off-On, 6 Pos, 0.025A, 24V, SMD	5.8x8.79mm
42	S2, S3	218-8LPST	2		CTS Electrocomponents	Switch, SPST, 8 Pos, 25mA, 24VDC, SMD	11.33x5.8mm
43	SH-J1, SH-J6, SH- J13, SH-J14, SH-J15	881545-2	5		TE Connectivity	Shunt, 100mil, Gold plated, Black	Shunt 2 pos. 100 mil
44	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	5016	16		Keystone	Test Point, Compact, SMT	Testpoint_Keystone_C ompact
45	U1	LP876242B0RQKRQ1	1		Texas Instruments	Four 8.8-MHz Buck Converters for AWR and IWR MMICs	VQFN-HR32
46	U2	LM2901AVQPWRQ1	1		Texas Instruments	AEC-Q100 Quad Comparator, PW0014A (TSSOP-14)	PW0014A
47	U3	MSP432E401YTPDT R	1		Texas Instruments	MSP432E401YTPDT, PDT0128A (TQFP-128)	PDT0128A
48	U4, U6	SN74GTL2003PWR	2		Texas Instruments	8-BIT BIDIRECTIONAL LOW-VOLTAGE TRANSLATOR, PW0020A (TSSOP-20)	PW0020A
49	U5	TPD6E004RSER	1		Texas Instruments	Low-Capacitance 6- Channel +/-15 kV ESD Protection Array for High-Speed Data Interfaces, RSE0008A (UQFN-8)	RSE0008A
50	U7	TPD4S012DRYR	1		Texas Instruments	4-Channel USB ESD Solution with Power Clamp, DRY0006A (USON-6)	DRY0006A

Table 5-1. Bill of Materials (continued)

Item#	Designator	Part Number	Quantity	Value	Manufacturer	Description	Package Reference
51	U8, U9	TS3A5018RSVR	2		Texas Instruments	10-Ohm Quad SPDT Analog Switch, RSV0016A (UQFN-16)	RSV0016A
52	U10	TPS60110PWPR	1		Texas Instruments	5 V, Boost Charge Pump, 300 mA, 2.7 to 5.4 V Input with Synchronization pin, -40 to 85 degC, 20-pin SOP (PWP20), Green (RoHS & no Sb/Br)	PWP0020C
53	U11	TS3A5223RSWR	1		Texas Instruments	0.5Ω Dual SPDT Bidirectional Analog Switch, RSW0010A (UQFN-10)	RSW0010A
54	U12	TLV73333PQDRVRQ 1	1		Texas Instruments	Capacitor-Free, 300-mA, Low-Dropout Regulator for Automotive, DRV0006A (WSON-6)	DRV0006A
55	U13	TLV73318PQDRVRQ 1	1		Texas Instruments	Capacitor-Free, 300-mA, Low-Dropout Regulator for Automotive, DRV0006A (WSON-6)	DRV0006A
56	Y1	NX3225SA-25.000M-STD-CRS-2	1		NDK	CRYSTAL 25.0000MHZ 8PF SMD	SMT_XTAL_3MM2_2MM5

6 Additional Resources

- Texas Instruments, [Scalable PMIC's GUI User's Guide](#)
- Texas Instruments, [LP876242-Q1 Four 8.8-MHz Buck Converters for AWR and IWR MMICs data sheet](#)

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2021) to Revision A (August 2022)	Page
• Updated the 8.8 MHz switching frequency information in introduction.....	3
• Updated the Figure 2-1.....	3
• Headers numbering changed.....	4
• Updated the current capability for each buck in Table 3-1	4
• Updated the test point numbers and included buck output voltage sense points in Table 3-2.....	4
• Updated the Figure 3-1 and header numbering in the corresponding description as well as in Table 3-3, changed header numbering in Table 3-4.....	4
• Updated the header numbering, Figure 3-2, capacitors numbering in Table 3-6, updated the dip switches description in Table 3-7	6
• Updated the header numbering and IC names for supplying power to the MCU, updated LED D5 description in Table 3-8	8
• Updated the jumper settings procedure information and updated Figure 4-1.....	9
• Updated all the figures with schematics, layout plots and bill of materials table.....	10

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

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3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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