EVM User's Guide: TPS562242BEVM

TPS562242B Step-Down Converter Evaluation Module

Description

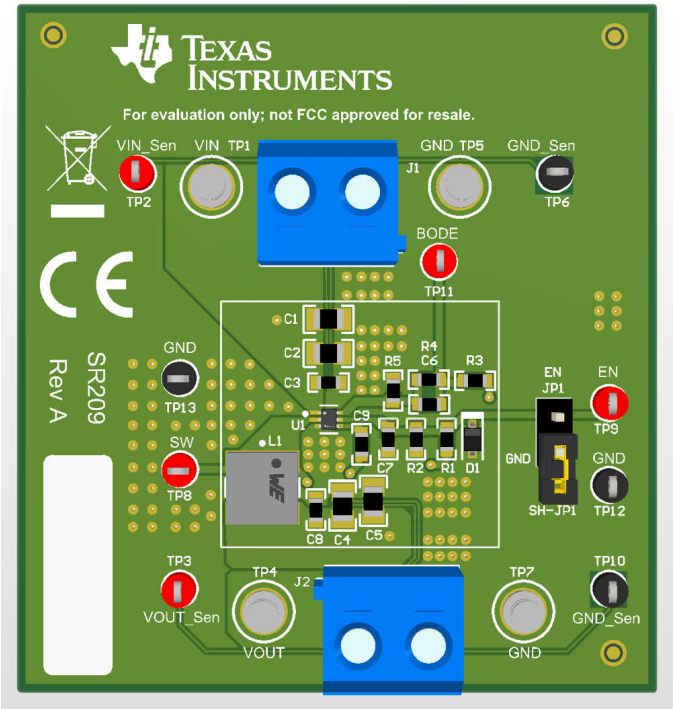
TPS562242B evaluation module (EVM) is a simple, easy-to-use, fully assembled and tested evaluation module for the TPS562242B 2A synchronous buck converter. The EVM operates from 3V to 17V input to deliver 1.05V output, with AC signal injection terminals for feedback loop measurements.

Features

- 3V to 17V input voltage range
- 0.6V to 10V output voltage range
- Up to 2A output current
- Eco-mode at light loading
- Fast transient response

Applications

- Appliances, video recorder
- WLAN/Wi-Fi access point, modem (cable, DSL, GFAST), small business router
- TV, STB and DVR



TPS562242BEVM Board (Top Side)

1 Evaluation Module Overview

1.1 Introduction

The TPS562242B is a single, adaptive on-time, D-CAP3™ control mode, synchronous buck converter that requires a very low external component count. The D-CAP3 control mode is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types, and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 1.2MHz and enters Eco-mode in light load conditions. The high-side and low-side switching MOSFETs are incorporated inside the TPS562242B package along with the gate-drive circuitry. The TPS562242B DC/DC synchronous converter is designed to support up to a 2A continuous current from an input voltage source of 3V to 17V. The output voltage range is from 0.6V to 10V. Table 1-1 gives rated input voltage and output current ranges for the evaluation module.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE (V_{IN}) RANGE	OUTPUT CURRENT (I_{OUT}) RANGE
TPS562242BEVM	V_{IN} = 3V to 17V	0A to 2A

The TPS562242BEVM evaluation module (EVM) is a single, synchronous buck converter providing 1.05V at 2A from 3V to 17V input. This user's guide describes the TPS562242BEVM performance.

This user's guide contains information for the TPS562242B as well as support documentation for the TPS562242BEVM evaluation module. Included are the performance specifications, board layout, schematic and the list of materials of the TPS562242BEVM.

1.2 Kit Contents

- One TPS562242BEVM board
- EVM disclaimer Read Me

1.3 Specification

This EVM operates from 3V to 17V input, 12V nominal, and provides a 1.05V output at 2A. The EVM also includes AC signal injection terminals for feedback loop measurements. Specification, application information, and schematic are shown in Section 4.1 and Section 5.1.

1.4 Device Information

Synchronous buck converter TPS562242B is used in the EVM to achieve the high-efficiency power delivery and voltage conversion. The TPS562242B operates in Eco-mode, which maintains high efficiency during light loading.

Table 1-2. Device Information

PART NUMBER	MODE	PACKAGE
TPS562242B	ECO	DRL (SOT-563, 6)

2 Performance Specification Summary

Table 2-1 provides a summary of the TPS562242BEVM performance specifications. Specifications are given for an input voltage of V_{IN} = 12V and an output voltage of 1.05V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. Performance Specifications Summary

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		3	12	17	V
Output voltage set point			1.05		V
Operating frequency	V_{IN} = 12V, I_O = 2A		1.4		MHz
Output current range		0		2	A
Over current limit	V_{IN} = 12V, L_O = 1.2µH		3		A
Output ripple voltage	V_{IN} = 12V, I_O = 2A		6		mV_{PP}

3 Output Voltage Setpoint

The output voltage of the EVM can be selected by changing the value of resistor R_4 (R_{UPPER}) and R_5 (R_{LOWER}). USe Equation 1 to calculate the value of R_4 for a specific output voltage. The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Start with a 10kΩ or 30kΩ for R4 (R_{FBB}) and use Equation 1 to calculate R5 (R_{FBT}). To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_4}{R_5}\right) \quad (1)$$

4 Hardware

4.1 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS562242BEVM. The section also includes test results typical for the evaluation modules and the following:

- Efficiency
- Output load regulation
- Output line regulation
- Load transient response
- Start-up
- Shutdown
- Output voltage ripple

4.1.1 Input, Output Connections

The TPS562242BEVM is provided with input, output connectors and test points as shown in Table 4-1. Figure 4-1 shows connectors and jumpers placement on TPS562242BEVM board.

A power supply capable of supplying 2A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 2A. Wire lengths must be minimized to reduce losses in the wires. Test point TP2 provides a place to monitor the V_{IN} input voltages with TP6 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP10 as the ground reference.

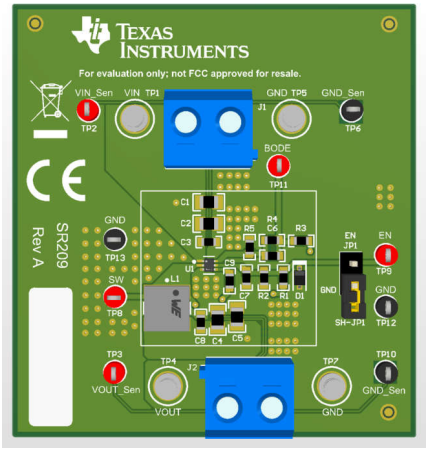


Figure 4-1. TPS562242BEVM Connectors and Jumpers Placement

Table 4-1. Connection and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	V_{OUT}, 1.05V at 2A maximum
JP1	EN control. Shunt EN to GND to disable
TP1	V_{IN} positive power point
TP2	V_{IN} positive monitor point
TP3	V_{OUT} positive monitor point
TP4	V_{OUT} positive power point
TP5, TP7	GND power point
TP6, TP10, TP12, TP13, TP16	GND monitor point
TP8	Switch node test point
TP9	EN test point
TP11	Test point for loop response measurements

4.1.2 Start-Up Procedure

1. Verify that the jumper at JP1 (Enable control) pins 1 and 2 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate input voltage to VIN (J1-2) and GND (J1-1).
3. Move the jumper at J1 (Enable control) pin 2 and 1 (EN and GND) to enable the output.

4.1.3 Efficiency

Figure 4-2 shows the efficiency for the TPS562242BEVM at an ambient temperature of 25°C.

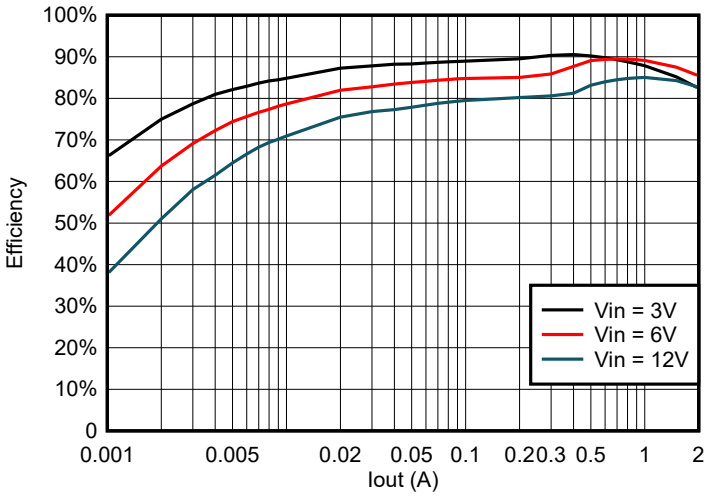


Figure 4-2. TPS562242BEVM Efficiency

4.1.4 Load Regulation

Figure 4-3 shows load regulation for the TPS562242BEVM.

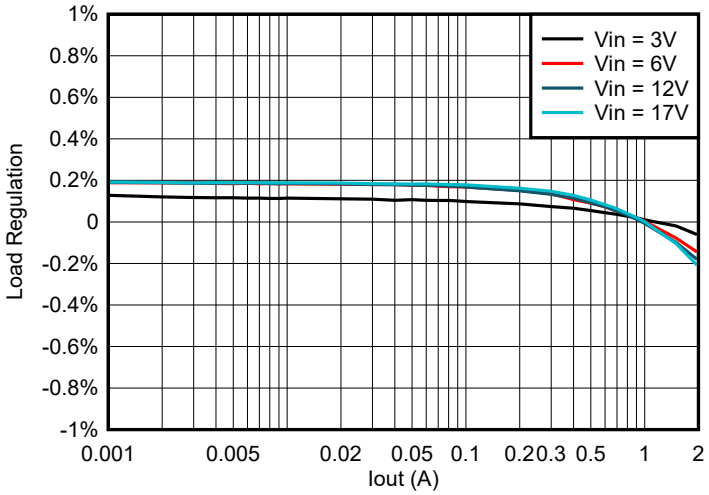


Figure 4-3. TPS562242BEVM Load Regulation

4.1.5 Line Regulation

Figure 4-4 shows line regulation for the TPS562242BEVM.

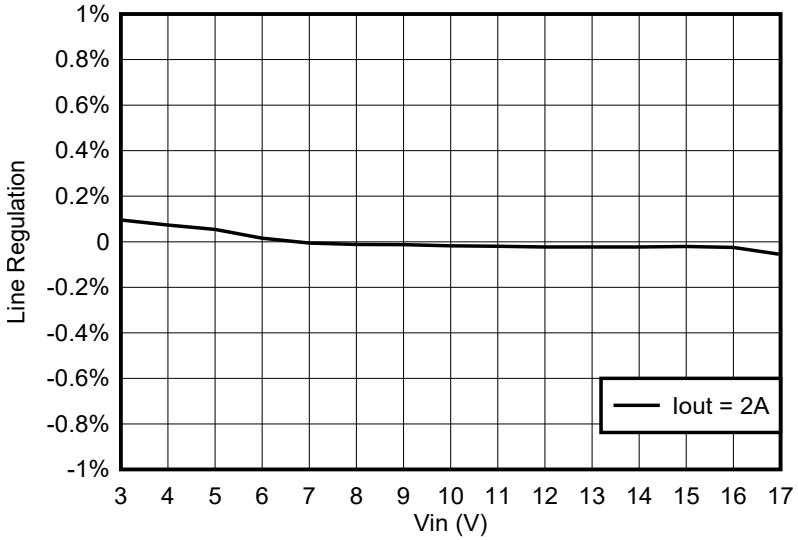


Figure 4-4. TPS562242BEVM Line Regulation

4.1.6 Load Transient Response

Figure 4-5 shows the response to load transient for TPS562242BEVM. The current steps slew rate is set as 0.8A/µs.

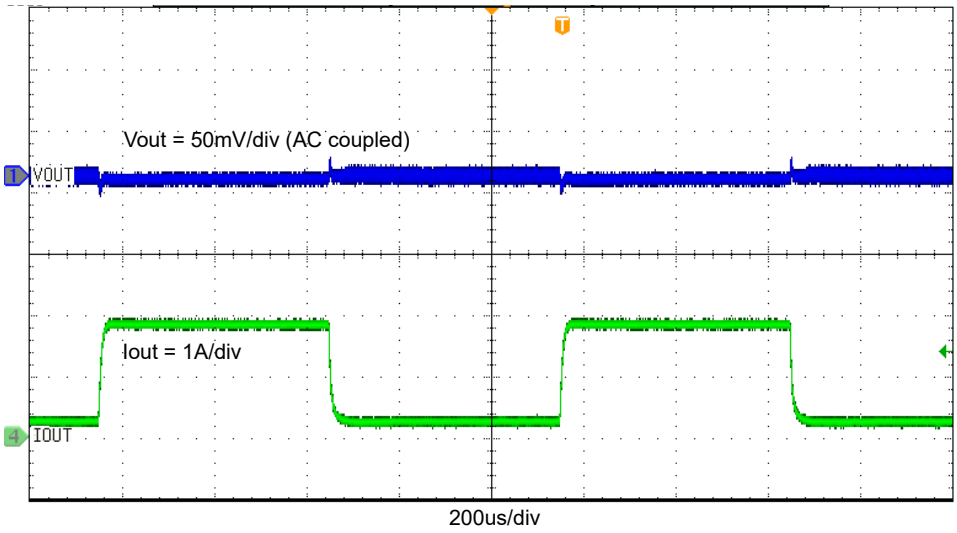


Figure 4-5. TPS562242BEVM Load Transient Response, 10% to 90% (0.2A to 1.8A) Load Step

4.1.7 Start-Up

Figure 4-6 shows the TPS562242BEVM start-up waveform relative to V_{IN}. The load is 2A.

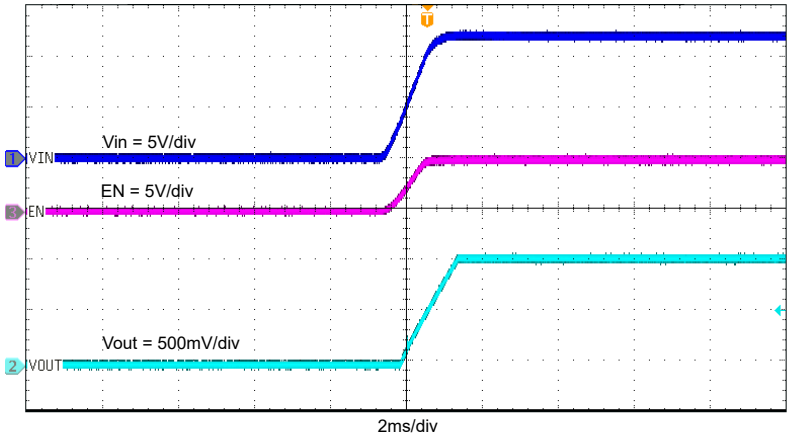


Figure 4-6. TPS562242BEVM Start-Up Relative to V_{IN}

Figure 4-7 shows the TPS562242BEVM start-up waveform relative to enable (EN). The load is 2A.

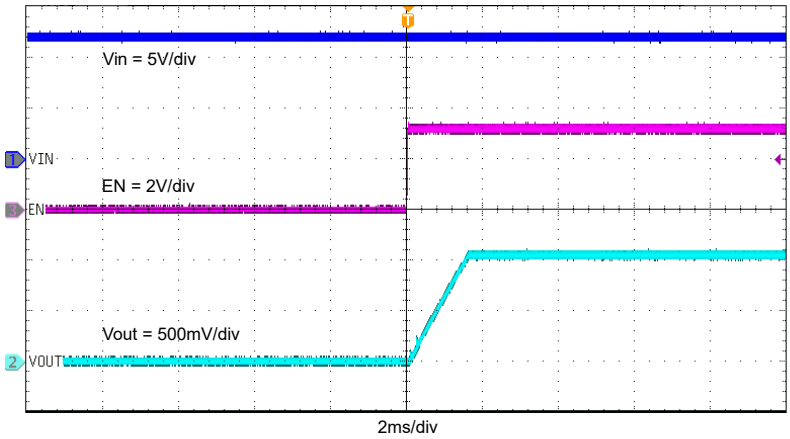


Figure 4-7. TPS562242BEVM Start-Up Relative to EN

4.1.8 Shutdown

Figure 4-8 shows the TPS562242BEVM shut-up waveform relative to V_{IN}. The load is 2A.

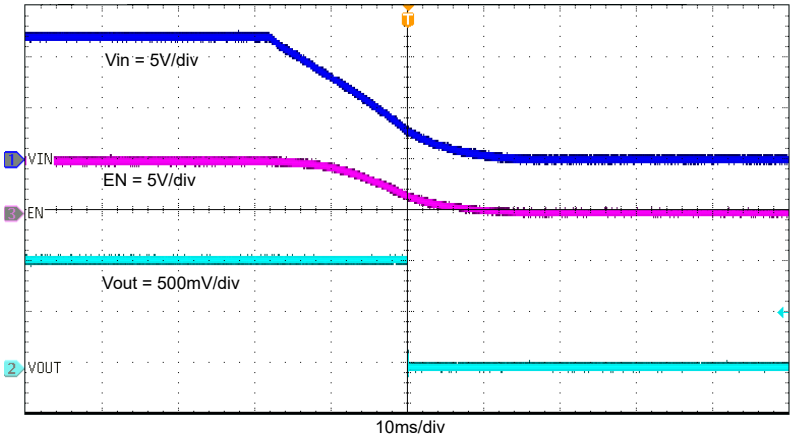


Figure 4-8. TPS562242BEVM Shutdown Relative to V_{IN}

Figure 4-9 shows the TPS562242BEVM shut-up waveform relative to enable (EN). The load is 2A.

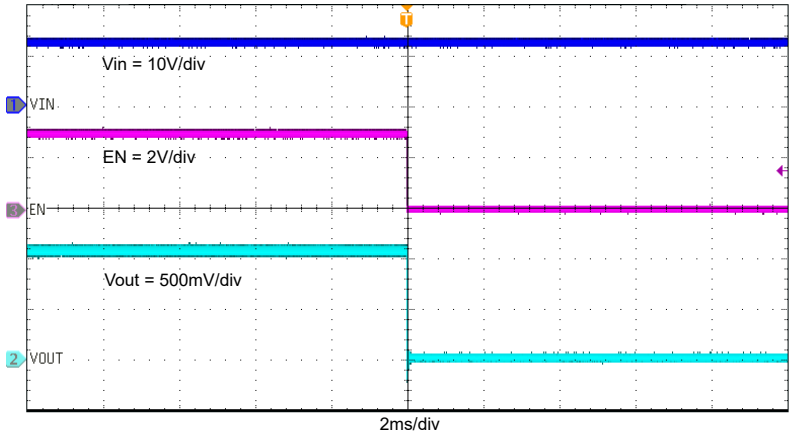


Figure 4-9. TPS564252EVM Shutdown Relative to EN

4.1.9 Output Voltage Ripple

Figure 4-10 and Figure 4-11 show the TPS562242BEVM output voltage ripple. The output currents are as indicated.

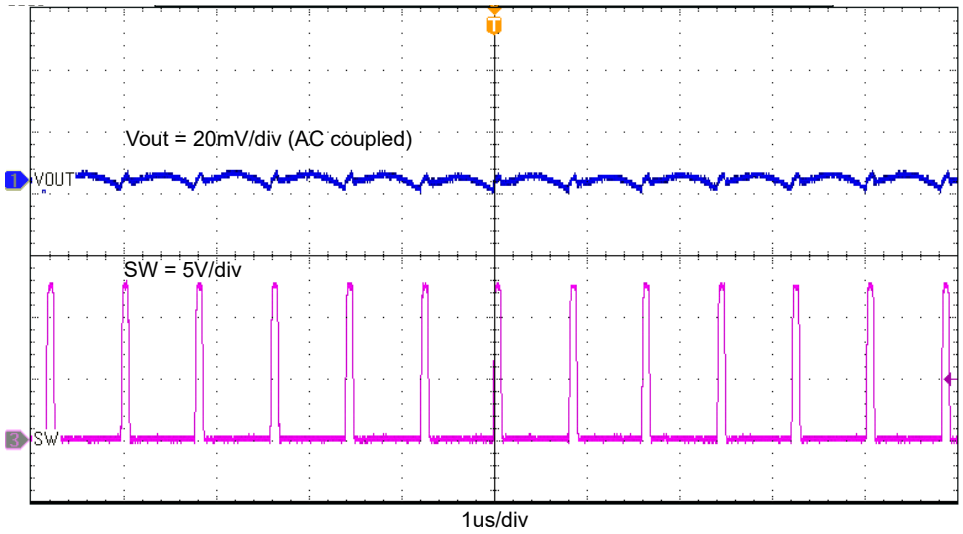


Figure 4-10. TPS562242BEVM Output Voltage Ripple, I_{OUT} = 2A

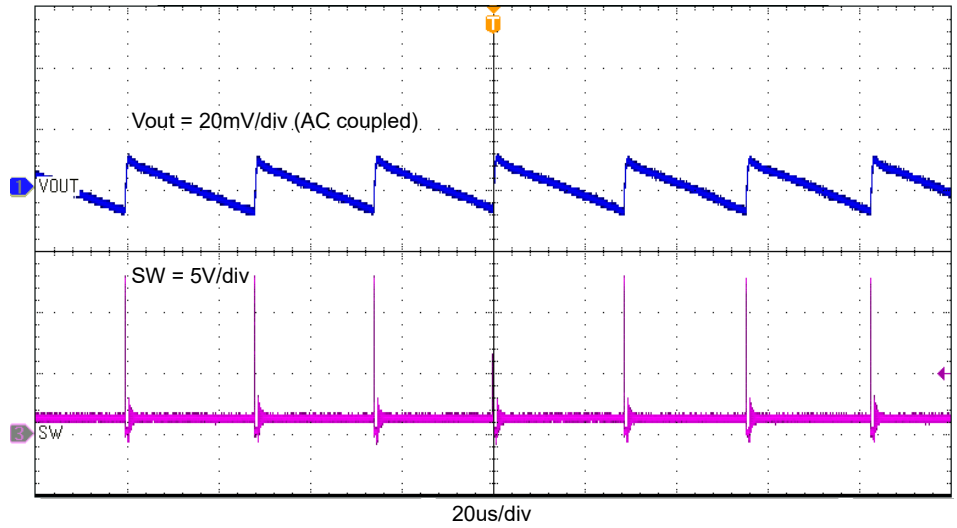


Figure 4-11. TPS562242BEVM Output Voltage Ripple, I_{OUT} = 0.01A

5 Hardware Design Files

5.1 Schematic

Figure 5-1 is the schematic for the TPS562242BEVM.

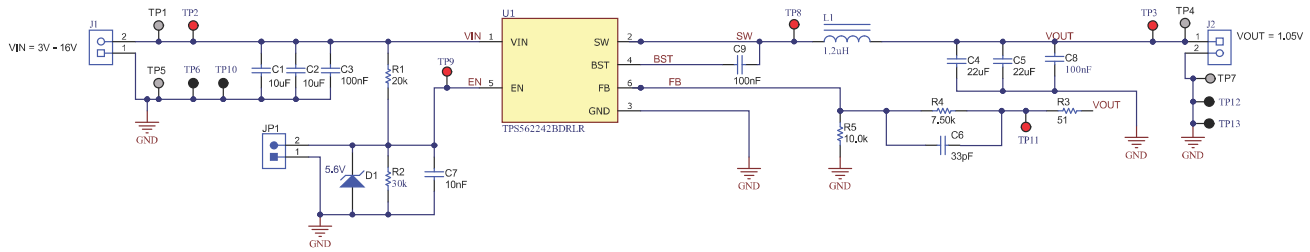


Figure 5-1. TPS562242BEVM Schematic Diagram

5.2 PCB Layout

This section provides a description of the TPS562242BEVM, board layout, and layer illustrations.

Figure 5-2, Figure 5-3, and Figure 5-4 show the board layout for the TPS562242BEVM. The top layer contains the main power traces for VIN, VOUT, and ground. Connections for the pins of the TPS562242B and a large area filled with ground are also on the top layer. Most of the signal traces are also located on the top side. The input decoupling capacitors C1, C2, and C3 are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. The bottom layer is a ground plane along with the signal ground copper fill and the feedback trace from the point of regulation to the top of the resistor divider network. Both the top layer and bottom layer use 2oz copper thickness.

Figure 5-5 and Figure 5-6 are the TPS562242BEVM board top view and bottom view, respectively.

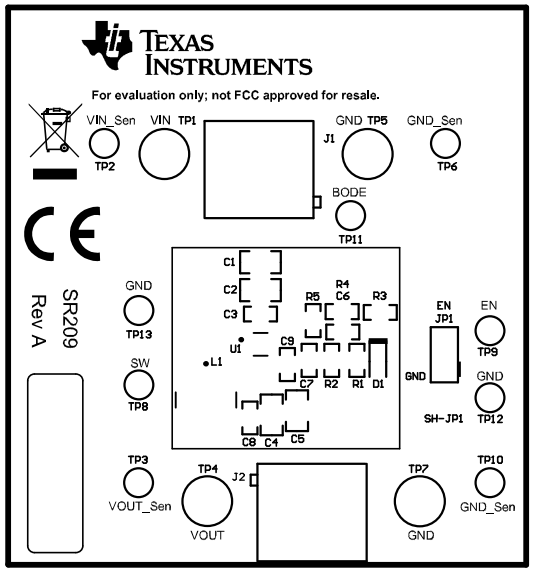


Figure 5-2. TPS562242BEVM Top Assembly

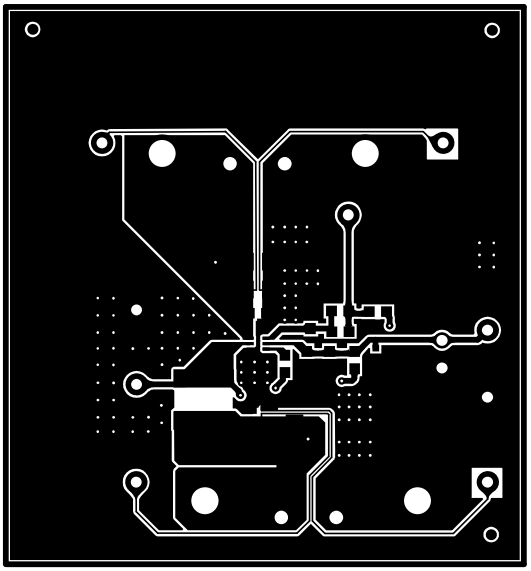


Figure 5-3. TPS562242BEVM Top Layer

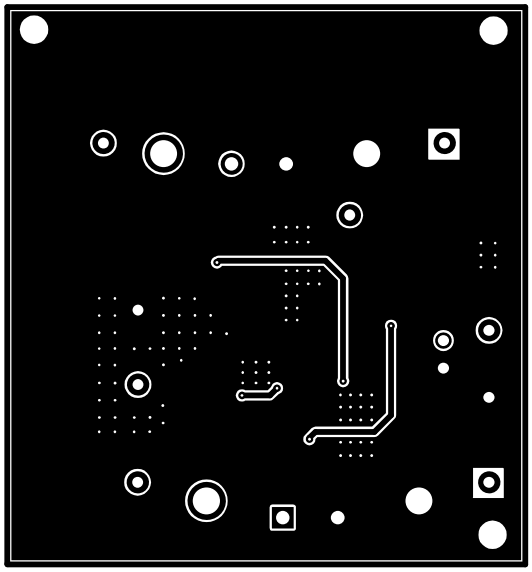


Figure 5-4. TPS562242BEVM Bottom Layer

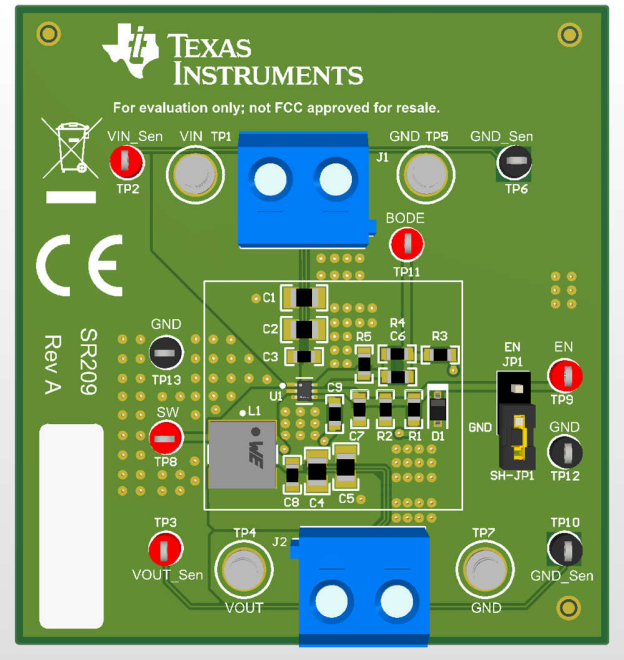


Figure 5-5. TPS562242BEVM Board (Top View)

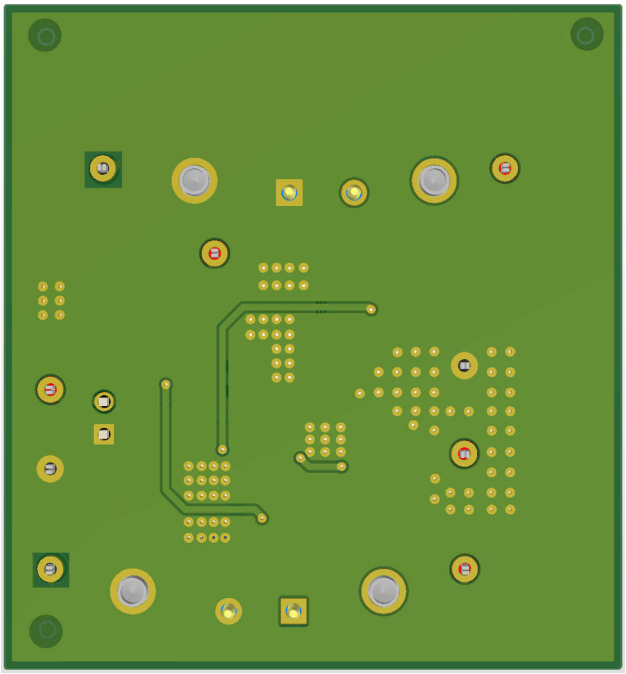


Figure 5-6. TPS562242BEVM Board (Bottom View)

5.3 Bill of Materials

Table 5-1 lists the bill of materials.

Table 5-1. Bill of Materials

DES	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
!PCB1	1	Printed Circuit Board	SR209	Any
C1, C2	2	Capacitor, ceramic, 10µF, 25V, ±20%, X5R, 0805	GRM21BR61E106MA73L	MuRata
C3, C8,C9	3	Capacitor, ceramic, 0.1uF, 25V, ± 10%, X7R, 0603	C1608X7R1E104K080AA	TDK
C4, C5	2	Capacitor, ceramic, 22µF, 10V, ±20%, X5R, 0805	GRM21BR61A226ME44L	MuRata
C6	1	Capacitor, ceramic, 33pF, 100V, ±5%, C0G/NP0, 0603	GRM1885C2A330JA01D	MuRata
C7	1	Capacitor, ceramic, 0.01uF, 50V, ± 10%, X7R, 0603	C1608X7R1H103K080AA	TDK
J1, J2	2	Terminal block, 5.08mm, 2 × 1, Brass, TH	ED120/2DS	On-Shore Technology
JP1	1	Header, 100 mil, 2 × 1, Tin, TH	PEC02SAAN	Sullins Connector Solutions
L1	1	Shielded Inductor, 1.2uH, 7A, 0.0155Ω, SMD	74438357012	Wurth Elektronik
LBL1	1	Thermal transfer printable labels, 0.650" W × 0.200" H – 10,000 per roll	THT-14-423-10	Brady
R1	1	Resistor, 20kΩ, 5%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060320K0JNEA	Vishay-Dale
R2	1	Resistor, 30kΩ, 5%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060330K0JNEA	Vishay-Dale
R3	1	Resistor, 51Ω, 5%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060351R0JNEA	Vishay-Dale
R4	1	Resistor, 7.5kΩ, 1%, 0.1W, 0603	RC0603FR-077K5L	Yageo
R5	1	Resistor, 10.0kΩ, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060310K0FKEA	Vishay-Dale
SH-JP1	1	Shunt, 100 mil, gold plated, black	SNT-100-BK-G	Samtec
TP1, TP4, TP5, TP7	4	Terminal, turret, TH, double	1502-2	Keystone
TP2, TP3, TP8, TP9, TP11	5	Test point, miniature, red, TH	5000	Keystone
TP6, TP10, TP12, TP13	4	Test point, miniature, black, TH	5001	Keystone
D1	1	Diode, Zener, 5.6V, 200 mW, SOD-323	MMSZ5232BS-7F	Diodes Inc.
U1	1	3V to 17V Input, 2A Synchronous Buck Converter, SOT-563	TPS562242BDRLR	Texas Instruments

6 Additional Information

6.1 Trademarks

D-CAP3™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7 Reference

Texas Instruments, *TPS56x24x 3V to 17V Input, 2A/3A, Synchronous Buck Converters in SOT-563 Package* datasheet

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