EVM User's Guide: TCAN4572EVM

TCAN4572 Evaluation Module User's Guide

Description

The TCAN4572EVM features the TCAN4572-Q1 automotive CAN FD controller with integrated transceiver. This EVM provides microcontrollers that can access CAN FD or CAN FD Light applications through SPI, without an integrated CAN FD controller or additional channels needed.

Features

- Supports Classical CAN, CAN FD and CAN FD Light applications
- SPI
- Crystal oscillator (40MHz)
- Industry-standard DB-9 connector
- TVS diode pad (not populated)
- CAN bus termination with disconnect headers
- Status LEDs

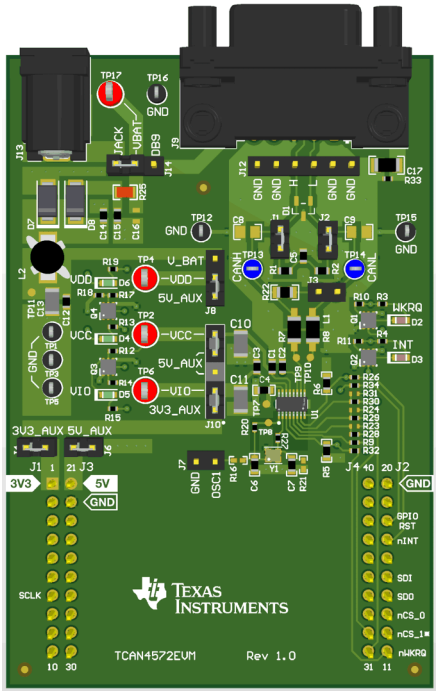

Figure 1-1. TCAN4572 EVM

1 Evaluation Module Overview

1.1 Introduction

This user's guide describes the TCAN4572 EVM. This EVM helps designers evaluate device performance, support fast development, and analyze CAN FD or CAN FD light systems using TCAN4572-Q1 CAN FD physical layer transceiver devices, explaining the board hardware details, functions and locations of jumpers and connectors. The EVM can also be used as a CAN FD light Commander node

1.2 Kit Contents

1. TCAN4572 EVM

1.3 Specification

The TCAN4572 EVM provides the user with the ability to evaluate the TI TCAN4572 Automotive CAN FD Controller with integrated transceiver devices. Any MCU or SPI controller with an I/O voltage of 3.3V or 5V can be connected to the EVM through a standard interface header.

Table 1-1. EVM Specification

Parameter	Specification
VDD Supply Voltage	5V or VBAT (jumper selectable)
VCC Supply Voltage	5V
VIO Supply Voltage	3.3V or 5V (jumper selectable)
CAN Bus Connector	DB9 (J9), screw terminal (J12)
Host Interface	SPI (via dual 20-pin receptacle J5/J11)
Orderable Part Number	TCAN4572EVM

1.4 Device Information

The EVM provides flexibility for device pin and CAN bus configuration. The EVM features a polarity-protected and EMC-filtered supply voltage that allows the EVM to operate from a 12V or 24V battery. There are test points for all main points where probing is necessary for evaluation such as GND, VDD, VCC, VIO, VSUP, OSC1, OSC2, CANH, CANL, and other logic pins. The EVM supports many options for CAN bus configuration. The EVM allows for two termination schemes through the use of jumpers to select between the split termination configuration or a single 120Ω resistor. If needed, there are footprints for a common-mode choke, TVS diode for ESD protection, and capacitors for further EMC protection or signal conditioning. A DSUB9 connector is included to allow the evaluation and use of the CAN bus in larger systems. A crystal oscillator is provided as external oscillator source for OSC1 and OSC2 pins.

2 Hardware

2.1 Power Requirements

The TCAN4572EVM supports multiple power supply configurations.

2.1.1 VBAT / VSUP

This EVM has an external battery supply voltage to be provided typically in 12V or 24V. CAN transceivers are commonly found in automotive applications and operate across a wide recommended supply voltage range corresponding to a vehicle battery. This supply voltage is used by the transceiver's VDD pin. The TCAN4572-Q1 operates across a range of 4.5V to 36V with an absolute maximum voltage of 42V, the voltage must be within device limits for proper operation.

The board uses a 30V Zener diode as protection from excessive supply voltages, along with a reverse-blocking Schottky diode and other EMC-filtering components on this supply voltage commonly found in system applications. The board refers to the raw voltage supplied to the board as VBAT to correspond with a system battery voltage, and the voltage after the supply filter as VSUP which is the actual voltage supplied to the device VDD pin. Supplying both a supply voltage and the bus communication through a single wire harness is common. This supply voltage can be supplied through pin 9 of the DB9 connector J9, or from a standalone supply through the DC barrel jack J13. Header J14 allows a shunt to be placed between the center pin and the selected voltage source.

2.1.2 VDD

VDD is the device supply voltage for the TCAN4572-Q1. VDD can be set to either 5V (from 5V_AUX) or connected directly to VSUP using jumper J8 (VDD selection).

Table 2-1. VDD Selection

J8 Position	VDD Source
Pins 1-2	VDD = VSUP (battery supply rail)
Pins 2-3	VDD = 5V_AUX

2.1.3 VCC

VCC is the 5V CAN transceiver supply voltage. VCC is supplied from the 5V_AUX.

2.1.4 VIO

VIO sets the logic level for the I/O pins. VIO can be set to either 3.3V or 5V using jumper J10 (V_CAN/IO selection):

Table 2-2. VIO Selection

J10 Position	VIO / VCC Source
Pins 1-2	CAN_VIO = 3V3_AUX
Pins 2-3	CAN_VIO = 5V_AUX

2.2 Crystal Oscillator

The TCAN4572-Q1 requires either a crystal oscillator or a single-ended clock to run the digital core. A 40MHz crystal oscillator is installed and connected to the OSC1 and OSC2 pins by default and is available whenever the VIO 3.3V supply is present. CAN FD data rates of 2Mbps or greater require a clock frequency of 40MHz to generate a time quanta small enough to allow for accurate data sampling of CAN bits. For slower applications with data rates < 2Mbps, the crystal can be replaced with a 20MHz version if desired, but the 40MHz crystal is still recommended. To use the internal clock source of the transceiver, the crystal oscillator can be bypassed through 0Ω resistors R16 and R21 (DNI). For more information on clock detection, refer to TCAN4572-Q1 datasheet.

2.3 CAN

The TCAN4572 EVM is populated with one 120Ω resistor selectable via jumper, between CANH and CANL, and the 120Ω split termination (two 60Ω resistors in series) including the split capacitor. When using only split termination, the EVM is used as a terminated end of a bus. For electrical measurements to represent the total loading of the bus, use both the split termination and the 120Ω resistor in parallel to give the standard 60Ω load for parametric measurement.

Table 2-3. CAN Bus Termination Configuration

Termination Configuration	Termination Jumpers			Split Termination Resistors		Split Termination Capacitor
Jumper	**J1**	**J2**	**J3**	**R1**	**R2**	**C5**
No termination	Open	Open	Open	Not available	Not available	Not available
120Ω standard termination	Open	Open	Shorted			
60Ω load	Shorted	Shorted	Shorted			
Split termination (common mode stabilization)	Shorted	Shorted	open	60Ω	60Ω	4.7nF

The EVM also has footprints for various protection schemes to enhance robustness for extreme system-level EMC requirements.

Table 2-4. CAN Protection and Filtering Configuration

Configuration	Footprint Reference	Use Case	Population and Description
Series resistors or common mode choke (CMC)	R7/R8	Connects the CAN transceiver to the CAN bus	R7 and R8 populated with 0Ω (default population)
		Series resistance protection	Can be populated with MELF resistor as necessary for harsh EMC environment.
	L1 (DNI)	CMC (bus filter)	Can be populated with CMC to filter noise (necessary for harsh EMC environment). Remove R7 and R8 to populate L1.
Bus filtering caps transient protection	C8/C9 (DNI)	Bus filter	Can be populated with filter capacitors for harsh EMC environment.
	D1(DNI)	Transient and ESD protection	Can be populated with TVS diode to add extra protection for system level transients and ESD

2.4 SPI

The SPI communication uses a standard SPI. Physically the digital interface pins are nCS (Chip Select Not), SDI (Slave Data In), SDO (Slave Data Out) and SCLK (SPI Clock). Each SPI transaction is a 32 bit word containing a command byte followed by two address bytes and length bytes. The data shifted out on the SDO pin for the transaction always starts with the Global Status Register (one byte). This register provides the high level status information about the device status. The two data bytes which are the 'response' to the command byte are shifted out next. Data bytes shifted out during a write command is content of the registers prior to the new data being written and updating the registers. Data bytes shifted out during a read command are the current content of the registers and the registers is not updated. The SPI input data on SDI is sampled on the low to high edge of the SCLK. The SPI output data on SDO is changed on the high to low edge of the SCLK.

2.4.1 nCS

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the SDO pin of the device is high impedance allowing a SPI bus to be shared with other devices. When nCS is low the SDO driver is activated and communication can be started. The nCS pin must be held low for the duration of the SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS. There are two pins on the EVM can be used for the SPI Chip Select defined as SPI_CS. Both of these pins are supported with the header pin 13 connected to the TCAN4572-Q1 nCS pin by default. If there is a conflict with this pin, the other supported chip select pin can be used by removing the 0Ω resistor (R30) and installing the resistor on R31 instead. These pins are labeled on the nCS_0 and nCS_1 next to pins 12 and 13 of the board-to-board headers.

Note

The Chip Select signal must transition back to a high following the end of the data transaction and cannot be held low indefinitely as is sometimes common practice when only a single device is on the SPI bus. There are 2 primary reasons for this:

1. The Global Status Register (byte) is always shifted out on the SDO pin for every SPI transaction starting with the first clock cycle following the chip select high-to-low transition.
2. The device counts the number of bits received on the SDI pin which must be a multiple of 32 bits between the chip select transition to low at the beginning of the transaction and then back to high at the completion of the transaction. If the number of bits is not a multiple of 32 bits, the last word of the transfer is ignored and the SPIERR flag is set.

2.4.2 SCLK

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The SPI Data Input is sampled on the rising edge of SCLK and the SPI Data Output is changed on the falling edge of the SCLK. Pin 7 of the board-to-board header is used for the SPI SCLK as is defined as SPI_CLK.

In test mode this pin is used as an EN pin input for testing the CAN transceiver and referenced as EN_INT. When this pin is high, the device is in normal mode. When this pin is low, the pin is in standby mode. For more information about test mode please refer to TCAN4572-Q1 datasheet

2.4.3 SDI

This input pin is used to shift data into the device. Once the SPI is enabled by a low on nCS the SDI samples the input shifted data on each rising edge of the SCLK. The data is shifted into a 32 bit shift register. If the command code is a write, the new data is written into the addressed register only after exactly 32 bits have been shifted in by SCLK and the nCS has a rising edge to deselect the device. If there are not exactly a multiple of 32 bits shifted in to the device during one SPI transaction (nCS low) the last word of the transfer is ignored, the SPIERR flag is set. Pin 15 of the board-to-board header is used for the SPI SDI as is defined as SPI_MOSI.

In test mode this pin is used as an TXD input pin for testing the CAN transceiver and referenced as TXD_INT_PHY.

Note

Due to needing multiples of 32 bits on each SPI transaction the device must be wired for parallel operation of the SPI as a bus with control to the device using nCS and not as a daisy chain of shift registers.

2.4.4 SDO

This pin is high impedance until the SPI output is enabled using nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the Global Fault Flag status which is also the first bit (bit 32) to be shifted out if the SPI is clocked. Once SCLK begins, on the first low to high edge of the clock the SDO retains the Global Fault Flag which is bit 31 of the shift. On the first falling edge of SCLK, the shifting out of the data continues with each falling edge on SCLK until all 32 bits have been shifted out the shift register. Pin 14 of the board-to-board header is used for the SPI SDO as is defined as SPI_MISO.

In test mode this pin is used as an RXD output pin for testing the CAN transceiver and referenced as RXD_INT_PHY.

2.5 Interrupt (nINT)

The nINT is a dedicated open drain global interrupt output pin. This pin needs an external pull-up resistor to VIO to function properly. All interrupt requests are reflected by this pin when pulled low.

Pin 17 of the connection header is connected to the nINT pin. Furthermore, since nINT is an interrupt status pin, an LED has also been added to this pin as a visual indicator to the user on the status of this pin and buffered through a transistor to prevent excessive loading on the device pin. However, since the nINT is a negative logic indicator, the signal is first inverted through an additional transistor such that the LED is illuminated when the nINT pin is low indicating a device interrupt has occurred. Pin 17 of the board-to-board header is used for the nINT as is defined as GPIO_INT.

2.6 Wake Request (nWKRQ)

This pin by default is an open-drain wake-up request pin from a bus wake (WUP) request, and power on (PWRON). The nWKRQ pin is defaulted to a wake enable based upon a wake event (similar to an INH output). In this configuration, the output is pulled low and latched to serve as an enable for a regulator. The nWKRQ pin can be configured by setting 16'h0800[8] = 1 as an interrupt pin for wake interrupts that pulls the output low. Once the wake interrupt flag is cleared, the flag releases the output back to a high. In this configuration, if a wake event takes place, the nWKRQ pin switches from high to low. This pin is an open drain output and requires an external pullup resistor to VIO rail. Some external regulators or power management chips can need a digital logic pin for a wake-up request, this pin can be used. An LED has also been added to this pin as a visual indicator to the user on the status of this pin and buffered through a transistor to prevent excessive loading on the device pin.

Pin 11 of the board-to-board header is used for the nWKRQ as is defined as GPIO_WKRQ.

2.7 Reset (RST)

The RST pin is a device reset pin. This pin has a weak internal pulldown resistor for normal operation. If communication has stopped with the TCAN4572-Q1 the RST pin can be pulsed high and then back low for greater than tPULSE_WIDTH to perform a power on reset to the device. This resets the device to the default settings and puts the device into standby mode. If the device is in normal or standby mode the INH and nWKRQ pins remain active (on) and do not toggle. If the device is in sleep mode and reset is toggled the device enters standby mode and at that time INH and nWKRQ turns on. After a reset has taken place a wait time of ≥ 700µS must be used before reading or writing to the TCAN4572-Q1.

Pin 18 of the board-to-board header is used for the RST as is defined as GPIO_RESET.

2.8 Status LEDs

An LED has been added to each DC power rail on the EVM buffered through a transistor and sourced from the 5V utility rail to not add to the current load of the individual rails more than the current needed for a 10kΩ pullup resistor. For more precise current measurements on the VIO and VCCOUT rails, remove these resistors.

Furthermore, to account for a large voltage range of VDD, a large voltage divider is used on the gate of the FET that controls the VDD LED (D6).

Because some of the signals where an LED is useful, such as nINT and nWKRQ, use negative logic, a second transistor has been added to invert the signals and allow the LED to be on when the IO pin voltage is in the active low state. All pullup resistors connected to the TCAN4572 side of the LED circuit are biased to the VIO rail to accommodate the desired I/O voltage of the MCU.

Table 2-5. LED Indicators

LED	Color	Indication	Control
D4	Green	VCC Power Good	VCC rail active
D5	Green	VIO Power Good	VIO rail active
D6	Green	VDD Power Good	VDD rail active
D2	Red	WKRQ Asserted	CAN_WKRQ low
D3	Red	INT Asserted	CAN_INT low

2.9 Setup

The following sections provide steps for a quick evaluation.

2.9.1 Jumper Configuration

Before powering the EVM, verify the following default jumper settings:

Table 2-6. Default Jumper Configuration

Jumper	Default Position	Function
J8	Pin 2-3	VDD = 5V_AUX
J10	(Pins 1-2, 4-5)	VCC = 5V_AUX, VIO = 3V3_AUX
J1, J2	Installed	Split termination enabled
J4, J6	Installed	3V3_AUX and 5V_AUX enabled

2.9.2 Connecting to a Host MCU/SPI Tool

1. Connect the TCAN4572EVM to a LaunchPad or compatible host MCU board using the board-to-board head connectors J5 and J11.
2. Verify that the host MCU provides 3.3V or 5V on the appropriate supply rails (3V3_AUX, 5V0_AUX).
3. Alternatively, remove the shunt then connect J4 (3.3V) and J6 (5V) headers with appropriate bench supplies.
4. Verify that the SPI pins are connected correctly

2.9.3 CAN Bus Connection

1. Connect the CAN bus network to J9 (DB9, pins 2 and 7 for CANL and CANH respectively) or to J12 (screw terminal).
2. Provide proper bus termination. The on-board split termination (R1/R2/C5) is active by default when J1 and J2 shunts are installed. If TCAN4572EVM is the only CAN node used, place shunt on J3 to enable the 120Ω standard termination.

2.9.4 SPI Communication

Once powered:

1. The host MCU communicates with the TCAN4572-Q1 via SPI through the routed signals on J5/J11.
2. Configure the SPI at the appropriate logic voltage (3.3V or 5V) by setting jumper J10 accordingly.
3. The host MCU must configure the TCAN4572-Q1 registers over SPI before CAN FD communication can begin. Refer to the TCAN4572-Q1 datasheet for register map details.

2.10 Jumper Information

Connection	Type	Description
J1	2-pin jumper	CANH split termination, must be used in combination with J2
J2	2-pin jumper	CANL split termination, must be used in combination with J1
J3	2-pin jumper	CAN standard termination
J4	2-pin jumper	3.3V auxiliary supply from host
J5	20-pin header	Primary host MCU interface (LaunchPad compatible)
J6	2-pin jumper	5V auxiliary supply from host
J7	2-pin jumper	OSC2 single-ended input (GND OSC1)
J8	3-pin jumper	VDD supply selection (5V_AUX or VSUP)
J9	DB9 connector	CAN bus interface
J10	5-pin jumper	VCC/VIO supply selection (5V_AUX or 3V3_AUX)
J11	20-pin header	Secondary host MCU interface (LaunchPad compatible)
J12	6-pin header	CAN bus access terminal
J13	DC barrel jack	2.1mm power jack – VBAT input
J14	3-pin jumper	VBAT selection (DB9 or power jack)
Test point	Red	Voltage supplies
	Black	GND
	Blue	CANH / CANL

3 Hardware Design Files

3.1 Schematic

Figure 3-1 is a schematic diagram of the EVM.

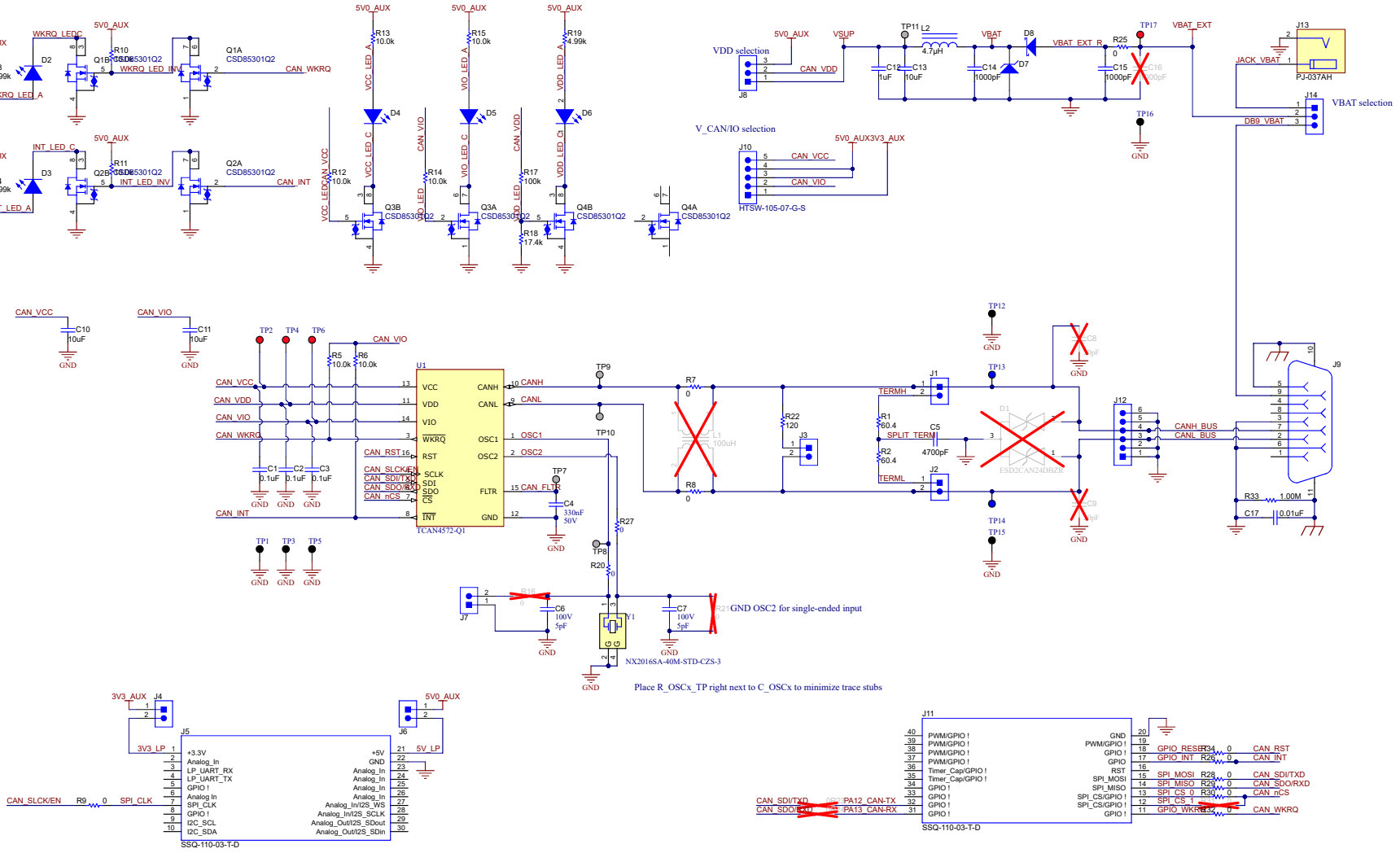

Figure 3-1. EVM Schematic

3.2 Board Layout

EVM Top and EVM Bottom show the top and bottom of the EVM.

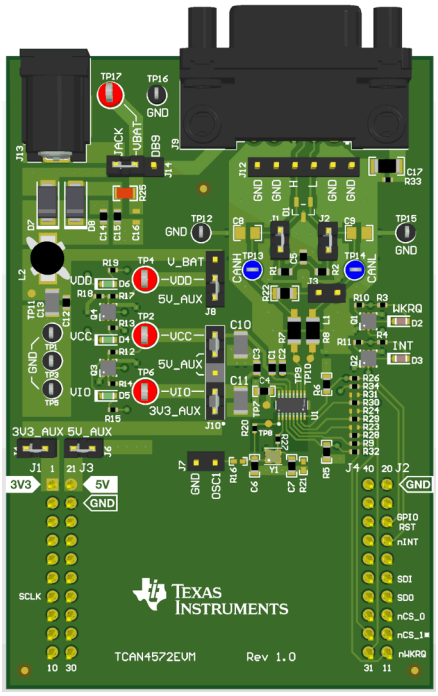

Figure 3-2. EVM Top

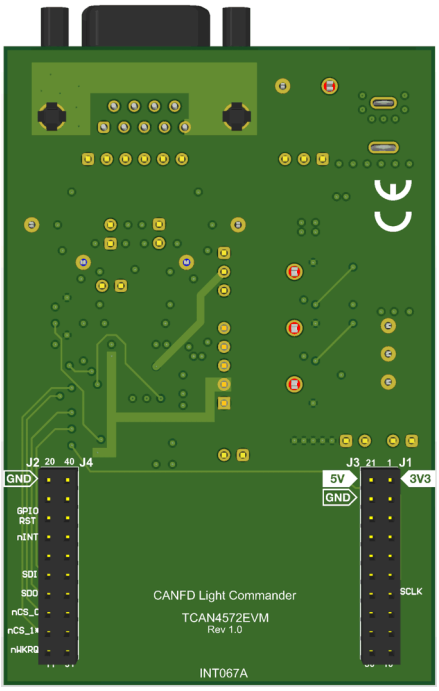

Figure 3-3. EVM Bottom

3.3 Bill of Materials

Table 3-1. Bill of materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1	—	Printed Circuit Board	—	INT067	Any
C1, C2, C3	3	0.1uF	CAP, CERM, 0.1uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1	0603	CGA3E2X7R1H104K080AA	TDK
C4	1	0.33uF	CAP, CERM, 0.33uF, 50V, +/- 10%, X7R	0603	C1608X7R1H334K080AC	TDK
C5	1	4700pF	CAP, CERM, 4700pF, 100V, +/- 10%, X7R	0603	06031C472KAT2A	AVX
C6, C7	2	5pF	CAP, CERM, 5pF, 100V, +/- 5%, C0G/NP0	0603	GRM1885C2A5R0CA01D	MuRata
C10, C11, C13	3	10uF	CAP, CERM, 10uF, 50V, +/- 10%, X7R	1206	CL31B106KBHNNNE	Samsung
C12	1	1uF	CAP, CERM, 1uF, 50V, +/- 10%, X7R	0603	UMK107AB7105KA-T	Taiyo Yuden
C14, C15	2	1000pF	CAP, CERM, 1000pF, 100V, +/- 10%, X7R, AEC-Q200 Grade 1	0603	CGA3E2X7R2A102K080AA	TDK
C17	1	0.01uF	CAP, CERM, 0.01uF, 100V, +/- 5%, X7R	1206	12061C103JAT2A	AVX
D2, D3	2	Red	LED, Red, SMD	LED_0603	150060RS75000	Wurth Elektronik
D4, D5, D6	3	Green	LED, Green, SMD	LED_0603	150060GS75000	Wurth Elektronik
D7	1	30V	Diode, Zener, 30V, 3W	SMA	3SMAJ5936B-TP	Micro Commercial Components
D8	1	40V	Diode, Schottky, 40V, 1A	SMA	MBRA140T3G	ON Semiconductor
J1, J2, J3, J4, J6, J7	6	—	Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07G-S	Samtec
J5	1	—	Receptacle, 2.54mm, 10x2, Tin, TH	10x2 Receptacle	SSQ-110-03T-D	Samtec
J8, J14	2	—	Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07G-S	Samtec

Table 3-1. Bill of materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
J9	1	—	D-Sub, 2.74mm, 9 Position, R/A, TH	D-Sub, 2.74mm, 9 Position, R/A, TH	5747840-5	TE Connectivity
J10	1	—	Header, 100mil, 5x1, Gold, TH	Header, 100mil, 5x1, TH	HTSW-105-07G-S	Samtec
J11	1	—	Receptacle, 2.54mm, 10x2, Tin, TH	10x2 Receptacle	SSQ-110-03T-D	Samtec
J12	1	—	Header, 100mil, 6x1, Gold, TH	6x1 Header	TSW-106-07G-S	Samtec
J13	1	—	Power Jack, 2mm, R/A, TH	Power Jack, R/A, TH	PJ-037AH	CUI Inc.
L2	1	4.7 uH	Inductor, Wirewound, Ferrite, 4.7 µH, 1.65A, 0.08ohm, AEC-Q200 Grade 0	6x6mm	B82462A4472M000	TDK
Q1, Q2, Q3, Q4	4	20V	MOSFET, 2-CH, N-CH, 20V, 6.7A	DQK0006B	CSD85301Q2	Texas Instruments
R1, R2	2	60.4Ω	RES, 60.4, 1%, 0.1W	0603	RC0603FR-0760R4L	Yageo
R3, R4, R19	3	4.99kΩ	RES, 4.99k, 1%, 0.063W	0402	RC0402FR-074K99L	Yageo America
R5, R6	2	10.0kΩ	RES, 10.0k, 1%, 0.1W, AEC-Q200 Grade 0	0603	RMCF0603FT10K0	Stackpole Electronics Inc
R7, R8	2	0Ω	RES, 0, 5%, 0.25W, AEC-Q200 Grade 0	1206	ERJ-8GEY0R00V	Panasonic
R9, R26, R28, R29, R30, R32, R34	7	0Ω	RES, 0, 5%, 0.063W	0402	RC0402JR-070RL	Yageo America
R10, R11, R12, R13, R14, R15	6	10.0kΩ	RES, 10.0k, 1%, 0.063W	0402	RC0402FR-0710KL	Yageo America
R17	1	100kΩ	RES, 100k, 1%, 0.063W	0402	RC1005F104CS	Samsung Electro-Mechanics
R18	1	17.4kΩ	RES, 17.4k, 1%, 0.063W, AEC-Q200 Grade 0	0402	CRCW040217K4FKED	Vishay-Dale
R20, R27	2	0Ω	RES, 0, 5%, 0.063W, AEC-Q200 Grade 0	0402	RK73Z1ETTP	KOA Speer
R22	1	120Ω	RES, 120, 1%, 0.4W	0805	ESR10EZPF1200	Rohm

Table 3-1. Bill of materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R25	1	0Ω	RES, 0, 1%, 0.5W	0805	5106	Keystone
R33	1	1.00MΩ	RES, 1.00M, 1%, 0.1W	0402	ERJ-2RKF1004X	Panasonic
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8	8	—	Shunt, 2.54mm, Gold, Black	Shunt, 2.54mm, Black	60900213421	Wurth Elektronik
TP1, TP3, TP5, TP12, TP15, TP16	6	—	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP2, TP4, TP6, TP17	4	—	Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP13, TP14	2	—	Test Point, Miniature, Blue, TH	Blue Miniature Testpoint	5117	Keystone
U1	1	—	Automotive CAN FD Controller with Integrated Transceiver	SOT23-16	TCAN4572-Q1	Texas Instruments
Y1	1	—	Crystal, 40MHz, 10ppm, 8pF, AEC-Q200 Grade 0	2.0x0.45x1.6mm	NX2016SA-40M-STD-CZS-3	NDK
C8, C9	0	20pF	CAP, CERM, 20pF, 100V, +/- 5%, C0G/NP0	0805	08051A200JAT2A	AVX
C16	0	1000pF	CAP, CERM, 1000pF, 100V, +/- 10%, X7R, AEC-Q200 Grade 1	0603	CGA3E2X7R2A102K080AA	TDK
D1	0	—	24V, 2-Channel ESD Protection Diode for In-Vehicle Networks	SOT-23-3	ESD2CAN24DBZR	Texas Instruments
L1	0	100 uH	Inductor, Ferrite, 100 uH, 0.15A, 2ohm	SMD, 4-Leads, Body 4.7x3.7mm	ACT45B-101-2P-TL003	TDK
R16, R21	0	0Ω	RES, 0, 5%, 0.063W, AEC-Q200 Grade 0	0402	RK73Z1ETTP	KOA Speer
R23, R24, R31	0	0Ω	RES, 0, 5%, 0.063W	0402	RC0402JR-070RL	Yageo America

4 Additional Information

4.1 Trademarks

All trademarks are the property of their respective owners.

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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