The IBIS model, Part 2: Determining the total quality of an IBIS model

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This article is Part 2 of a three-part series. Part 1 (see Reference 1) discussed the fundamental elements of digital input/output buffer information specification (IBIS) simulation models and how they are generated in the SPICE environment. This article, Part 2, investigates IBIS-model validation. Part 3, which will appear in a future issue of the *Analog Applications Journal*, will show how IBIS users investigate signal-integrity issues and problems during the development phase of a printed circuit board (PCB).

IBIS models can be generated from the SPICE deck of an integrated circuit (IC) or in the lab. In both cases, the modeling engineer collects DC data to generate the power-clamp, ground-clamp, pull-up, and/or pull-down data for the various digital buffers on the chip. Following this, data is collected on the output buffer's transient or on the AC rise and fall times. See Reference 1 for more information on these data-collection processes. The IBIS model's transient data replicates the time behavior of output buffers. The modeling engineer acquires the model data with an array of power-supply conditions and junction temperatures. Further enhancements include the addition of the IC's package characteristics, buffer-input chip capacitance, and surrounding documentation. Once the IBIS model exists, the engineer reviews it to verify several quality stages and then produces a validation report that correlates the IBIS model to SPICE simulations or bench data.

Historically, IBIS models have had a reputation of poor quality because many IBIS users have received incorrect models from vendors. The errors range from simple format errors to the model not really portraying the behavior of the buffers in the IC at all. Texas Instruments (TI) is committed to generating quality, reliable IBIS models for customers' signal-integrity investigations.

The IBIS Open Forum's Quality Task Group and Model Review Task Group have formulated a quality-control (QC) process using four QC stages, which are described in the "IBIS Quality Specification," Version 2.0 (Reference 2). The IBIS task groups are subcommittees of TechAmerica's Systems, Standards & Technology Council. Other model users and model makers across the industry have also contributed to this QC process. The four QC stages are:

- Stage 0: An automated quality check using an IBIS parser
- Stage 1: A manual and visual quality check of the model
- Stage 2: Correlation to SPICE or hardware test data
- Stage 3: Correlation to both SPICE and hardware test data

TI performs stages 0, 1, and 2 for its IBIS models, correlating them with SPICE for stage 2. This article will describe the nuances of performing stages 0, 1, and 2 (with SPICE correlation only).

Stage 0: IBIS parsers

The first stage of QC for an IBIS model begins with an IBIS parser program. This computer program provides an essential first-stage model check, inspecting the IBIS file for the validity of the IBIS model data and for syntax errors. This type of program can create "Error," "Warning," and/or "Note" messages in relation to the IBIS model under test, but creating an IBIS model that is free of these messages is possible.

For instance, the parser program IBISCHK4 looks for illegal text types, verifies model types, insures that all proper variables are available for each model, validates end points of data, and performs other housekeeping checks. An example of the results of running an IBISCHK4 program with an IBIS model is shown in the sidebar below.

The "Error," "Warning," and "Note" messages from the parser check provide an opportunity for the IBIS-model designer to identify errors and easily correct them. Running a parser with an IBIS model is essential at the beginning of the quality check; however, the parser does not provide an exhaustive list of IBIS-model errors and does not necessarily guarantee a good model.

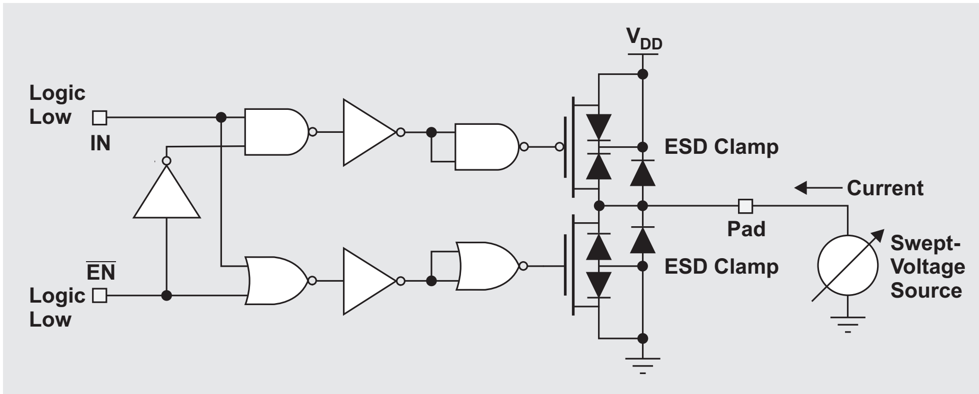
Example IBISCHK4 results

```
ERROR (line 137) - Invalid Model_type ("InputX")
WARNING (line 154) - Vinl should not be specified for model type (null)
WARNING (line 155) - Vinh should not be specified for model type (null)
ERROR - Model 'sdi_3p3': Ramp Not Defined

Errors : 2
Warnings: 2

File Failed
```

Figure 1. Pull-down I-V test circuit for three-state buffer



Parser freeware programs are available for dos32, hp_111, Linux®, and Sun® platforms at the IBIS Open Forum's Web site (http://www.eda.org/ibis). To date there are four parsers available: IBISCHK2, IBISCHK3, IBISCHK4, and IBISCHK5. The level number of each parser program corresponds respectively to the version number of the documented IBIS specification. For example, the most recent parser program, IBISCHK5, corresponds to Version 5.0 of the IBIS specification (Reference 3). TI uses IBISCHK4 and IBISCHK5 to validate its IBIS models.

Stage 1: Visual check

A visual QC check of an IBIS model consists of a manual review of its text and waveforms. During this visual review, the modeling engineer verifies that the header section of the IBIS model contains accurate information. For instance, the header must have the proper products within the product families listed and must have appropriate modeling comments and notes. Following the header, the model must have reasonable package parasitics and well-defined selector entries and must map directly to parameters in the product data sheet, including buffer types, load conditions, input-buffer thresholds, and operating or specified temperature range.

Additionally, the DC and transient waveforms must comply with IBIS standards. The measurement voltage span of the DC waveforms ranges from $-V_{DD}$ to $+2 \times V_{DD}$ (where V_{DD} is the power-supply voltage to the buffer). Across this range, the input and output current must not exceed 2 A. Notes in the comments section in the IBIS model header explain the reason for any excessive currents beyond 2 A. Figure 1 shows the pull-down test configuration for an output buffer, and Figure 2 shows a sample of a pull-down curve from an IBIS model.

Figure 2. Pull-down IBIS graph for DAC7718 output buffer

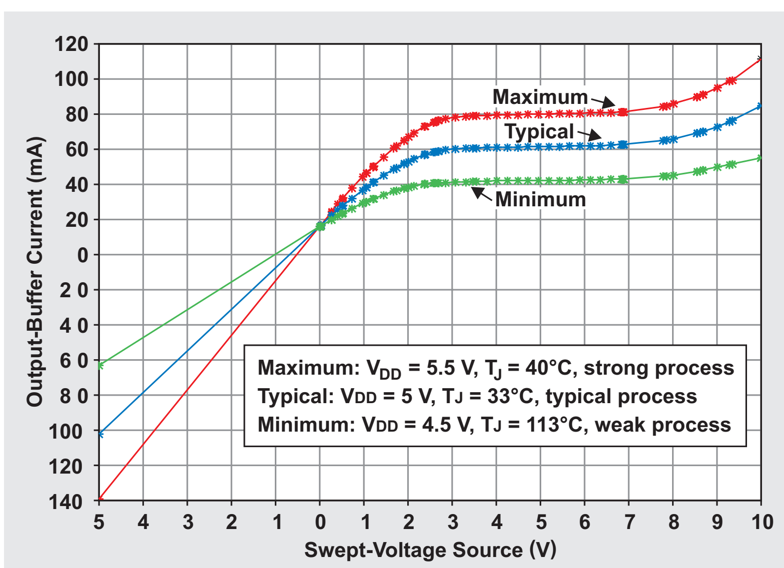


Figure 3. Falling-edge V-t test circuit for an output buffer

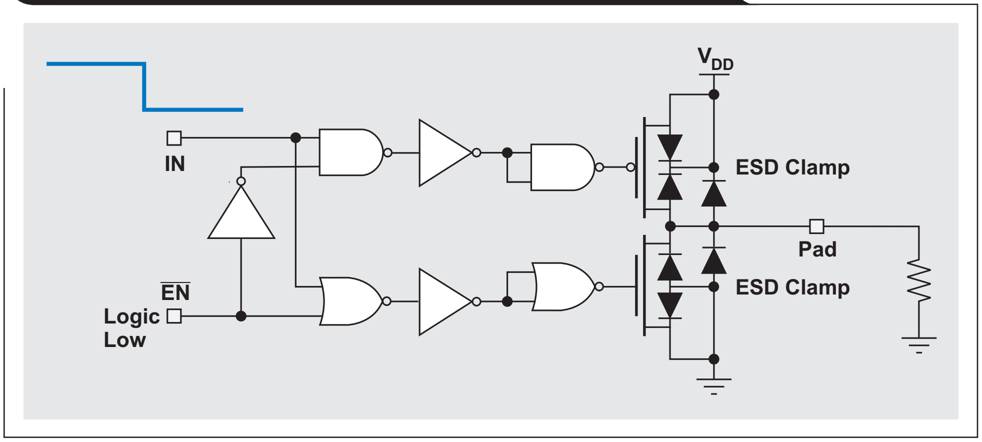


Figure 3 shows the proper test-circuit configuration for the transient falling edge of an output buffer. The resistor following the pad is usually 50 Ω; however, it can be a different value depending on the IC's requirements as stated in the product data sheet.

Figure 4 shows typical falling-edge data for an IBIS model. In this graph, the initial output voltage remains constant for at least two points in time. The data completes its migration to the final value within approximately two-thirds of the total x-axis time.

The text and graphics checks of the IBIS model can be found in Reference 2, where they are described in detail.

Stage 2: Correlation to SPICE or hardware test data

A primary use for IBIS models is to simulate timing and signal integrity, including over/undershoot or crosstalk behavior on an IC's PCB. For stage 2 QC, the modeling engineer compares the performance of an IBIS model in this environment to the device's IC SPICE simulation or test data. The engineer selects appropriate models for a typical board's transmission lines for the specific product under test and compares the test results graphically and with a figure of merit.

Figure 4. DAC7718 input-buffer fall-time analysis

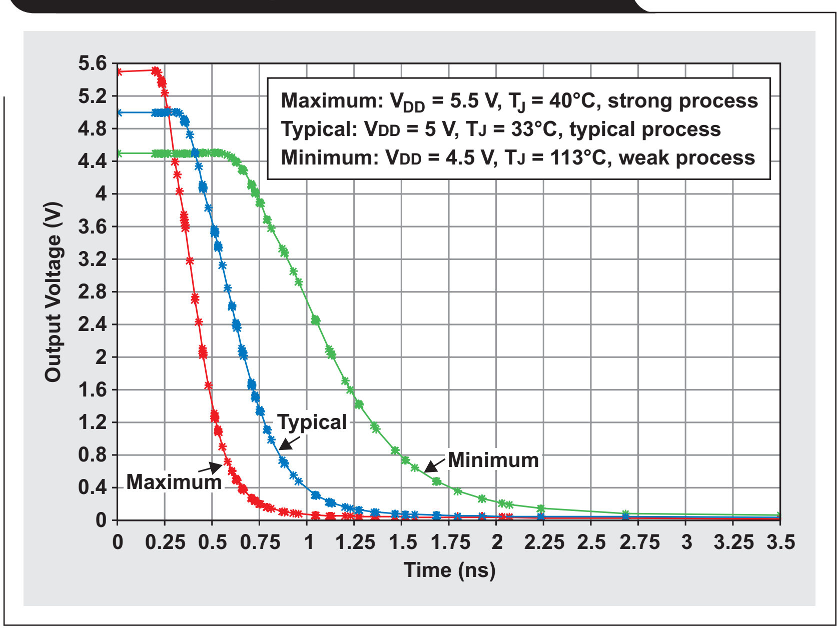


Figure 5 shows an example of a validation test circuit for a SPICE-deck output buffer. This circuit includes the resistive, inductive, and capacitive package parasitics (R_pkg, L_pkg, and C_pkg, respectively) at the output of the SPICE buffer. Following these parasitics is a model of a PCB transmission line, T1. The SPICE simulation collects data at the far end of the transmission line, $V_{(SPICE)}$.

Figure 6 shows an example of an output-buffer IBIS circuit. Notice that the package parasitics do not appear in the circuit, as they are embedded in the IBIS model. This IBIS simulation circuit has the same model of a PCB transmission line (T1) as that in the SPICE-deck simulation circuit.

Figure 7 provides a simulation rise-time comparison between the SPICE and IBIS models based on TI's ADS8319. The outputs were compared at the $V_{(SPICE)}$ node in Figure 5 and the $V_{(IBIS)}$ node in Figure 6. Simulated model conditions were based on a nominal or 1.8-V power supply, a junction temperature of 27°C, and a typical process corner.

Figure 5. Example circuit for SPICE test of an output buffer

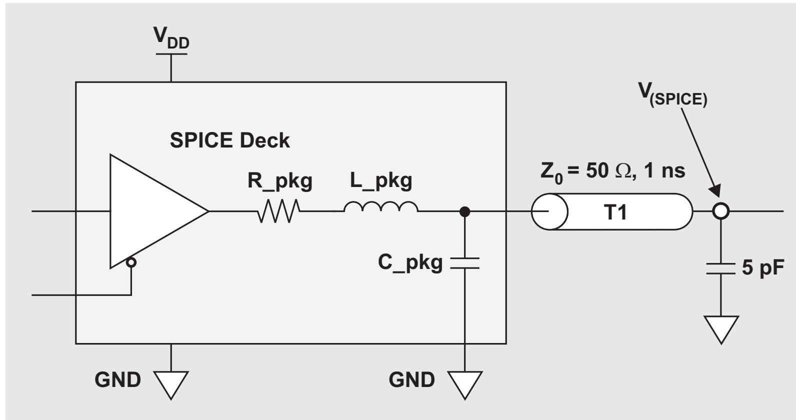


Figure 6. Example circuit for IBIS-model test of an output buffer

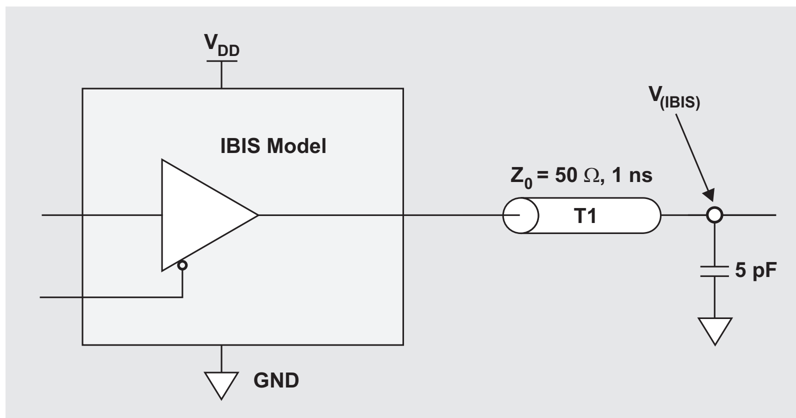


Figure 7. Comparison of output rise times for SPICE and IBIS models

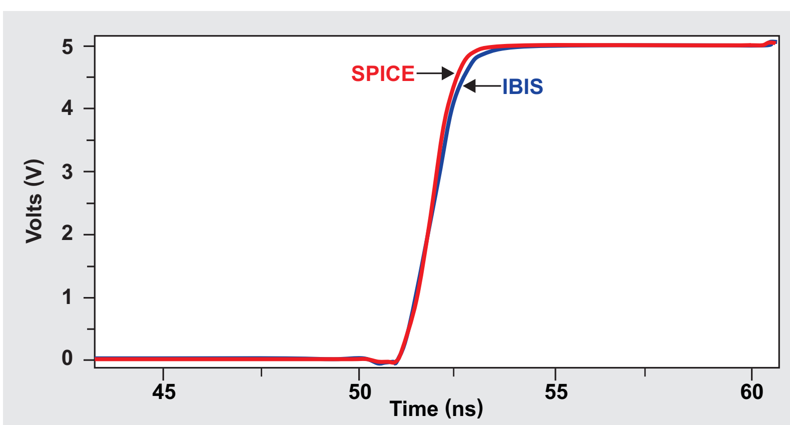


Figure 8. Comparison of output fall times for SPICE and IBIS models

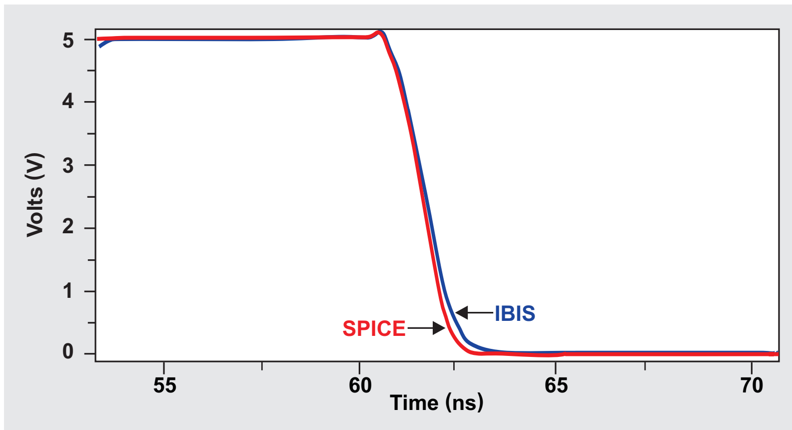


Figure 8 shows a similar fall-time comparison between the SPICE and IBIS models, also based on the ADS8319. Simulated model conditions were based on a 5-V power supply, a junction temperature of 25°C, and a typical process corner.

It is common to calculate a figure of merit (FOM) when curves like those in Figures 7 and 8 are compared. The FOM calculation is

$$\mathrm{FOM} = 100 \times \left[1 - \frac{\sum_{i=1}^{N} \left| X_i(\mathrm{golden}) - X_i(\mathrm{DUT}) \right|}{\Delta X \times N} \right],$$

where X_i(golden) is a time sample of the SPICE-deck curve, X_i(DUT) is the matching time sample of the IBIS-model curve, ΔX is the range of data points, and N is the number of samples. The FOM formula compares the two waveforms by summing the absolute value of the x-axis differences between two data points. This sum is divided by the range of the data points as well as by the number of data points. A preliminary numerical task must map each set of data points to a common x-y grid by interpolation. The FOM for the curves in Figures 7 and 8 combined is 0.68%.

Conclusion

In the past, IBIS models have been known to be of poor quality. This lack of quality can be rectified by using the IBIS Open Forum's QC process. At stage 0 in this process, an IBIS parser software finds errors in syntax and in the IBIS model's format. Stage 1 IBIS QC is implemented with a visual inspection of the text and graphics. At stage 2, the IBIS model is mapped back to the product's data sheet. Finally, as the modeling engineer generates IBIS models for SPICE decks, it is important to complete the loop by validating that the IBIS model does match the SPICE-deck performance in a PCB environment. Using stages 0, 1, and 2 to validate the IBIS model insures reliable simulations with signal integrity.

References

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1. Bonnie Baker, "The IBIS model: A conduit into signal-integrity analysis, Part 1," *Analog Applications Journal* (4Q 2010) slyt390
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Related Web sites

dataconverter.ti.com
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